

Impact of area scaling on the ferroelectric properties of Back-End Of Line compatible $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ and Si:HfO_2 -based MFM capacitors

T. Francois^{1,3*}, L. Grenouillet¹, J. Coignus¹, N. Vaxelaire¹, C. Carabasse¹, F. Aussenac¹, S. Chevalliez¹, S. Slesazek², C. Richter², P. Chiquet³, M. Bocquet³, U. Schroeder², T. Mikolajick^{2,4}, F. Gaillard¹, E. Nowak¹

¹Univ. Grenoble Alpes, CEA, LETI, F-38000 Grenoble, France

²NaMLab gGmbH, Noethnitzer Str. 64a, Dresden, 01187, Germany

³Aix Marseille Univ, Université de Toulon, CNRS, IM2NP, Marseille, France

⁴IHM, TU Dresden, 01062 Dresden, Germany

*Contact email: terry.francois@cea.fr

ABSTRACT

Scaling of planar HfO_2 -based ferroelectric capacitors is investigated experimentally by varying the capacitor area within 5 orders of magnitude, under the scope of limited thermal budget for crystallization. Both $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ (HZO) and Si-doped HfO_2 (HSO) based metal/ferroelectric/metal (MFM) capacitors with 10 nm dielectric film thickness and TiN electrodes are demonstrated to be ferroelectric when integrated in a back-end of line (BEOL) of 130 nm CMOS technology, with a maximum thermal budget below 500°C. When the area of the ferroelectric capacitors is scaled down from 7850 μm^2 to 0.28 μm^2 , no degradation of the remanent polarization ($2 \cdot P_R > 10 \mu\text{C}/\text{cm}^2$ for HSO, $> 30 \mu\text{C}/\text{cm}^2$ for HZO) or of the switching kinetics (down to 100 ns at 3V) is observed. Significant improvement of the field cycling endurance is demonstrated upon area scaling, consistent with the reduction of the total number of defects when devices are shrunk. The results pave the way to future BEOL demonstrations in 130 nm and more advanced nodes with record endurance similar to perovskite ferroelectrics.

Ferroelectric HfO_2 -based materials have been intensively studied since 2011 [1], thanks to their excellent CMOS compatibility and potential for scalability compared to state-of-the-art conventional perovskites [2]. Promising performance has been reported on metal/ HfO_2 -based ferroelectric/metal (MFM) capacitors [3–8]. However, in the vast majority of papers, the area of the capacitors is very large (typically $10^4 \mu\text{m}^2$) with no specific constraints on the thermal budget required for crystallization. Therefore, there is a need to assess the ferroelectric properties of HfO_2 -based capacitors as their area shrinks into the sub μm^2 range, under the constraint of low thermal budgets ($< 500^\circ\text{C}$) required by BEOL integration. In particular, in the perspective of ultra-low power memory applications based on 1T-1C FeRAM architecture, the field cycling endurance until breakdown of ferroelectric HfO_2 scaled capacitors should be extremely high due to the destructive nature of the reading operation.

In this study, both $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ (HZO) mixed oxide and Si:HfO_2 (HSO) doped oxide ferroelectric capacitors with TiN electrodes were integrated in the back-end of line (BEOL) of a 130 nm CMOS technology, between metal 4 (M4) and metal 5 (M5) lines. The oxide films were deposited by atomic layer deposition (ALD) at 300°C and a thickness of 10 nm was targeted. ALD precursors for HfO_2 deposition are HfCl_4 and H_2O . Deposition is performed in an ASM Polygon Pulsar chamber. In the case of Si:HfO_2 films, Si doping was provided by ion implantation performed right after HfO_2 deposition, with an energy and a dose of 4 keV and $3 \cdot 10^{14} \text{cm}^{-2}$ respectively, corresponding to 1% Si effective concentration as extracted in a previous work [9]. A TiN bottom electrode was deposited by physical vapor deposition (PVD) at 350°C and planarized by chemical mechanical polishing (CMP) to

decrease the TiN surface roughness down to 0.18 nm RMS prior to ferroelectric film deposition.

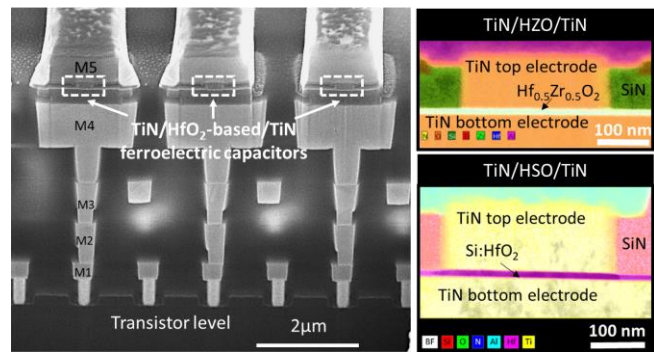


Fig.1: (left) Scanning Electron Microscope (SEM) cross section of TiN/ HfO_2 -based/TiN capacitors integrated in the BEOL of 130 nm CMOS. (right) Energy Dispersive X-ray (EDX) image detail of BEOL integrated 300 nm diameter TiN/HZO/TiN (top) and TiN/HSO/TiN (bottom) capacitors revealing process flow integrity with sharp interfaces.

The 100 nm thick TiN top electrode deposited by PVD at 350°C was further etched to define the 600 nm diameter capacitors (0.28 μm^2). Capacitor encapsulation is then performed by SiN and SiO_2 deposition at 400°C, followed by planarization by CMP, via opening, and M5 deposition performed at 450°C, which corresponds to the highest temperature in this BEOL integration (Fig. 1).

Capacitors with a diameter of 100 μm (7850 μm^2) with the same stacks and similar thermal budgets (500°C) were also fabricated as reference capacitors in order to assess the impact of capacitor scaling (from 7850 μm^2 down to 0.28 μm^2) and BEOL integration on the electrical characteristics.

High-resolution transmission electron microscopy (HRTEM) images reveal that the thermal budget used in BEOL integration ($T_{\max} = 450^\circ\text{C}$) is sufficient to crystallize both the HZO and HSO films, with an in-plane crystallite size of 20 nm (Fig.2).

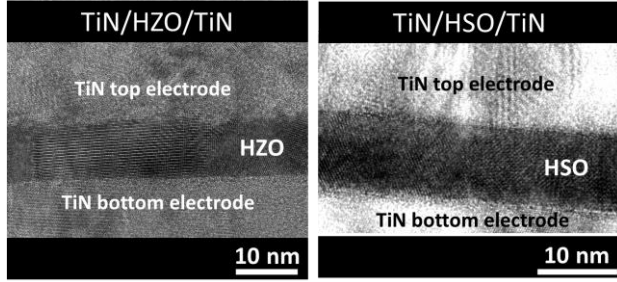


Fig.2: HRTEM cross section images of TiN/10 nm HfO₂-based/TiN capacitors integrated in the BEOL of 130 nm CMOS. (left) TiN/HfZrO₂/TiN capacitor and (right) TiN/Si:HfO₂/TiN capacitor with typical in-plane crystallite size of 20 nm.

Grazing incidence (GIXRD) and in-plane X-ray diffraction (IPXRD) have been used to analyze the films using laboratory X-ray sources (Panalytical-Empyrean® and Rigaku-Smartlab® with a wavelength of $\lambda=1.5406 \text{ \AA}$). Full sheet wafers of HZO and HSO with the same deposition and similar annealing ($< 500^\circ\text{C}$) conditions have been used for the analysis. X-ray diffraction patterns inform about phase nature and microstructure of the films. First, a strong peak around 30° is noticed (Fig.3), which can be attributed to a ferroelectric orthorhombic (111) or a tetragonal (101) phase reflection [1]. A small halo at 28.5° is also indicative of a residual proportion of monoclinic phase. The combination of GI and IP geometry provides insight about crystallite aspect ratio and the stress state. In GI geometry, crystallites are probed at an inclination ψ from the out-of-plane direction of $2\theta/2 - \alpha$ where α is the grazing angle (e.g. $\psi \approx 14.5^\circ$ for o(111) peak). In in-plane configuration, the inclination ψ is 90° . Crystallite sizes are evaluated using Scherrer's [10] formula,

$$l^* = \frac{k\lambda}{B \cos(\theta)}$$

where B is the peak broadening corrected from the instrumental one, K is a dimensionless shape factor taken at 0.94, and 2θ the peak position. This evaluation leads to a pancake like crystallite aspect ratio of $L^*[\psi = 14.5^\circ] = 8.6 \text{ nm}$ and $L^*[\psi = 90^\circ] = 17.2 \text{ nm}$. This statistical observation is in good agreement with the dimension of a unique crystallite seen in the cross-sectional TEM image (Fig. 2). The two o(111) peak positions at $\psi = 14.5^\circ$ and $\psi = 90^\circ$ also provide the stress magnitude in the HfO₂-based film. If the stress state is supposed iso-biaxial and the film elastically isotropic, one can write the classical sinus square formula [11] as:

$$\varepsilon_\psi = \frac{1 + \eta}{M} \sigma \sin^2 \psi - \frac{\eta}{M} \sigma$$

Where $\eta = -\varepsilon_{\psi=0^\circ} / \varepsilon_{\psi=90^\circ}$, and the biaxial $M = E/(1-\nu)$ modulus are introduced. From the lattice extracted for Bragg peak position, one can deduce the free-of-stress interplanar spacing and the stress level. Using $E = 384 \text{ GPa}$ and $\nu = 0.3$ [12], for

the HZO capacitor stack with maximum thermal budget $< 500^\circ\text{C}$, a $d_0 = 2.9418 \text{ \AA}$ and $\sigma = 3.35 \text{ GPa}$ are found. This high level of tensile stress is in accordance with previous studies [13,14] and is an indication of the link between high polarization and stress magnitude in HfO₂-based films [15,16]. Similar results were obtained on the HSO stack where $d_0 = 2.9396 \text{ \AA}$ and $\sigma = 2.84 \text{ GPa}$ are extracted.

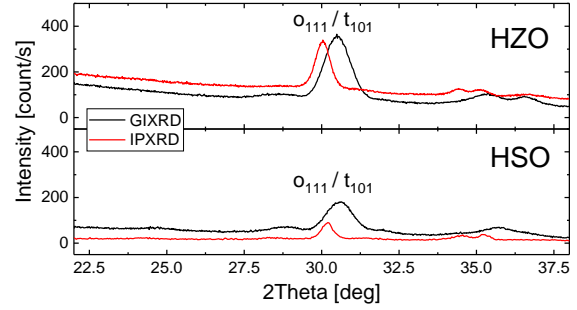


Fig. 3: Grazing incidence and in-plane X-ray diffraction spectra from full sheet (top) TiN/HZO/TiN and (bottom) TiN/HSO/TiN annealed samples with maximum thermal budget $< 500^\circ\text{C}$.

XRD results demonstrated the presence of a peak at 30° , which can be attributed to the ferroelectric orthorhombic phase but also to a non-ferroelectric tetragonal phase. Hence, electrical characterization has been performed to quantify the ferroelectric behavior and confirm the presence of the orthorhombic phase. A Keysight B1500 equipped with two B1530 Waveform Generator/Fast Measurement Units has been used to measure the current response of capacitors during a voltage ramp. Ferroelectric materials have two typical metrics extracted from this response: the remanent polarization $2 \cdot P_R = |P_R^+| + |P_R^-|$ corresponding to the memory window in FeRAM architectures and the coercive field E_C , i.e. the switching electrical field.

Positive Up Negative Down (PUND) ($\pm 4 \text{ V}/10 \text{ kHz}$) methodology has been used, allowing the extraction of ferroelectric parameters without any parasitic non-ferroelectric currents [17]. A triangular wake-up cycling of $\pm 4 \text{ V}/100 \text{ kHz}$ has been used to evaluate the evolution of $2 \cdot P_R$ and E_C along cycling. Fig.4 shows the typical polarization versus electric field hysteretic behavior of ferroelectrics on both HZO and HSO-based capacitors for large ($\varnothing 100 \mu\text{m}$) and scaled ($\varnothing 600 \text{ nm}$) diameters, resulting from the integration of the ferroelectric switching currents represented above.

First, for large-scaled $\varnothing 100 \mu\text{m}$ capacitors, the remanent polarization is lower in the HSO case compared to the HZO case, which is commonly observed in the literature and attributed to a lowest crystallization temperature for HZO compared to HSO [18]. HZO is also very often used as it exhibits one of the highest polarization among all dopants [2]. Nevertheless, both materials possess a significant remanent polarization, even in pristine state (see black dashed-lines of Fig.4 bottom), which confirms the presence of orthorhombic phase observed in XRD results even at low thermal budget (Fig.3).

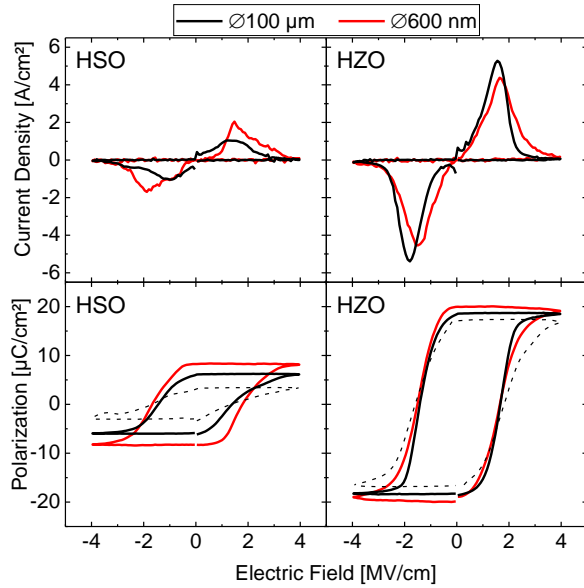


Fig. 4: (top) Current density and (bottom) polarization versus electric field of HSO and HZO capacitors with thermal budget $< 500^{\circ}\text{C}$, after 10^4 wake-up cycling of $\pm 4\text{V} / 100\text{ kHz}$. For the characterization of $\text{\O}600\text{ nm}$ capacitors, PUND measurement has been repeated several times and averaged to reduce the parasitic noise as the nA range is close to the highest sensitivity of the tool. Black dashed-lines correspond to the pristine polarization of $\text{\O}100\text{ }\mu\text{m}$ capacitors.

Then, for $\text{\O}600\text{ nm}$ BEOL-integrated capacitors, the ferroelectric response of HSO is lower than for HZO, as previously seen on large area capacitors. When shrinking the capacitors from $7850\text{ }\mu\text{m}^2$ down to $0.28\text{ }\mu\text{m}^2$, the ferroelectric behavior of the layer is maintained and similar remanent polarization is measured, *i.e.* the overall orthorhombic/tetragonal phase ratio remains unchanged. Finally, neither the difference of material nor the shrinking of the devices have significantly affected the coercive field of the ferroelectric layers. E_C varies between 1.4 MV/cm and a maximum of 2 MV/cm along electrical cycling, in agreement with literature [18–20].

During the electrical characterization along the $\pm 4\text{V} / 100\text{ kHz}$ triangular wake-up cycles, all tested $\text{\O}100\text{ }\mu\text{m}$ capacitors have encountered hard-breakdown before 10^6 cycles for both materials. At the same time, $\text{\O}600\text{ nm}$ capacitors remained functional and ferroelectric even after 10^9 cycles. Thus, in Fig. 5, the cycle-to-breakdown (CBD) of both $\text{\O}100\text{ }\mu\text{m}$ and $\text{\O}600\text{ nm}$ capacitors have been evaluated with triangular wake-up cycling (100 kHz) and various cycling fields. Cycling fields $> 4\text{ MV/cm}$ have been used to accelerate the hard-breakdown, mostly for $\text{\O}600\text{ nm}$ capacitors, and a minimum of 5 capacitors have been tested for all conditions.

As for Fig. 4, all the tested capacitors remained ferroelectric until hard-breakdown, which is the failure mechanism of these devices. Indeed, $2 \cdot P_R$ remained at least higher than $5\text{ }\mu\text{C/cm}^2$, which is the worst case for $100\text{ }\mu\text{m}$ HSO capacitors cycled at 3 MV/cm . All capacitors showed various wake-up / fatigue behaviors depending on the cycling electric field, *e.g.* high cycling electric field of 6 MV/cm leads to a strong wake-up, higher $2 \cdot P_R$ values and dielectric breakdown even before the fatigue state. A typical trend is highlighted: decreasing the

cycling field improves the CBD, *i.e.* decreases the probability of formation of a conductive filament that causes the hard-breakdown. Another CBD improvement is observed when shrinking the capacitors area from $7850\text{ }\mu\text{m}^2$ to $0.28\text{ }\mu\text{m}^2$, no matter which material is considered.

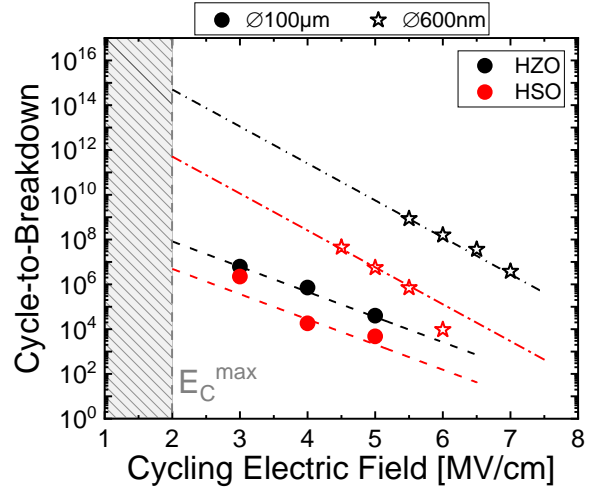


Fig. 5: Mean Cycle-to-Breakdown (CBD) of both materials under various cycling electric fields. At least 5 capacitors have been tested for all conditions. Dashed-lines as guides for the eye.

For example, at 5 MV/cm cycling field, CBD is increased by 3 orders of magnitude for the HSO case and 5 orders of magnitude for the HZO case. This expected behavior is attributed to the reduced total number of defects susceptible to initiate hard-breakdown when shrinking from $7850\text{ }\mu\text{m}^2$ down to $0.28\text{ }\mu\text{m}^2$ [21]. The voltage acceleration factor is found slightly higher when dealing with scaled capacitors, supposedly due to peripheral effects [22]. The HSO case is found to have a lower CBD than the HZO case, on both $7850\text{ }\mu\text{m}^2$ and $0.28\text{ }\mu\text{m}^2$ capacitors. Indeed, even though the ion implantation technique allows a thinner control of the doping concentration and could be used for thinner films, the quantity of defects in the HfO_2 layer in this case is much higher than with ALD technique, explaining such behavior.

Finally, at 2.5 MV/cm cycling field, *i.e.* an operating electric field superior to the highest coercive field of the devices, CBD is extrapolated to be 10^{11} cycles for the HSO case and even 10^{14} for the HZO case. Shrinking the capacitors and decreasing the cycling field is not only determining for industrial applications, but also greatly improves the cycling capability of the devices.

The required performance for a memory technology is application dependent. Optimizing the operation conditions for a specific application will result in a trade-off between several parameters, such as the cycling endurance, the operating voltage and the programming speed. As previously discussed, $2 \cdot P_R$ corresponds to the memory window in a FeRAM architecture and is directly linked to the proportion of ferroelectric domains switched by the write/erase pulses. This switched proportion has to be evaluated to assess the possible operating voltages and programming speed of the devices. Therefore, square pulses have been used instead of the triangular ones as it is most often used in the memory

operation. A specific electrical sequence has been used to evaluate the switching efficiency of a square pulse with various amplitudes/widths. More details have already been published in [23]. This methodology allows a precise measurement of the polarization switched by the square pulses themselves, named $2 \cdot P_{sw}$. This sequence was applied after 10^4 wake-up triangular cycles to minimize polarization variation during the test. Fig. 6 depicts the switching efficiency $= (2 \cdot P_{sw} / 2 \cdot P_R^{PUND}) \times 100$ of both materials, whether it is a large-scaled $\text{Ø}100 \mu\text{m}$ capacitor (top) or a BEOL-integrated $\text{Ø}600 \text{ nm}$ capacitor (bottom). Fig. 6 highlights that all capacitors can switch efficiently ($>75\%$) with a 100 ns pulse width. At higher frequencies, $\text{Ø}100 \mu\text{m}$ capacitors have a reduced switching efficiency compared to $\text{Ø}600 \text{ nm}$ capacitors, which is attributed to a RC effect, as the bottom electrode is connected from the periphery of the capacitor. Long pulses of lower voltage than the coercive voltage are able to switch the ferroelectric domains, consistently with ferroelectric switching dynamic models such as the nucleation-limited switching (NLS) [8,24,25] or the Kolmogorov-Avrami-Ishibashi model [26].

Finally, considering a high switching efficiency $>90\%$, optimized operating conditions of 3 V pulse amplitude and 30 ns pulse width are highlighted for both HZO and HSO-based $\text{Ø}600 \text{ nm}$ capacitors. With such optimized operating conditions, *e.g.* lower operating voltage combined with short pulse duration, the endurance of the $\text{Ø}600 \text{ nm}$ capacitors is expected to increase even further compared to experimental trends reported in Fig. 5 [23].

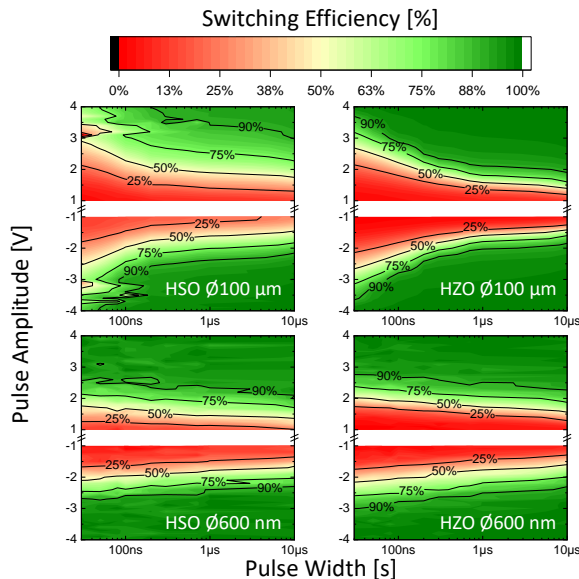


Fig. 6: Switching efficiency map on (left) HSO and (right) HZO capacitors. (top) corresponds to $\text{Ø}100 \mu\text{m}$ capacitors while (bottom) is for $\text{Ø}600 \text{ nm}$ capacitors. The measurement methodology is described in Fig. 9 of [23]. Rising and fall time of the pulses are $t_{rise/fall} = 100\text{ns}$.

$\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ and Si:HfO_2 10 nm ferroelectric films with TiN electrodes have been successfully integrated in the back-end of line of a 130nm CMOS technology. HRTEM images and XRD measurements confirm the crystallization of the films with

thermal budget below 500°C . Crystallite dimensions are extracted, resulting in a pancake like shape with 20 nm in-plane size and out-of plane size corresponding to the thickness of the film. The orthorhombic ferroelectric phase determined from XRD is confirmed by in-depth electrical characterization. The impact of the capacitor area shrink on the ferroelectric characteristics of the devices is examined by systematically comparing $0.28 \mu\text{m}^2$ BEOL-integrated capacitors with $7850 \mu\text{m}^2$ capacitors of the same stack fabricated with similar process conditions. No detrimental impact on the ferroelectric parameters is demonstrated, with similar remanent polarization, coercive fields, switching speeds and operating voltages. Optimized operating conditions of 3 V pulse amplitude / 30 ns pulse width are extracted from switching efficiency maps for both BEOL-integrated materials. Considering a maximum of 30 nA on 600 nm capacitors (Fig. 4), such operating conditions demonstrate low programming power of 2.7 fJ per bit, which is at least 1000 times lower than other emerging memories like PCRAM or OxRAM [27]. Significant CBD improvement is highlighted for both materials when shrinking the capacitors leading to a projected endurance value of 10^{14} cycles for the HZO $\text{Ø}600 \text{ nm}$ capacitors under 2.5 MV/cm cycling. Such endurance performance for HfO_2 -based capacitors is promising to bridge the gap towards the 10^{15} cycling capability as reported for commercial perovskite-based memories.

This project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No. 780302 (3eFERRO project). The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

- [1] T.S. Böske, J. Müller, D. Bräuhäus, U. Schröder, U. Böttger, Applied Physics Letters 99 (2011) 102903.
- [2] M.H. Park, Y.H. Lee, T. Mikolajick, U. Schroeder, C.S. Hwang, MRS Communications 8 (2018) 795–808.
- [3] D. Das, V. Gaddam, S. Jeon, IEEE Electron Device Letters 41 (2020) 34–37.
- [4] T. Schenk, C.M. Fancher, M.H. Park, C. Richter, C. Künneth, A. Kersch, J.L. Jones, T. Mikolajick, U. Schroeder, Advanced Electronic Materials 5 (2019) 1900303.
- [5] S. Mueller, J. Muller, U. Schroeder, T. Mikolajick, IEEE Transactions on Device and Materials Reliability 13 (2013) 93–97.
- [6] A.G. Chernikova, M.G. Kozodaev, D.V. Negrov, E.V. Korostylev, M.H. Park, U. Schroeder, C.S. Hwang, A.M. Markeev, ACS Applied Materials & Interfaces 10 (2018) 2701–2708.
- [7] M. Si, X. Lyu, P.R. Shrestha, X. Sun, H. Wang, K.P. Cheung, P.D. Ye, Applied Physics Letters 115 (2019) 072107.
- [8] X. Lyu, M. Si, P.R. Shrestha, K.P. Cheung, P.D. Ye, in: 2019 IEEE International Electron Devices Meeting (IEDM), 2019, p. 15.2.1-15.2.4.
- [9] T. Francois, J. Coignus, L. Grenouillet, M. Barlas, B. Bessif, N. Vaxelaire, H. Boutry, M. Coig, E. Vilain, N. Rambal, J.-M. Pedini, Y. Morand, F. Mazen, E. Nowak, F. Gaillard, in: 2018.
- [10] P. Scherrer, Nachr. Ges. Wiss. Goettingen. (1918).
- [11] I.C. Noyan, J.B. Cohen, Residual Stress: Measurement by Diffraction and Interpretation, Springer-Verlag, New York, 1987.
- [12] M.H. Park, Y.H. Lee, H.J. Kim, T. Schenk, W. Lee, K.D. Kim, F.P.G. Fengler, T. Mikolajick, U. Schroeder, C.S. Hwang, Nanoscale 9 (2017) 9973–9986.
- [13] T.D. Huan, V. Sharma, G.A. Rossetti, R. Ramprasad, Physical Review B 90 (2014).
- [14] R. Materlik, C. Künneth, A. Kersch, Journal of Applied Physics 117 (2015) 134109.
- [15] T. Shiraishi, K. Katayama, T. Yokouchi, T. Shimizu, T. Oikawa, O. Sakata, H. Uchida, Y. Imai, T. Kiguchi, T.J. Konno, H. Funakubo, Applied Physics Letters 108 (2016) 262904.
- [16] S.J. Kim, D. Narayan, J.-G. Lee, J. Mohan, J.S. Lee, J. Lee, H.S. Kim, Y.-C. Byun, A.T. Lucero, C.D. Young, S.R. Summerfelt, T. San, L. Colombo, J. Kim, Applied Physics Letters 111 (2017) 242901.
- [17] I. Fina, L. Fàbrega, E. Langenberg, X. Martí, F. Sánchez, M. Varela, J. Fontcuberta, Journal of Applied Physics 109 (2011) 074105.

- [18] M.H. Park, Y.H. Lee, H.J. Kim, Y.J. Kim, T. Moon, K.D. Kim, J. Müller, A. Kersch, U. Schroeder, T. Mikolajick, C.S. Hwang, *Advanced Materials* 27 (2015) 1811–1831.
- [19] U. Schroeder, E. Yurchuk, J. Müller, D. Martin, T. Schenk, P. Polakowski, C. Adelman, M.I. Popovici, S.V. Kalinin, T. Mikolajick, *Japanese Journal of Applied Physics* 53 (2014) 08LE02.
- [20] S. Clima, D.J. Wouters, C. Adelman, T. Schenk, U. Schroeder, M. Jurczak, G. Pourtois, *Applied Physics Letters* 104 (2014) 092906.
- [21] J. Sune, *IEEE Electron Device Letters* 22 (2001) 296–298.
- [22] E.Y. Wu, J. Suné, *IEEE TRANSACTIONS ON ELECTRON DEVICES* 56 (2009) 9.
- [23] T. Francois, J. Coignus, L. Grenouillet, J.P. Barnes, N. Vaxelaire, J. Ferrand, I. Bottala-Gambetta, M. Gros-Jean, S. Jeannot, P. Boivin, in: 2019 IEEE 11th International Memory Workshop (IMW), IEEE, 2019, pp. 1–4.
- [24] A.K. Tagantsev, I. Stolichnov, N. Setter, J.S. Cross, M. Tsukada, *Physical Review B* 66 (2002).
- [25] N. Gong, X. Sun, H. Jiang, K.S. Chang-Liao, Q. Xia, T.P. Ma, *Applied Physics Letters* 112 (2018) 262903.
- [26] A. N. Kolmogorov, “On the Statistical Theory of Crystallization of Metals”, *Izv. Akad. Nauk SSSR, Ser. Mat.*, No. 3, 1937, pp. 355-359.
- [26] M. Avrami, *The Journal of Chemical Physics* 8 (1940) 212–224.
- [27] G. Sassine, D. Alfaro Robayo, C. Nail, J.-F. Nodin, J. Coignus, G. Molas, E. Nowak, in: 2018 IEEE International Memory Workshop (IMW), IEEE, Kyoto, 2018, pp. 1–4.