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16kbit HfO₂:Si-based 1T-1C FeRAM Arrays Demonstrating High Performance Operation and Solder Reflow Compatibility

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Abstract—16kbit 1T-1C FeRAM arrays are demonstrated at 130nm node with TiN/HfO₂:Si/TiN ferroelectric capacitors integrated in the Back-End-of-Line (BEOL). Zero bit failure is reported at the array level, with memory window fully open down to 2.5V programming voltage, capacitor area down to 0.16μm² and switching speed down to 4ns. Promising endurance is reported at the array level up to 10⁷ cycles. For the first time, solder reflow compatibility is demonstrated for HfO₂-based FeRAM. These results pave the way to competitive ultra-low power embedded non-volatile memories at more advanced nodes.

INTRODUCTION

Since 2011 [1], ferroelectric HfO₂ is paving the way towards the next generation of ferroelectric non-volatile memory devices for high endurance and ultra-low power applications. Recently, Hf_{0.5}Zr_{0.5}O₂ [2] and HfO₂:Si [3] based ferroelectric capacitors were successfully integrated in the Back-End-Of-Line (BEOL) of 130nm CMOS technology, demonstrating their scalability and compatibility with low thermal budgets. Functional FeRAM arrays were reported for the first time by Okuno *et al.* [4,5], in which the Hf_{0.5}Zr_{0.5}O₂-based capacitor (1C) of the bitcell is integrated in the Middle-Of-Line (MOL) on the contact of the transistor (1T), prior to BEOL process. This integration approach allows crystallization anneal higher than 500°C to be used [5]. In this paper, 16kbit 1T-1C FeRAM arrays with BEOL integrated HfO₂:Si-based ferroelectric capacitors are designed and demonstrated for the first time. State distributions at the array level, operating voltages, switching kinetics, endurance, data retention and solder reflow immunity are assessed, and scaling potential is discussed.

1T-1C FERAM ARRAY INTEGRATION AT 130NM NODE

TiN/HfO₂:Si(10nm)/TiN capacitors with designed areas of 0.36μm², 0.24μm² and 0.16μm² have been integrated in the BEOL of 130nm CMOS technology between M4 and M5 (Fig. 1) [3]. Various test structures have been designed, from single bitcell with one capacitor connected to the drain of a transistor (1T-1C), up to 16kbit 1T-1C arrays. Stand-alone 1T-1C structures have been electrically measured at wafer level with Positive-Up-Negative-Down (PUND) technique (4.8V 10kHz) [6] along square-shaped cycling (4.8V 2μs), in order to mimic the electrical signal waveform used in 16kbit array (Fig. 2).

Remanent polarization (2.P_R) shows the expected wake-up, stable and fatigue phases of HfO₂-based ferroelectric capacitors, with a maximum 2.P_R value of 40μC/cm². Extracted coercive fields below 2MV/cm promise low voltage operation, as discussed later on. In the following, and unless specified, 16kbit array reported data have been measured after an initial wake-up operation of 1000 cycles using a 4.8V 2μs square signal.

Fig. 3 shows a layout view of the 128x128 16kbit array, which features Scan Chains for bitcell addressing and circuit control, Pulse Generators for tuning pulse widths over more than 3 decades, capacitive bitcell reading via Sense Amplifiers and Write-Back capability after destructive read operations. 1T-1C programming operations and conventions are summarized in Fig. 4a: ferroelectric 0 and 1 states are defined as bitcell states after pulsing Source Line (SL) and Bit Line (BL), respectively. Subsequent read operations consist in an attempt to program a 0 state via SL pulsing, with floating BL potential: depending on capacitor ferroelectric state, BL potential elevates at either V_{BL}^{NSW} (no ferroelectric switch, *i.e.* pure dielectric response) or V_{BL}^{SW} (dielectric response with an additional contribution of switched ferroelectric charge) (Fig. 4b). V_{BL} is then compared to an *a priori* fixed reference potential V_{REF} with one Sense Amplifier (SA) per BL (Fig. 4c). Digital SA outputs are stored in a buffer prior to data reading.

16KBIT 1T-1C FERAM ARRAY PERFORMANCE

The distributions of 0 and 1 states have been extracted by alternating several programming and read operations (4.8V 2μs) with incremental V_{REF} values. Both are found to follow normal distributions and a fully opened 170mV Memory Window (MW) is demonstrated at 16kbit-scale with 0.36 μm² integrated capacitors, without any bit failure (Fig. 5a). Extrapolating towards higher statistics demonstrates MW still opened at 6σ=32mV, suggesting potential for Gbit-size arrays. The bitcell-wise difference ΔV_{BL}=V_{BL}^{SW}-V_{BL}^{NSW} isolates the contribution of pure ferroelectric switching and is found homogeneously distributed across the 16kbit array without design-driven variation (Fig. 5b).

From measured distributions, V_{REF}=0.85V is defined for the 16kbit array digital reading operations. As expected from Fig. 5a, a bit failure free bitmap pattern is reported with 4.8V 2μs

operations (**Fig. 6**). The destructive nature of read operation does not allow to track directly the retention of polarization during high temperature bake. Data retention evaluation has thus been performed on a single 16kbit array subdivided in 8 regions, each one being pre-programmed and baked equivalently but read with different V_{REF} values in order to assess distribution drift with temperature bake (**Fig. 7**). A nominal 0.85V V_{REF} operation shows no bit failure after a 10^4 s bake at 125°C, while V_{REF} values targeting the core of t_0 distributions show a slight distribution drift (**Fig. 8**). As MW remains fully open after 10^4 s at 125°C, no satisfactory extrapolation up to 10 years can be provided with confidence at the moment. Promising data retention is confirmed by the demonstration of HfO₂:Si FeRAM immunity to solder reflow. A pattern pre-programmed at 4.8V 2 μ s on the 16kbit array is found able to withstand three successive Surface Mount Technology (SMT) temperature stresses (max temperature of 260°C for 30s), without any bit failure for both memory states (**Fig. 9**).

Internal Pulse Generators (PG) allow to probe the 1T-1C FeRAM switching kinetics from 1.7 μ s down to 520ps. From 0 and 1 states pre-programmed at 4.8V 2 μ s, various pulse widths and amplitudes have been applied to the entire 16kbit array and bit failures are here reported for bitcells not capable to overcome $V_{REF}=0.85$ V (**Fig. 10**). For the first time, a constant V_{REF} sensing offer a realistic vision of both states switching kinetics. Evaluation using other V_{REF} values has been found to improve sensitivity to fast pulses for one state while being detrimental for the other one. Switching capability at 4ns is demonstrated at 4V for both states (**Fig. 10**). Based on this voltage-time trade-off investigation performed at the 16kbit array level, a 40ns 4V pulse is defined for endurance evaluation. Unlike previously reported data measured after 10^3 4.8V 2 μ s wake up cycles, endurance evaluation has been conducted at 16kbit scale without bitcell electrical preconditioning (*i.e.* starting at pristine state). Here again, an optimized $V_{REF}=0.85$ V shows excellent 16kbit FeRAM operation during 10^7 cycles (test limit) (**Fig. 11a**). Distributions measured after 10^7 cycles show that bit failures originate from Hard and Soft Breakdown events (0.46% and 0.90%, respectively), while ferroelectric performance is preserved as seen from $\Delta V_{REF}>0$ at 0σ (**Fig. 11b**). No preferential spatial location for breakdown is found in post-endurance bitmaps (**Fig. 11c**). In the case of 4V device operation, dielectric reliability is thus the limiting factor for 10nm HfO₂:Si films and scaling down the operating voltage is expected to improve endurance performance [7] towards the intrinsic limits of ferroelectric fatigue.

VOLTAGE AND AREA SCALING ASSESSMENT

Distributions of lower voltage operations down to 2.5V (2 μ s-wide pulses) are represented in **Fig. 12a**. Compared to the monotonic dependence of remanent polarization with programming voltage measured on stand-alone 1T-1C bitcell (**Fig. 12b**), MW at the 16kbit scale is found optimal at intermediate voltage, e.g. 4V for 0.36 μ m² area capacitors. The expected reduction of MW with voltage scaling (*i.e.* less

ferroelectric domains being switched) is partly compensated by improved distribution slopes, attributed to their dielectric component rather than a ferroelectric effect (**Fig. 12a**). The origin of 0 state slope partly lies in a gradient effect along the 128 BLs of the array, as seen in the 0 state bitmap reported in **Fig. 13a**. Regarding the homogeneity of ferroelectric properties within the array, this effect is attributed to BL-dependent C_{BL} values, thus a design-induced variation. 0 state dependence with BL location has been suppressed while preserving the variability within each WL in order to simulate a future design update correcting from C_{BL} variations. **Fig. 13b** shows an improvement of 0 state from 28mV/ σ down to 19mV/ σ at 4.8V and a subsequent improvement of the 4.8V MW from 170mV to 188mV (less distribution overlap).

Capacitor area scaling down to 0.16 μ m² is reported in **Fig. 14** for various operating voltages. MW opened at 16kbit scale (no bit failure) is demonstrated for 3V operation on 0.16 μ m² scaled bitcells. Correcting for C_{BL} variations across BLs leads to fully opened MW for 0.16 μ m² bitcells, whatever the operating voltage down to 2.5V (**Fig. 14b**). From 16kbit test structures with different capacitor areas, a 280fF median C_{BL} value is extracted, assuming $\epsilon_{HfO_2:Si}=30$ and $2.P_R=35\mu C/cm^2$ extracted from stand-alone 1T-1C located on the same die (**Fig. 2a**). **Fig. 15** proposes an extrapolation of 1T-1C HfO₂:Si FeRAM scaling capability based on actual ferroelectric performance: C_{BL} scaling tends to improve MW and appears necessary for accompanying the reduction of capacitor area while preserving memory performance. Thus, advanced technological nodes providing lower access capacitance per BL are expected to drastically improve MW and/or allow aggressive capacitor scaling. From ΔV_{REF} , one may derive the median ferroelectric switching energy here calculated as $E=2.P_R.S.V_{prog}=\Delta V_{REF,0\sigma}.(C_D+C_{BL}).V_{prog}$, with $\epsilon_{HfO_2:Si}=30$ and $C_{BL}=280$ fF (**Fig. 15**). An energy lower than 100fJ/bit is demonstrated at low voltage operation on 0.16 μ m² capacitor area, highlighting the potential of 1T-1C FeRAM technology for ultra low-power application with capacitor area and programming voltage scaling (**Fig. 16**). **Table 1** summarizes the main results obtained so far on HfO₂-based FeRAM arrays including this work.

CONCLUSION AND PERSPECTIVES

For the first time, 16kbit FeRAM arrays with 10nm HfO₂:Si-based ferroelectric capacitor are reported with capacitor area ranging from 0.36 μ m² down to 0.16 μ m². Switching kinetics have been investigated and 4ns writing capability is demonstrated. Endurance performance up to 10^7 is reported on a full 16kbit array. Resistance to threefold solder reflows is demonstrated for the first time on HfO₂-based FeRAM arrays together with data retention up to 125°C after 10^4 s. Specific design improvement for further scaling and more advanced nodes is presented and sub-10mV/ σ state distribution slopes are expected.

ACKNOWLEDGMENT

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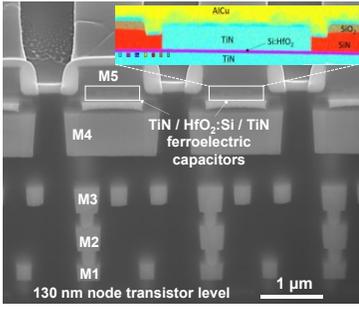


Fig. 1: Scanning Transmission Electron Microscope (STEM) cross-section image of TiN/HfO₂:Si/TiN ferroelectric capacitors integrated within 1T-1C 16kbit array between M4 and M5 of 130nm CMOS, with inset, energy dispersive X-ray (EDX) cross-section image of a 0.55µm diameter capacitor.

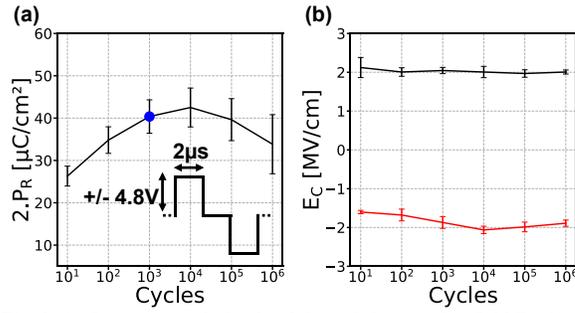


Fig. 2: (a) Remanent polarization $2.P_R$ and (b) coercive field E_C along cycling measured on 1T-1C structures cycled with square electrical pulses (4.8V 2µs) to mimic the electrical signal waveform used for 16kbit array characterization. $2.P_R$ is extracted using PUND methodology (4.8V 10kHz) and the mean value on 5 dies tested in this paper is extracted. The blue dot represents the median $2.P_R$ considered in the 16kbit arrays, *i.e.* after 1000 cycles 4.8V 2µs.

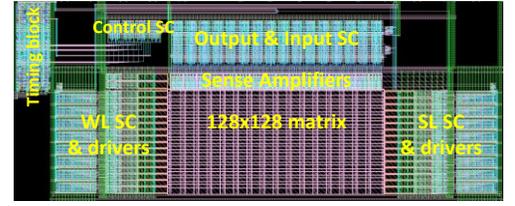


Fig. 3: Layout view of the 16kbit FeRAM array with the different digital blocks, including the control block handling the pulse generators and the sense amplifier block.

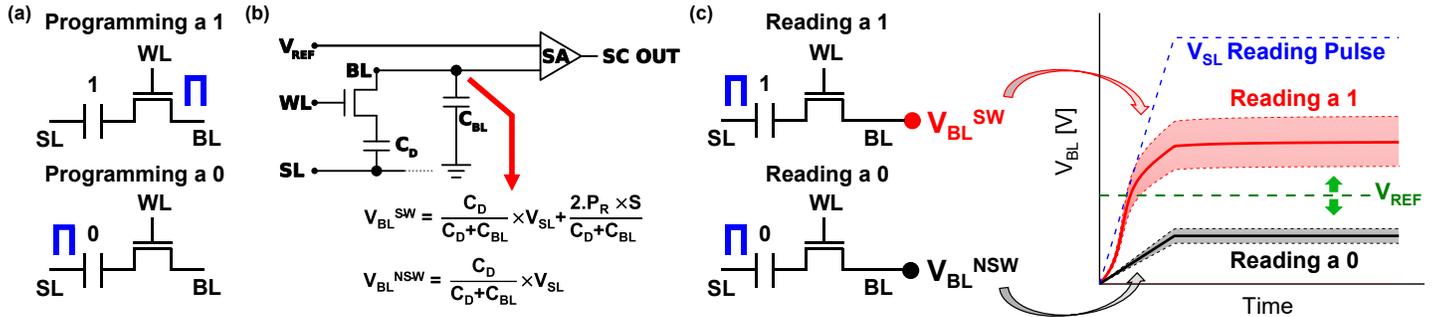


Fig. 4: (a) Schematic of the 1T-1C bitcell's programming operations where either the SL or the BL is positively pulsed. (b) Schematic of the 1T-1C architecture with the FeRAM array with V_{BL} equations depending on the ferroelectric switching behavior of the capacitor during the read operation, *i.e.* Non Switching (NSW) and Switching (SW), corresponding to reading a 0 and a 1, respectively. C_D , C_{BL} and V_{SL} denote 1C capacitance, BL capacitance and SL voltage, respectively. (c) Read operations where only SL pulses are used and V_{BL} voltages according to the equations of (b), where a variability on $2.P_R$ and ϵ_r is introduced to emulate bitcell variability at the 16kbit array level. The green dashed-line represents the optimum V_{REF} position leading to a correct Read operation.

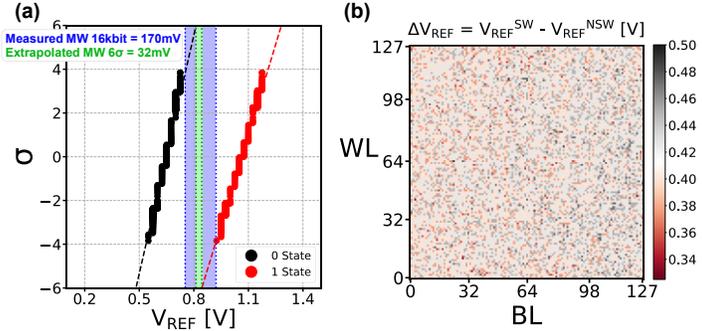


Fig. 5: (a) 0 and 1 state distributions measured on 16kbit array with 0.36µm² TiN/HfO₂:Si/TiN capacitors using 25mV incremental V_{REF} steps and 4.8V 2µs programming and read pulses. (b) 128x128 bitmap of ΔV_{REF} , *i.e.* the bitcell-wise Memory Window.

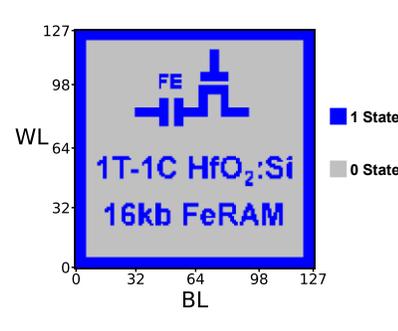


Fig. 6: Programmed and read pattern using 4.8V 2µs pulses and a fixed V_{REF} of 0.85V demonstrating no bit failure and correct addressing of the whole 16kbit 1T-1C array (0.36µm² TiN/HfO₂:Si/TiN capacitors).

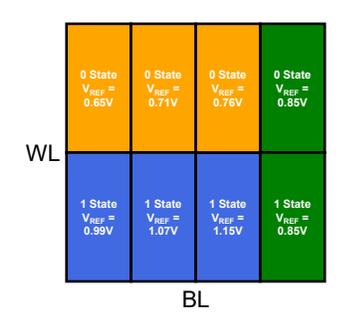


Fig. 7: Simplified schematic of the repartition of V_{REF} values for data retention evaluation of both 0 and 1 states. In practice, the different regions have been scrambled over the array in order not to be impacted by location effects.

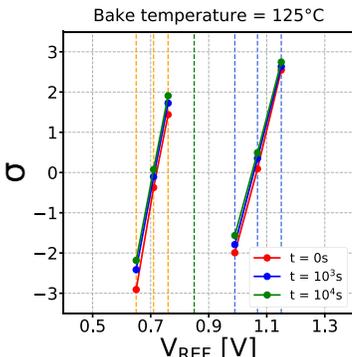


Fig. 8: Drift of 0 and 1 states partial distributions along Data Retention test at 125°C. The dashed-lines represent the V_{REF} repartition presented in Fig. 7.

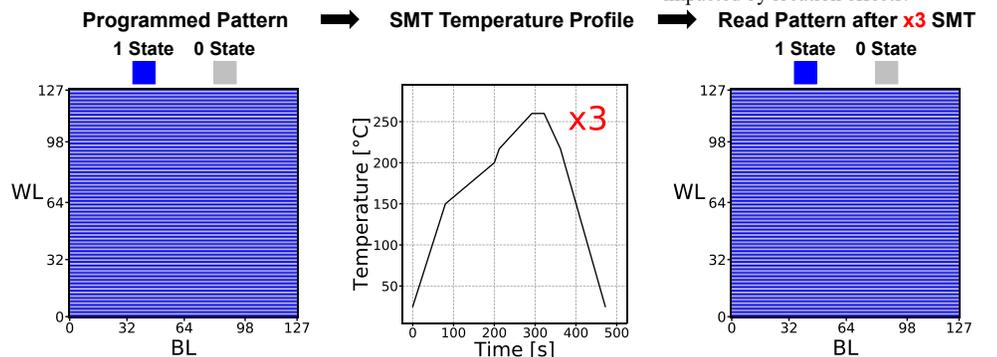


Fig. 9: Programmed (left) and read (right) patterns on 16kb array with 0.36µm² TiN/HfO₂:Si/TiN capacitors (V_{REF} =0.85V) demonstrating no bit failure after 3 successive SMT temperature stresses (max. 260°C 30s).

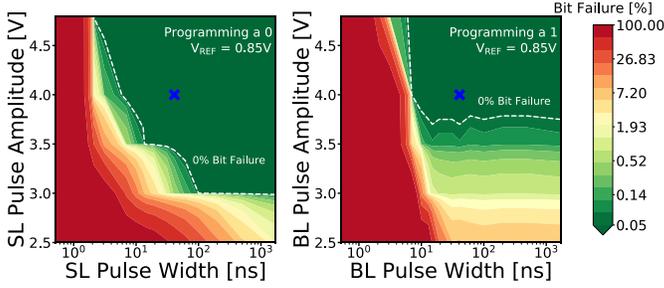


Fig. 10: Evaluation of the switching efficiency of programming 0 and 1 pulses at various voltages and pulse widths down to sub-ns pulses using internal Pulse Generators. A 4.8V 2 μ s pre-set pulse of opposite state is applied prior to the characterized pulse. A fixed V_{REF} of 0.85V is used for all pulses. The blue cross highlights the pulse considered for endurance evaluation.

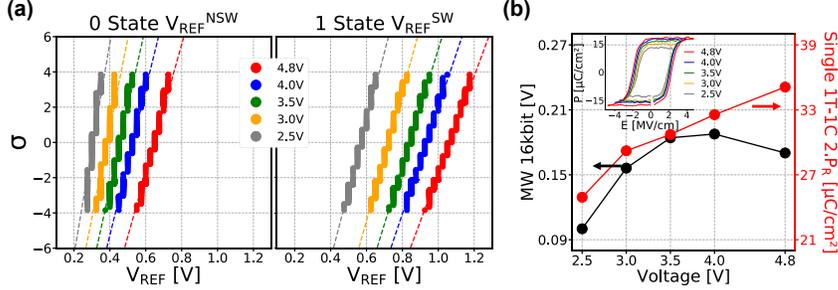


Fig. 12: (a) Distributions of 0 and 1 states measured on a 16kbit array when varying programming and read pulse amplitude from 4.8V down to 2.5V at constant 2 μ s pulse width (0.36 μ m² TiN/HfO₂/Si/TiN capacitors). (b) Memory Window at 16kbit scale as a function of programming/reading voltage compared with 2.P_R after wake-up measured on a stand-alone 1T-1C capacitor.

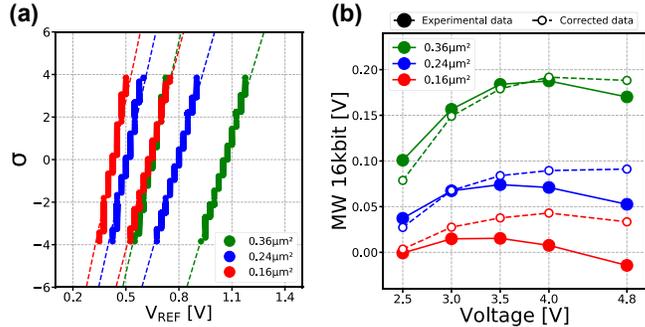


Fig. 14: (a) Distributions of the 0 and 1 states measured on 16kbit arrays for 3 capacitor areas, down to 0.16 μ m² at 4.8V and (b) corresponding 16kbit-scale MW after C_{BL} correction when varying programming and read pulse amplitude from 4.8V down to 2.5V at constant 2 μ s pulse width.

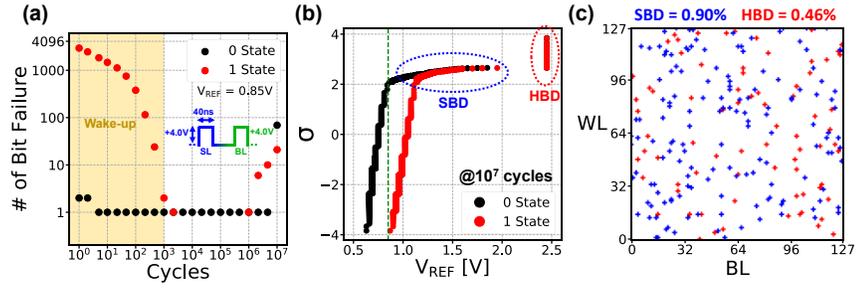


Fig. 11: (a) Endurance of the 16kbit array with a cycling pulse of 4.0V 40ns, as depicted in inset, measured with a read pulse of 4.8V 2 μ s at a fixed V_{REF} =0.85V. (b) Corresponding distributions after 10⁷ cycles, where the devices in Hard Breakdown (HBD), i.e. $V_{REF}^{SW} - V_{REF}^{NSW} = 0V$, and the Soft Breakdown (SBD) devices ($V_{REF}^{NSW} > 0.95V$) are highlighted respectively by the red and blue circles. (c) 16kbit array bitmap showing bitcells in a HBD and SBD state after 10⁷ cycles.

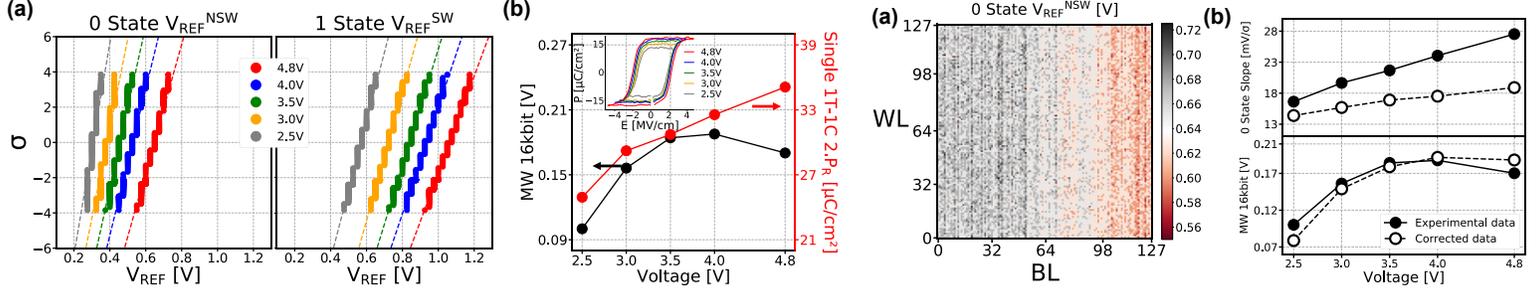


Fig. 13: (a) V_{REF}^{NSW} bitmap at 4.8V showing a gradient along BLs, attributed to a gradient of C_{BL} . (b) (top) In solid lines, 0 state experimental distribution's slope along increasing programming/read voltage amplitude and in dashed line, slopes corrected from the C_{BL} gradient. (bottom) In solid lines, experimental 16kbit MW corresponding to Fig. 12 (b) and in dashed lines, MW expected after C_{BL} gradient correction.

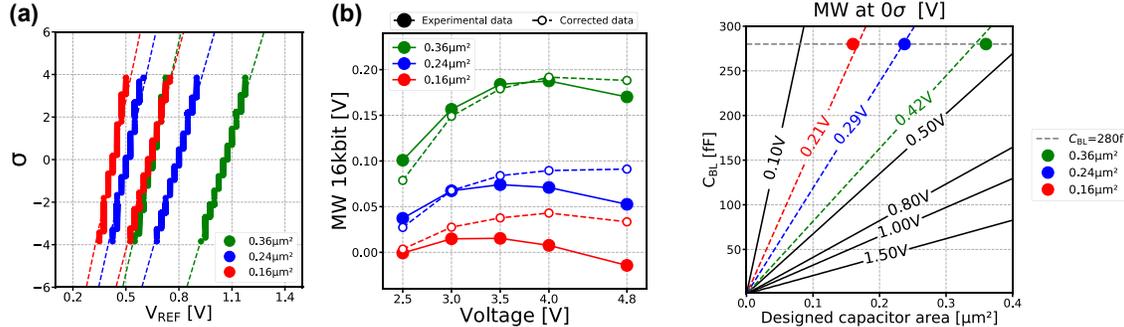


Fig. 15: Simulation of median MW (streamlines) with C_{BL} and capacitor area scaling. Horizontal dashed line indicates the actual C_{BL} achieved with 130nm technology node, and colored markers show experimental ΔV_{REF} at 0 σ .

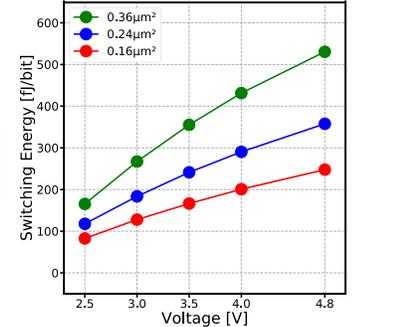


Fig. 16: Median ferroelectric switching energy per bit calculated as $E=2.P_R.S.V_{prog}=\Delta V_{REF,0\sigma}.(C_D+C_{BL}).V_{prog}$, with $\epsilon_{FeHfO_2:Si}=30$ and $C_{BL}=280fF$

Ref.	Bitcell structure / node	FeRAM array size	Ferroelectric material / Thickness	Capacitor integration / Thermal budget	Minimum Write voltage	Write speed	Endurance at array level	Retention at array level	Solder reflow compat.
[4]	1T-1C 130nm	64kbit	Hf _{0.5} Zr _{0.5} O ₂ 10nm	MOL (M1) > 500°C	2.5V	14ns at 2.5V (one state)	-	-	-
[5]	1T-1C 130nm	64kbit	Hf _{0.5} Zr _{0.5} O ₂ 8nm	MOL (M1) > 500°C	2.0V	16ns at 2.0V (one state)	> 10 ¹⁵ cycles at 2V (extrapol.)	-	-
this work	1T-1C 130nm	16kbit	Si implanted HfO ₂ 10nm	BEOL (M4-M5) < 500°C	2.5V	4ns at 4.8V (both states)	10 ⁷ cycles at 4V 40ns (meas.)	125°C during 10 ⁴ s with no bitfail	Yes (3x SMT with no bitfail)

Table 1: Summary of results obtained at array level on HfO₂-based FeRAM kbit arrays.

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