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***Abstract*—16kbit 1T-1C FeRAM arrays are demonstrated at 130nm node with TiN/HfO_2:Si/TiN ferroelectric capacitors integrated in the Back-End-of-Line (BEOL). 0 state and 1 state distributions measured on the arrays demonstrate perfect yield at 4.8V operation, with extrapolations suggesting memory window is still open at 6 sigma statistics. Programming speed down to 4ns at 4V is highlighted at the array level, together with endurance up to 10^7 cycles. Promising data retention up to 10^4s at 125°C is measured on the arrays and, for the first time, solder reflow compatibility is demonstrated for HfO_2-based FeRAM. Memory window on 16kbit arrays remains open down to 2.5V programming voltage and when capacitor area decreases from 0.36µm² down to 0.16µm², with calculated programming energy lower than 100fJ/bit. These results pave the way to competitive ultra-low power embedded non-volatile memories at more advanced nodes.**

***Index Terms*—16kbit array, ferroelectric random-access memory (FeRAM), 130-nm technology node, HfO_2:Si, hafnium oxide, solder reflow, data retention, endurance, emerging memory, nonvolatile memory (NVM), ferroelectric memories.**

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I. Introduction

SINCE 2011 [1], ferroelectric HfO_2 is paving the way towards the next generation of ferroelectric non-volatile memory devices for high endurance and ultra-low power applications. Recently, TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN [2] and TiN/HfO_2:Si/TiN [3] ferroelectric capacitors were successfully integrated in the Back-End-Of-Line (BEOL) of 130nm CMOS technology, demonstrating their scalability and compatibility with low thermal budgets. Functional FeRAM arrays were reported for the first time by Okuno et al [4], [5], in which the $Hf_{0.5}Zr_{0.5}O_2$-based capacitor (1C) of the bitcell is integrated in the Middle-Of-Line (MOL) on the contact of the transistor (1T), prior to BEOL process. This integration approach allows crystallization anneal higher than 500°C to be used [5]. In this paper, 16kbit 1T-1C FeRAM arrays with BEOL integrated HfO_2:Si-based ferroelectric capacitors are designed and demonstrated for the first time. First, state distributions at the array level are measured through specific methodology accounting for the destructive reading nature of FeRAM. Then, data retention at 125°C and solder reflow immunity are assessed. Programming kinetics and endurance are analyzed depending on the reading parameters, their dynamic being discussed according to the analog stand-alone capacitor characterization. Finally, operation towards low voltages and capacitor scaling potential are studied, foreshadowing performance towards more advanced technological nodes.

II. 1T-1C FERAM ARRAY INTEGRATION AT 130NM NODE

A. Ferroelectric 16kbit arrays fabrication

TiN/HfO_2:Si(10nm)/TiN capacitors with designed areas of 0.36µm², 0.24µm² and 0.16µm² have been integrated in the BEOL of 130nm CMOS technology between Metal 4 and Metal 5 lines (Fig. 1) [3]. The HfO_2 film was deposited by atomic layer deposition in an ASM Polygon Pulsar chamber at 300°C with $HfCl_4$ and H_2O as precursors. The oxide film was then Silicon-doped by ion implantation, targeting a 1% Si mean concentration, as formerly reported [6]. TiN electrodes have been deposited by physical vapor deposition at 350°C and the

resulting stack was further etched to define the capacitors diameter. Capacitors were then encapsulated by SiN and SiO_2 deposited at 400°C, followed by a planarization step prior to via opening and M5 deposition at 450°C.

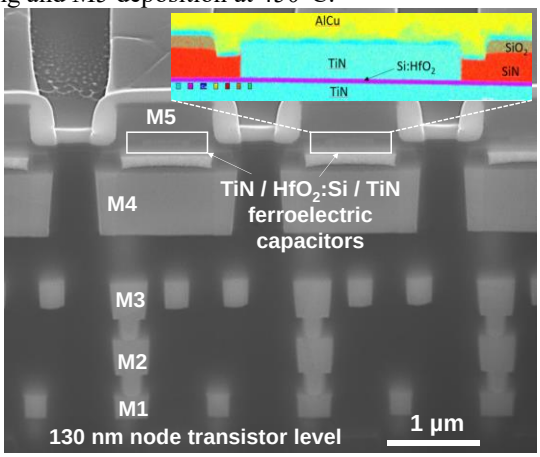

Figure 1: Scanning Transmission Electron Microscope (STEM) cross-section image of TiN/HfO_2:Si/TiN ferroelectric capacitors integrated within 1T-1C 16kbit array between M4 and M5 of 130nm CMOS, with inset, energy dispersive X-ray (EDX) cross-section image of a 0.55µm diameter capacitor.

B. Ferroelectric characterization of 1T-1C structures

Various test structures have been designed, from single bitcell with one capacitor connected to the drain of a transistor (1T-1C), up to 16kbit 1T-1C arrays. Stand-alone 1T-1C structures have been electrically measured at wafer level with Positive-Up-Negative-Down (PUND) technique (4.8V 10kHz) [7] along square-shaped cycling (4.8V 2µs), in order to mimic the electrical signal waveform used for the latter 16kbit arrays (Fig. 2).

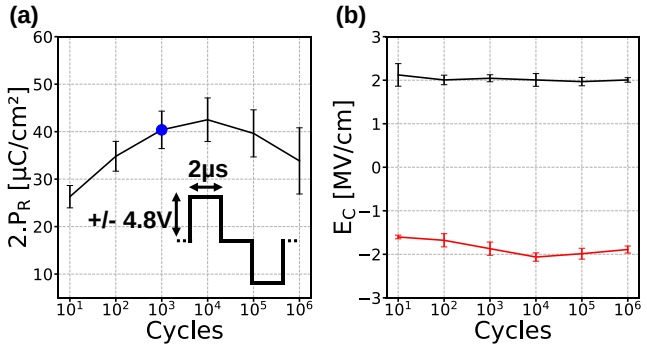

Figure 2: (a) Remanent polarization $2.P_R$ and (b) coercive field E_C along cycling measured on 1T-1C structures cycled with square electrical pulses (4.8V 2µs). The mean value on 5 dies tested in this paper is extracted. The blue dot represents the median $2.P_R$ considered in the 16kbit arrays on the same wafer, i.e. after 1000 cycles 4.8V 2µs.

Remanent polarization ($2.P_R$) shows the expected wake-up, stable and fatigue phases of HfO_2-based ferroelectric capacitors. The evolutions of $2.P_R$ through cycling have been thoroughly studied in literature and represent a challenge for HfO_2-based memory arrays, as later presented. Several mechanisms are proposed in the literature. A first possibility is a field-cycling-induced phase transitions from monoclinic [8]–[10] or [11] tetragonal phase to orthorhombic ferroelectric phase. Another one states that an interfacial "dead" layer, hindering ferroelectric switching through electric field local modifications, vanishes along field cycling [10], [12], [13]. Finally, the most studied mechanism proposes in-homogenously distributed charges, *e.g.* oxygen vacancies, inducing a built-in electric field pinning ferroelectric domains, that redistribute through electrical cycling [9], [13]–[16].

The maximum $2.P_R$ value of 40µC/cm² measured (Fig. 2 (a)) appears to be at the state-of-the-art for HfO_2-based ferroelectric materials, even compared to $Hf_{0.5}Zr_{0.5}O_2$ which is among the most used and most ferroelectric of the HfO_2-based layers [17]. Extracted coercive fields below 2MV/cm (Fig. 2 (b)) promise low voltage operation, as discussed later on. In the following, and unless specified, 16kbit array reported data have been measured after an initial wake-up operation of 1000 cycles using a 4.8V 2µs square signal.

III. 1T-1C FeRAM ARRAY WORKING PRINCIPLE AND CIRCUIT FEATURES

The 128x128 16kbit array features Scan Chains for bitcell addressing and circuit control, Pulse Generators for tuning pulse widths over more than 3 decades, capacitive bitcell reading via Sense Amplifiers and Write-Back capability after destructive read operations. 1T-1C programming operations and conventions are summarized in Fig. 3: ferroelectric 0 and 1 states are defined as bitcell states after pulsing Source Line (SL) and Bit Line (BL), respectively.

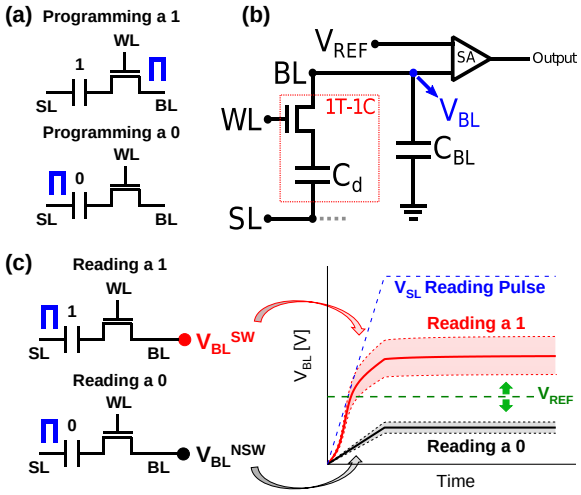

Figure 3: (a) Schematic of the 1T-1C bitcell's programming operations where either the SL or the BL is positively pulsed. (b) Schematic of the 1T-1C architecture within the FeRAM array. (c) Read operations where only SL pulses are used and V_{BL} voltages representation according to equations (1).

Subsequent read operations consist in an attempt to program a 0 state via SL pulsing, with floating BL potential: depending on the capacitor ferroelectric state (0 or 1), BL potential elevates, following charge sharing between the 1C capacitance C_d and the BL capacitance C_{BL}, at either V_{BL}^{NSW} (no ferroelectric switch, *i.e.* pure dielectric response) or V_{BL}^{SW} (dielectric response with an additional contribution of switched ferroelectric charge). These potentials can be calculated according to the schematic of Fig. 3b as:

$$V_{BL}^{NSW} = \frac{C_d}{C_d + C_{BL}} \times V_{SL}$$
$$V_{BL}^{SW} = \frac{C_d}{C_d + C_{BL}} \times V_{SL} + \frac{2.P_R \times A}{C_d + C_{BL}} \quad (1)$$

Where V_{SL} and A denote the SL voltage and the ferroelectric capacitor's area, respectively. Fig. 3c is the simulation of the

V_{BL} behavior calculated with the equations (1) during a read operation, where a variability on $2.P_R$ and ε_r is introduced to emulate bitcell variability at the 16kbit array level. V_{BL} is then compared to an a priori fixed reference potential V_{REF} with one Sense Amplifier (SA) per BL (Fig. 3c), denoted by the green dashed-line representing the optimum V_{REF} position leading to a correct Read operation. Digital SA outputs are stored in a buffer prior to data reading.

IV. 16KBIT 1T-1C FERAM ARRAY PERFORMANCE

A. *States distributions and Memory Window*

The distribution of 0 state (and 1 state respectively) has been extracted by alternating several programming 0 (and 1 respectively) and read operations with 4.8V 2µs pulses. The procedure is as follows: the bitcells are first programmed in either the 0 (respectively 1) state. Then, a first read operation is performed, starting with a low V_{REF} value. As V_{REF} is low, $V_{REF} < V_{BL}^{NSW}$ (respectively $V_{REF} < V_{BL}^{SW}$), hence the SA output is 1 in any case for the first read and therefore none of the bitcells falls in the 0 population. Subsequently, the bitcells are re-programmed at 0 (respectively 1) and read again, but with a slightly higher V_{REF}. This operation is repeated, with incrementing V_{REF} values, counting the bitcells within the array falling into the 0 (or 1) population for each V_{REF}, until $V_{REF} > V_{BL}^{NSW}$ (or $V_{REF} > V_{BL}^{SW}$), *i.e.* until the SA output is 0 for every bitcell in the array.

Both states are found to follow normal distributions and a fully opened 170mV Memory Window (MW) is demonstrated at 16kbit-scale with 0.36 µm² integrated capacitors, without any bit failure (Fig. 4). Extrapolating towards higher statistics demonstrates MW still opened at 6σ=32mV, suggesting potential for Gbit-size arrays.

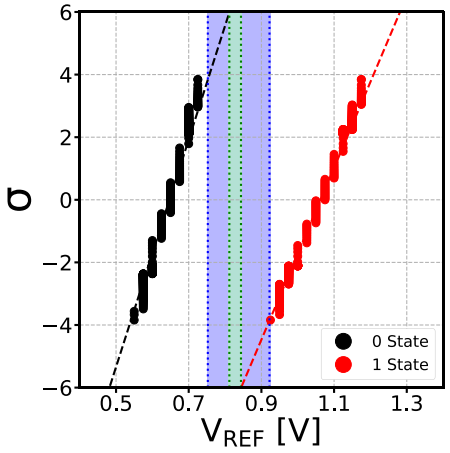

Figure 4: 0 and 1 state distributions measured on 16kbit array with 0.36µm² TiN/HfO_2:Si/TiN capacitors using 25mV incremental V_{REF} steps and 4.8V 2µs programming and read pulses. The blue box corresponds to the MW at the 16kbit-scale while the green one stands for the 6σ extrapolation.

The 0 state distribution is found sharper than the 1 state one which can be understood through equation (1): while the dispersion of V_{BL}^{NSW} is only driven by the variability of the HfO_2's dielectric parameters inside the array, V_{BL}^{SW} accounts, in addition, for the dispersion of the ferroelectric polarization. Fig. 3 (c) directly illustrates such difference.

The difference $\Delta V_{BL}=V_{BL}^{SW}- V_{BL}^{NSW}$ on each independent bitcells isolates the contribution of pure ferroelectric switching and is found homogeneously distributed across the 16kbit array without design-driven variation. From measured distributions, V_{REF}=0.85V is defined for the 16kbit array digital reading operations. Using this V_{REF}, a bit failure free bitmap pattern is achieved with 4.8V 2µs operations, *cf.* Fig. 6 of [18].

B. *Time/Temperature stability assessment*

The retention of the programmed information within a memory through time and/or elevated temperature is a primordial parameter for NVM technologies [19] and appears to be one of the main weak points of HfO_2-based memories [17]. To the author's knowledge, such characterizations has never been done at the array level for HfO_2-based FeRAM. In the literature, the retention of polarization is evaluated on stand-alone capacitors through a methodology similar to the PUND characterization. It allows the extraction of 6 different analog retentions values, depending on the pulsing scheme [20]. The programming and reading schematics of Fig. 3 define the SS^+ and OS^+ (cf. Fig. 3 of [20]) as the evaluated one in this circuit.

However, the destructive nature of read operation does not allow to track directly the retention of polarization after high temperature bake. Data retention evaluation has thus been performed on a 16kbit array subdivided in 8 regions, each region being pre-programmed and baked equivalently but read with different V_{REF} values in order to assess distribution drift with temperature bake.

A nominal 0.85V V_{REF} operation shows no bit failure after a 10^4s bake at 125°C, while V_{REF} values targeting the core of t = 0s distributions show a slight distribution drift (Fig. 5). No satisfactory extrapolation up to 10 years can be provided with confidence at the moment. However as the MW remains fully open after 10^4s at 125°C and a negligible distribution drift is observed, FeRAM's data retention at the array level is not found as detrimental as expected from single 1C capacitors characterizations.

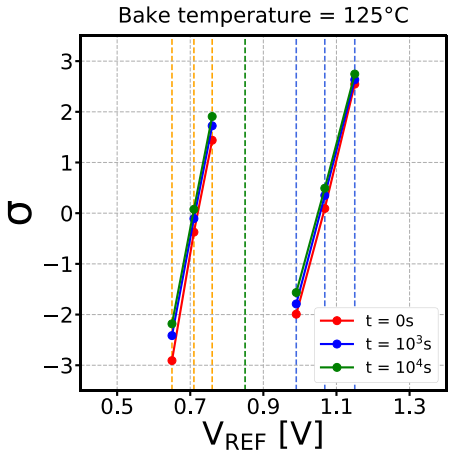

Figure 5: Drift of 0 and 1 states partial distributions along Data Retention test at 125°C. The dashed-lines represent the V_{REF} repartition, the 8 different regions being scrambled over the array in order not to be impacted by location effects.

Promising data retention is confirmed by the demonstration of HfO_2:Si FeRAM immunity to solder reflow. A pattern pre-programmed at 4.8V 2µs on the 16kbit array is found able to withstand three successive Surface Mount Technology (SMT) temperature stresses (max temperature of 260°C for 30s), without any bit failure for both memory states, *cf.* Fig. 9 of [18].

C. *Programming kinetics of the 16kbit array*

Internal Pulse Generators (PG) allow to probe the 1T-1C FeRAM switching kinetics from 1.7µs down to 520ps. From 0 and 1 states pre-programmed at 4.8V 2µs, various pulse widths and amplitudes have been applied to the entire 16kbit array and bit failures are here reported for bitcells not capable to overcome V_{REF}=0.85V (Fig. 6).

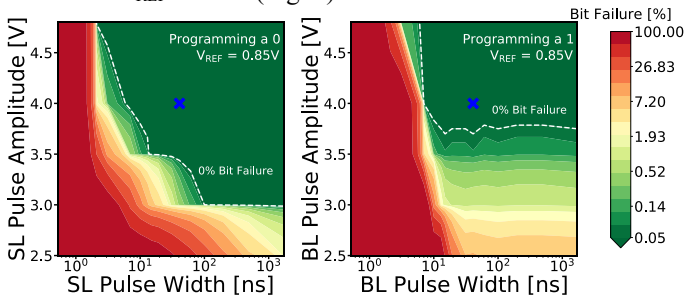

Figure 6: Evaluation of the bit programming failure of 0 and 1 states at various voltages and pulse widths down to sub-ns pulses using internal Pulse Generators. A 4.8V 2µs pre-set pulse of opposite state is applied prior to the characterized pulse. A fixed V_{REF} of 0.85V is used for all pulses. The blue cross highlights the pulse considered for endurance evaluation.

For the first time, a constant V_{REF} sensing offer a realistic vision of both states programming kinetics. Programming capability at 4ns is demonstrated at 4V for both states (Fig. 6). Based on this voltage-time trade-off investigation performed at the 16kbit array level, a 40ns 4V pulse is defined for the endurance evaluation reported in section IV D.

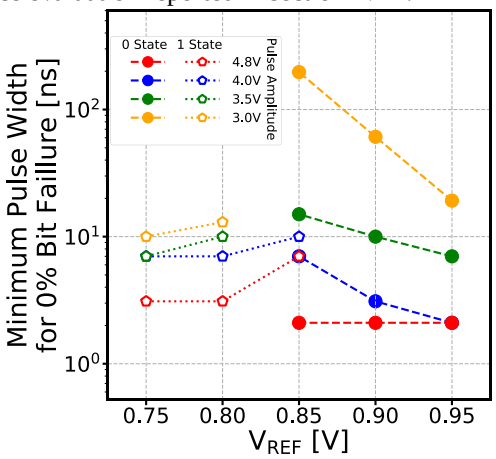

Figure 7: Minimum pulse width required to avoid any bit failure depending on the V_{REF}, at several programming pulse amplitude.

Evaluation using other V_{REF} values has been found to improve sensitivity to fast pulses for one state while being detrimental for the other one. Figure 7 shows the minimum programming pulse width, *i.e.* SL pulses and BL pulses for 0 state and 1 state respectively, leading to a bit failure free read operation depending on the reference voltage V_{REF}. While decreasing V_{REF} allows the use of shorter pulses for the 1 state, the opposite effect is observed for the 0 state. The minimum pulse width can decrease of up to a decade for a 100mV V_{REF} decrease at 3.0V pulse amplitude. Hence, for FeRAM technologies based on Sense Amplifiers for the reading opereations, programming kinetics have to be carefully measured at specified V_{REF}. In our case, V_{REF} = 0.85V chosen regarding the distributions of Fig. 4 appears to be the optimum reference voltage for all tested parameters.

The used methodology does not allow measuring the intrinsic switching kinetics of ferroelectric domains as only a fraction of switched domains could lead to a correct read operation depending on the used V_{REF}. However, no matter which pulse amplitude or which V_{REF} used, 520ps programming pulses have not lead to any correct subsequent reading. In the meantime, with 1.1ns programming pulses, *i.e.* the second shortest pulse used in this work, several correct reads have been acquired even with less favorable V_{REF} or at lower pulse amplitudes. Even though it is not possible to affirm that not a single ferroelectric domain has been switched with 520ps pulses, this observation strongly correlates with Lyu *et al.* [21] that demonstrated up to now the fastest ferroelectric switching times of 925ps with 6MV/cm pulses.

D. *Endurance performance of the 16kbit array*

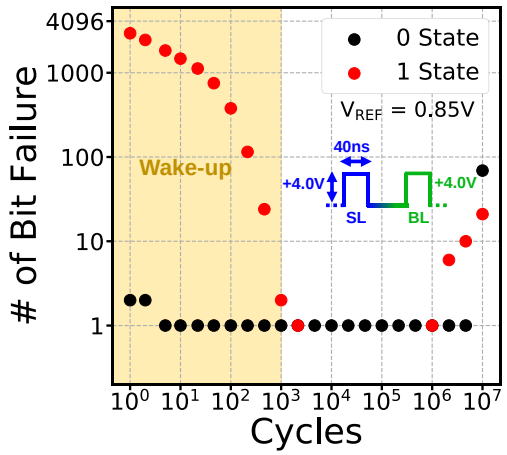

Figure 8: Endurance of the 16kbit array with a cycling pulse of 4.0V 40ns, as depicted in inset, measured with a read pulse of 4.8V 2µs at a fixed V_{REF}=0.85V.

Unlike previously reported data measured after 10^3 cycles that aimed wake up the bitcells at 4.8V 2µs pulses, endurance evaluation has been conducted at 16kbit scale without bitcell electrical preconditioning (*i.e.* starting at pristine state). Here again, an optimized V_{REF}=0.85V shows excellent 16kbit FeRAM operation during 10^7 cycles (test limit) (Fig. 8).

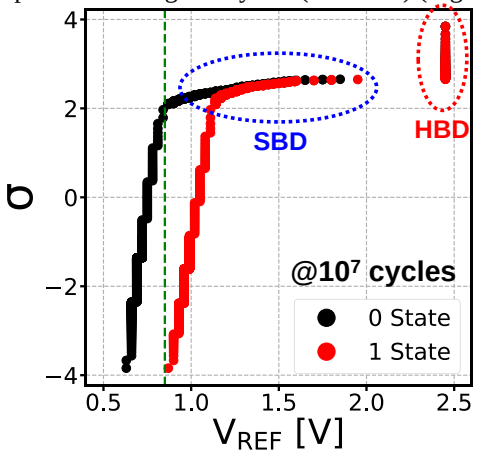

Figure 9: States distributions after 10^7 cycles 4.0V 40ns, where the devices in Hard Breakdown (HBD), i.e. $V_{REF}^{SW} - V_{REF}^{NSW}$= 0V, and the Soft Breakdown (SBD) devices (V_{REF}^{NSW} > 0.95V) are highlighted respectively by the red and blue circles.

Distributions measured after 10^7 cycles show that bit failures originate from Hard and Soft Breakdown events (0.46% and

0.90%, respectively), while ferroelectric performance is preserved as seen from $\Delta V_{REF}>0$ at 0σ (Fig. 9). No preferential spatial location for breakdown is found in post-endurance bitmaps, cf. Fig. 11 (c) of [18]. In the case of 4V device operation, dielectric reliability is thus the limiting factor for 10nm HfO_2:Si films and scaling down the operating voltage is expected to improve endurance performance [22] towards the intrinsic limits of ferroelectric fatigue. Also, previous work with similar BEOL-integration reported an increase of 3 orders of magnitude on endurance using ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ ALD deposited layer rather than HfO_2:Si doped by ion implantation [22]. Such endurance performance are expected to bridge the gap toward the 10^{15} cycling capability of commercial perovskite-based memories.

As for programming kinetics, endurance evaluation is found sensitive to the chosen V_{REF}. Fig 10 depicts the endurance performance of a single 16kbit array sub-divided in 4 V_{REF}. As expected, increasing V_{REF} benefits the 0 State readings, *e.g.* no bitfails are measured at V_{REF} = 0.9V up to the last 10^7 point, while deteriorating the 1 State readings. While the wake-up behavior poorly affects the 0 State, mostly seen with V_{REF} = 0.75V and 0.8V, it has an important impact on the 1 State.

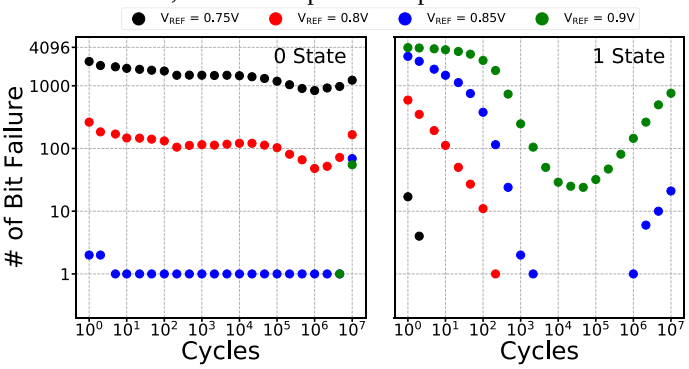

Figure 10: Endurance of the 16kbit array with a cycling pulse of 4.0V 40ns measured with a read pulse of 4.8V 2µs at 4 different V_{REF} values.

The decrease of the 1 state bit failure up to $10^4/10^5$ cycles is explained by the ferroelectric wake-up, where the ferroelectric switching charges will increase. Indeed, the evolution along cycling of the 1 state depends on both the dielectric and the ferroelectric characteristics while only the variation of dielectric parameters can influence the 0 state. Fig. 2 (a) highlights an increase of 60% in $2.P_R$ between pristine and wake-up stage and subsequent decrease of 20% up to 10^6 cycles (test limit). It demonstrates a high variation of the ferroelectric parameters, even though the cycling pulse scheme from Fig. 2 to Fig. 10 varies, *i.e.* different polarization values and dynamics are expected [23]. In the meantime, the magnitude of evolution of dielectric variables through wake-up phenomena is expected to be of a lower value, *e.g.* the variation of permittivity with field-induced phase change [10], [11].

V. VOLTAGE AND AREA SCALING ASSESSMENT

A. *Correction of C_{BL}'s design-induced variation*

Distributions of lower voltage operations down to 2.5V, with constant 2µs-wide pulses have been measured, cf. Fig 12 (a) of [18], and corresponding MW is extracted. The 16kbit memory window remains fully open down to 2.5V operating voltages. Compared to the monotonic dependence of remanent polarization with programming voltage measured on stand-alone 1T-1C bitcell (Fig. 11), MW at the 16kbit scale is found optimal at intermediate voltage, e.g. 4V for 0.36µm² area capacitors.

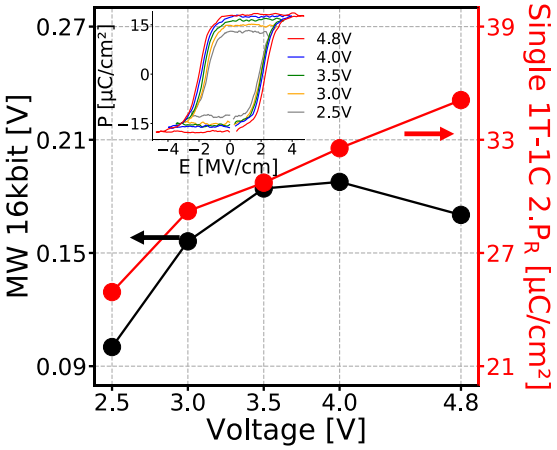

Figure 11: Memory Window at 16kbit scale as a function of programming/reading voltage from 4.8V down to 2.5V at constant 2µs pulse width (0.36µm² TiN/HfO_2:Si/TiN capacitors) compared with $2.P_R$ after wake-up measured on a stand-alone 1T-1C capacitor.

The expected reduction of MW with voltage scaling (*i.e.* less ferroelectric domains being switched) is partly compensated by improved distribution slopes, attributed to their dielectric component rather than a ferroelectric effect. The origin of 0 state slope partly lies in a gradient effect along the 128 BLs of the array, as seen in the 0 state bitmap reported in Fig. 12.

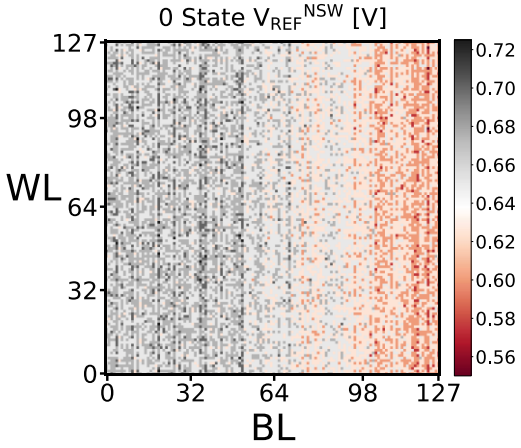

Figure 12: V_{REF}^{NSW} bitmap at 4.8V showing a gradient along BLs, attributed to a gradient of C_{BL}.

Regarding the homogeneity of ferroelectric properties within the array, this effect is attributed to BL-dependent C_{BL} values, thus a design-induced variation. 0 state dependence with BL location has been suppressed while preserving the variability within each WL in order to simulate a future design update correcting from C_{BL} variations. Fig. 13 shows an improvement of 0 state from 28mV/σ down to 19mV/σ at 4.8V and a subsequent improvement of the 4.8V MW from 170mV to 188mV (less distribution overlap).

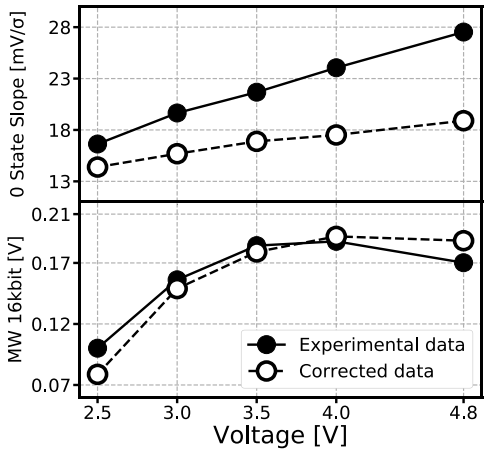

Figure 13: (top) In solid lines, 0 state experimental distribution's slope along increasing programming/read voltage amplitude and in dashed line, slopes corrected from the CBL gradient. (bottom) In solid lines, experimental 16kbit MW corresponding to Fig. 7 and in dashed lines, MW expected after CBL gradient correction.

B. Capacitor scaling and switching energy

Capacitor area scaling down to 0.16µm² is reported in Fig. 14 for various operating voltages. MW opened at 16kbit scale (no bit failure) is demonstrated for 3V operation on 0.16µm² scaled bitcells. Correcting for C_{BL} variations across BLs leads to fully opened MW for 0.16µm² bitcells, whatever the operating voltage down to 2.5V.

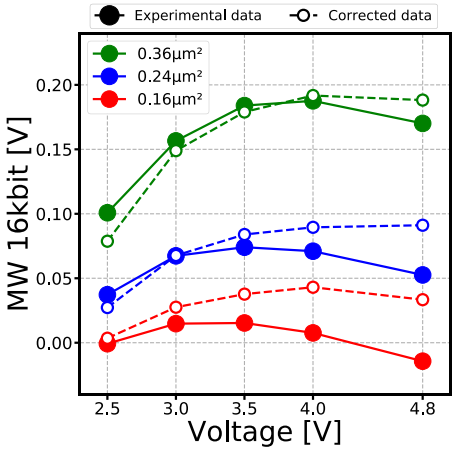

Figure 14: 16kbit-scale MW after C_{BL} correction when varying programming and read pulse amplitude from 4.8V down to 2.5V at constant 2µs pulse width measured for 3 capacitor areas, down to 0.16µm².

From 16kbit test structures with different capacitor areas, a 280fF median C_{BL} value is extracted, assuming $\varepsilon r_{HfO_2:Si}$=30 and $2.P_R$=35µC/cm² extracted from stand-alone 1T-1C located on the same die. Fig. 15 proposes an extrapolation of 1T-1C HfO_2:Si FeRAM scaling capability based on actual ferroelectric performance: lowering C_{BL} tends to improve MW and appears necessary for accompanying the reduction of capacitor area while preserving memory performance. Thus, advanced technological nodes providing lower access capacitance per BL are expected to drastically improve MW and/or allow aggressive capacitor scaling.

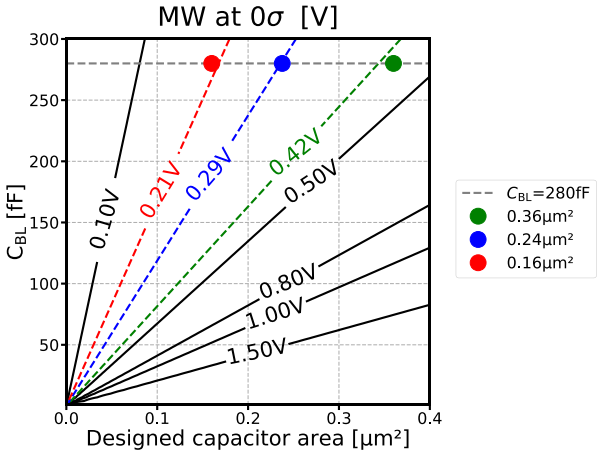

Figure 15: Simulation of median MW (streamlines) with C_{BL} and capacitor area scaling. Horizontal dashed line indicates the actual C_{BL} achieved with 130nm technology node, and colored markers show experimental ΔV_{REF} at 0σ.

From ΔV_{REF}, one may derive the median ferroelectric switching energy here calculated as:

$$E = 2.P_R \times A \times V_{prog} = \Delta V_{REF,0\sigma} \times (C_d + C_{BL}) \times V_{prog} \quad (2)$$

With $\varepsilon r_{HfO_2:Si}$=30 and C_{BL}=280fF, an energy lower than 100fJ/bit is demonstrated at low voltage operation on 0.16µm² capacitor area, highlighting the potential of 1T-1C FeRAM technology for ultra low-power application at more advanced nodes (Fig. 16).

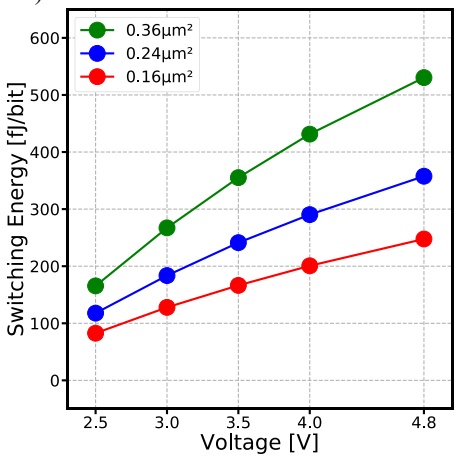

Figure 16: Median ferroelectric switching energy per bit calculated with equation (2), using $\varepsilon r_{HfO_2:Si}$=30 and C_{BL}=280fF.

VI. CONCLUSION AND PERSPECTIVES

For the first time, 16kbit BEOL-integrated FeRAM arrays with 10nm HfO_2:Si-based ferroelectric capacitor are reported. 0.36µm² capacitor area-based 1T-1C arrays demonstrate a memory window of 170mV, extrapolated to 32mV for Gbit-size arrays, at 4.8V 2µs operating voltages. Programming kinetics have thereafter been investigated and 4ns writing capability is demonstrated for programming voltage of 4V. Endurance performance up to 10^7 is reported on a full 16kbit array with 40ns 4V programming pulses and the wake-up/fatigue phases of ferroelectric materials are highlighted through V_{REF} tuning. Resistance to threefold solder reflows is demonstrated for the first time on HfO_2-based FeRAM arrays together with data retention up to 125°C after 10^4s. Influence of operation voltages on state distributions is measured for 3 capacitor areas, down to

0.16µm². Subsequently, design-induced variability correction leads to 16kbit memory window fully opened even for 0.16µm² capacitor area upon 2.5V operation voltages. Specific design improvement for further scaling and more advanced nodes is presented and sub-10mV/σ state distribution slopes are expected.

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