



HAL
open science

Hot Electron Source Side Injection Comprehension in 40nm eSTM™

Franck Melul, Thibault Kempf, Vincenzo Della Marca, Marc Bocquet, Madjid Akbal, Frederique Trenteseaux, Marc Mantelli, Arnaud Regnier, Stephan Niel, Francesco Rosa

► **To cite this version:**

Franck Melul, Thibault Kempf, Vincenzo Della Marca, Marc Bocquet, Madjid Akbal, et al.. Hot Electron Source Side Injection Comprehension in 40nm eSTM™. 2021 IEEE International Memory Workshop (IMW), May 2021, Dresden, France. pp.1-4, 10.1109/IMW51353.2021.9439613 . hal-03596898

HAL Id: hal-03596898

<https://hal.science/hal-03596898v1>

Submitted on 4 Mar 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Hot Electron Source Side Injection Comprehension in 40nm eSTMTM

Franck MELUL^{*†}, Thibault KEMPF[†], Vincenzo DELLA MARCA^{*}, Marc BOCQUET^{*}, Madjid AKBAL[†], Frederique TRENTSEAU[†], Marc MANTELLI[†], Arnaud REGNIER[†],

Stephan NIEL[‡] and Francesco LA ROSA[†]

^{*}Aix-Marseille University, CNRS, IM2NP UMR 7334, F-13397 Marseille, France

[†]STMicroelectronics, 190 Avenue Celestin Coq, 13106, Rousset, France

[‡]STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France

Abstract—In this paper, we detail an experimental study of the hot electron Source Side Injection programming operation of the embedded Select in Trench Memory (eSTMTM) cell. A complete set of electrical characterizations is carried out. A focus on the Select Gate bias to improve the programming window and the consumption is reported. Moreover, the impact of the Sense-to-Select distance, on the memory behavior is highlighted. These characteristics give us the keys to find the best trade-off to program this cell. Finally, the optimized programming scheme is used to show the endurance up to 500k cycles, while the programming current is monitored. We report an energy consumption decrease during the cycling thanks to the Source Side Injection mechanism. This makes the eSTMTM cell suitable for low-power and scalable embedded applications.

I. INTRODUCTION

The embedded Select in Trench Memory (eSTMTM) has been presented as a 40nm split-gate cell with a vertical Select transistor. This 1.5T NVM cell has been developed to optimize costs, area and performances [1]. Nowadays, the need for low consumption embedded scaled applications is increasing and drives the development of charge storage memory cell [2]. As the programming is the more consuming operation, this paper presents a detailed analysis of the specific Source Side Injection programming of eSTMTM and its consumption [3]. The absence of over erase and the programming window centered around 0V to avoid read disturb make the eSTMTM a serious candidate to address the 40nm floating gate based cell market [4]. Finally, we show in this paper the endurance performances. The 33% of the initial programming window is preserved after 500k cycles with a decreasing of hot electron Source Side Injection consumption energy during the cell aging. This enables the eSTMTM for high reliability applications.

II. SAMPLES DESCRIPTION

A. eSTMTM Cell Architecture

In Fig. 1a, the schematic and an eSTMTM transmission electron microscopy (TEM) picture are shown. Two neighbor memory bits share the same Select Trench transistor, left or right memory point (Sense) selection is done using the associated Drain contact. The Trench transistor (Select) enables us

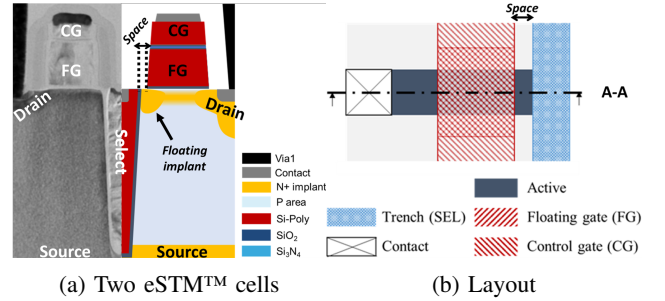


Fig. 1: TEM cut, sketch and layout of the eSTMTM cell.

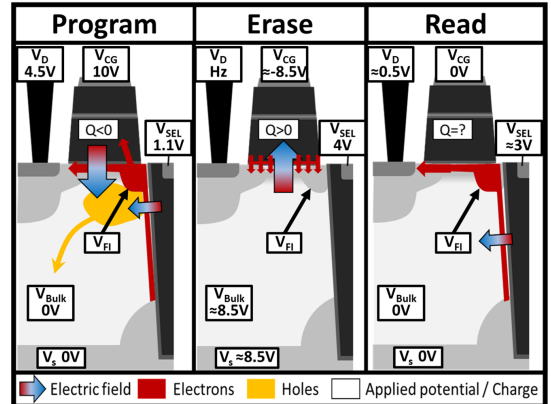


Fig. 2: eSTMTM Electrical activation.

to control consumption and leakage in this 1.5T architecture with the possibility to scale the global structure. The Fig. 1b shows the top view layout of the eSTMTM cell. As explained below, the Sense-to-Select distance, referred as Space, plays a fundamental role in the programming efficiency.

B. Cell Operations

Fig. 2 schematizes the different electrical operations. The erasing is performed by a Fowler-Nordheim (FN) tunneling [5] and the programming is based on Hot Electron Source-Side Injection (SSI) [6]. Hot carriers are generated in the Select Trench channel flowing in a direction almost parallel to the vertical electric field in the tunnel oxide enabling an

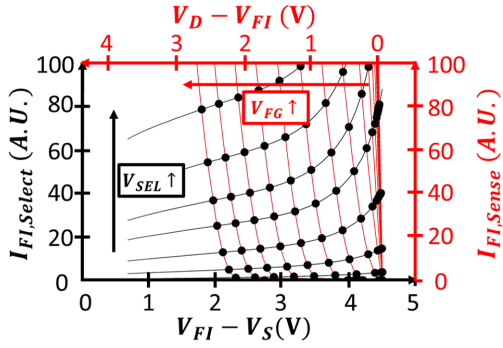


Fig. 3: Quasi-static characteristics of the single Sense and the single Select allowing the extraction of V_{FI} for $V_D = 4.5V$.

efficient injection. The edge between the Sense and the Select is characterized by the presence of a floating LDD implant, called "Floating Implant". Its potential, noted V_{FI} has an important impact on the creation of hot carriers and the injection efficiency [7]. Therefore the determination of this potential is essential for understanding the injection mechanisms.

III. HOT ELECTRON SOURCE SIDE INJECTION STUDY

A. V_{FI} measurement method

To extract the V_{FI} potential as a function of the Select Gate voltage (V_{SEL}) and Floating Gate potential (V_{FG}), we performed a complete set of current/voltage characteristics on a single vertical Trench transistor (without the Sense) and on an single equivalent Sense transistor (without the Select) where the Floating Gate and the Control Gate are shorted. In Fig. 3, the black lines represent the results of the single Select Floating Implant current $I_{FI,Select} = fct(V_{FI} - V_S)$. In addition, the $I_{FI,Sense} = fct(V_D - V_{FI})$ characteristics of the equivalent single Sense are also carried out (Fig. 3 red lines). These characteristics are realized using a Drain voltage (V_D) of 4.5V and a Source voltage V_S of 0V.

Hence, the V_{FI} potential can be extracted as a function of V_{SEL} and V_{FG} considering the continuity of the current through the Floating Implant between the Sense and the Select,

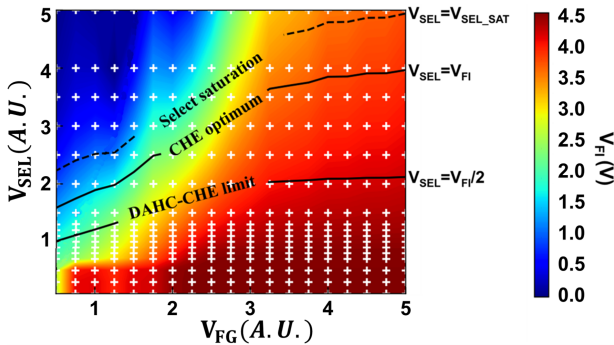
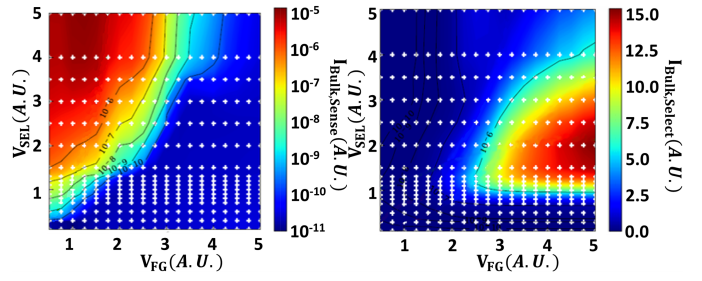


Fig. 4: V_{FI} map as a function of V_{SEL} and V_{FG} . Black isolines refers to the single Select Trench only transistor main theoretical current states.



(a) Bulk current of Sense Transistor. (b) Bulk current of Select Transistor.

Fig. 5: Bulk current map in the range of V_{SEL} and V_{FG}

$I_{FI,Sense} = I_{FI,Select}$, (Fig. 4). White crosses represent all the measurements conditions addressed. Black isolines refer to the single Select main theoretical current states: saturation, Channel Hot Electron (CHE) and Drain Avalanche Hot Carrier (DAHC) [8].

Based on the previous quasi-static study, it is possible to extract the different currents as a function of the eSTM™ programming electrical conditions, especially Bulk current of single Sense ($I_{Bulk,Sense}$) and single Select ($I_{Bulk,Select}$) which is a marker of hot carrier generation [7] as reported in Fig. 5. At low V_{SEL} , the Select Transistor is off and zero current flows to the Bulk. At high V_{SEL} and relatively low V_{FG} (but enough to enable a current flowing), the Select transistor is in his linear state and the Sense channel is pinched-off. The horizontal electric field generating the hot carriers is then localised under the Sense transistor close to the Drain. Thus, $I_{Bulk,Sense}$ is such higher than $I_{Bulk,Select}$ (Fig. 5a).

At a really high V_{FG} (used to inject hot electrons in the Floating Gate), the Sense channel is less resistive than the Select one. The Drain potential moves to the Floating Implant, transferring the pinch-off region to the Select channel. Hot electrons are thus generated by the Select transistor (Fig. 5b) and, due to the high V_{FG} , injected into the Floating Gate.

The Sense Gate current allows a finer analysis of charge injection in the Floating Gate. The Fig. 6 highlights that the optimized injection is obtained when the Select transistor is in its linear mode. The measurements have been realized

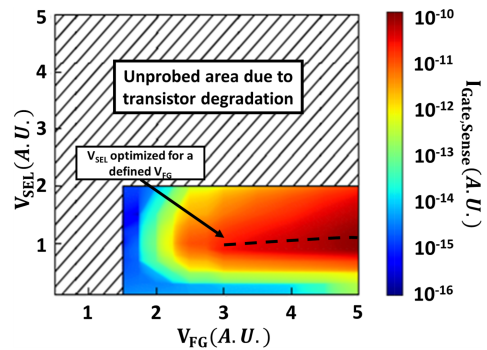


Fig. 6: Map of measured Sense Gate current on a 2048 parallel memory array.

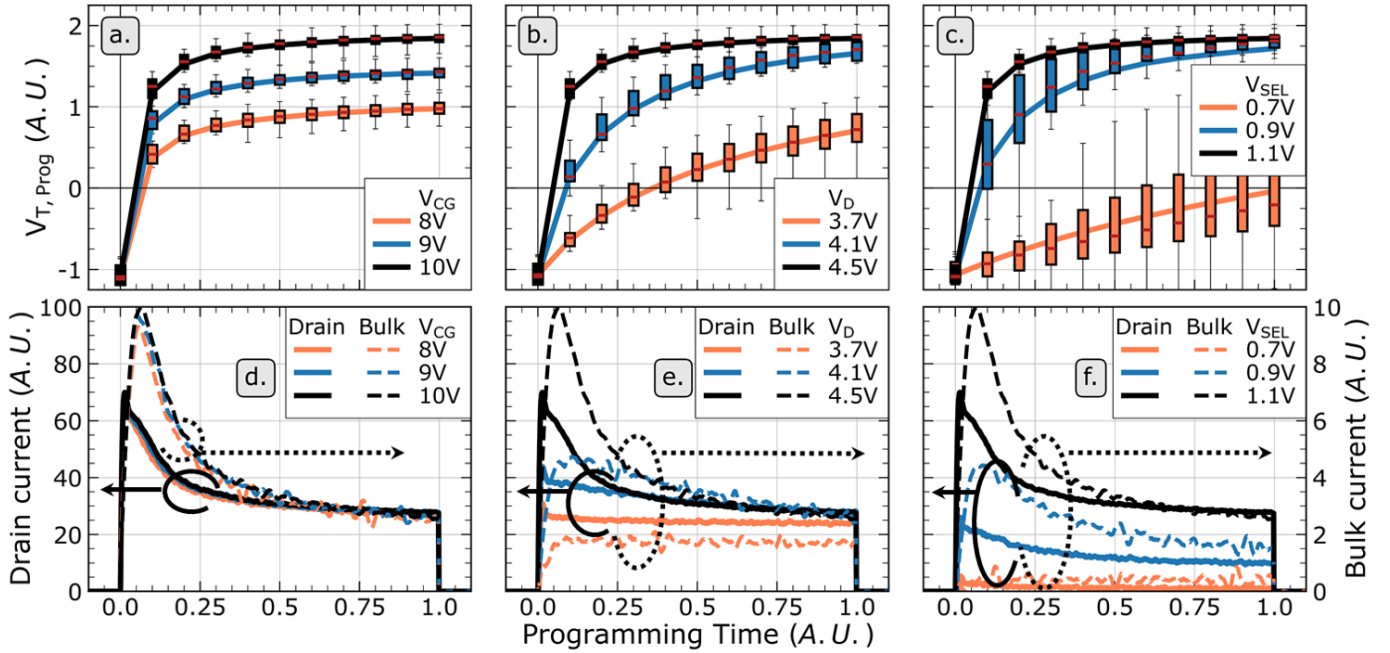


Fig. 7: Impact of the 4 freedom degrees (V_{CG} , V_D , V_{SEL} , $Time$) on programming kinetics (resp. a., b. and c.) and Drain and Bulk mean consumption currents associated (resp. d., e. and f.). Black curves correspond to standard programming with $V_{CG} = 10V$, $V_D = 4.5V$, $V_{SEL} = 1.1V$. Boxplot and mean current curves are based on 10 samples.

on a 2048 parallel memory array. The higher V_{FG} is, the higher the injection current is. In the next section, we will present dynamic characteristics of the programming operation to corroborate these results.

B. Programming conditions optimization

Fig. 7 shows the impact of the 4 freedom degrees (V_{CG} , V_D , V_{SEL} , $Time$) on the threshold voltage and consumption currents. In this article, the threshold voltage is defined as the sense voltage V_{CG} needed to reach a fixed read current.

The more the Sense Control Gate bias increases, the more the final amount of charges in the Floating Gate increases too, reaching a higher programming threshold voltage ($V_{T,Prog}$) as shown on Fig. 7a. The hot electron injection starts at the very beginning of programming pulse. Quickly the V_{FG} and the current consumption decrease and stabilize at a constant value seen on Fig. 7d. Whatever V_{CG} , currents and thus the Floating Gate potentials achieve the same level at the end of pulse.

Higher V_D and V_{SEL} are, higher the programming injection current peaks is (Fig. 7e. and f.) making the programming operation faster (Fig. 7b. and c.). Before the pulse, the cell is erased. The consumed current is then really high. As injected charges move into the entire Floating Gate, and then, they increase the Sense threshold voltage. The fast charge injection makes the peak current really short. At the end, consumption current does not vary with V_D .

The same observations can be done for the V_{SEL} variation. The main fact is the impact of V_{SEL} on the dispersion of $V_{T,Prog}$ during programming. This spread is due to the

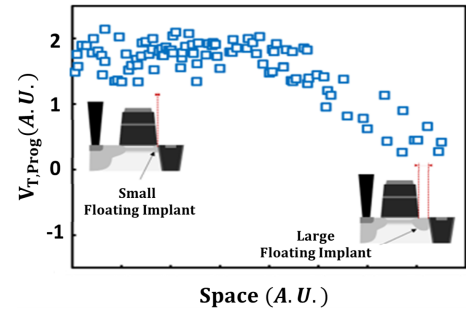


Fig. 8: Programming window for various Sense-to-Select distances for standard programming conditions.

dispersion on the cell morphology and exactly on the Sense-to-Select distance as explained in the next section (Fig. 8).

One can see in Fig. 7b., that depending on the programming window width tolerance, the programming time for standard conditions can be divided by ten making the programming energy consumption divided as much if a 80% programming window is tolerated. This programming flexibility allows the eSTM™ to address low-power market.

To conclude, on this graph, V_{CG} defines the final $V_{T,Prog}$, V_D sets the speed of the programming and V_{SEL} tunes the consumption and it is at the origin of the dispersion. Dynamic characteristics of the programming operation presented in this section corroborate static measurements introduced in previous section.

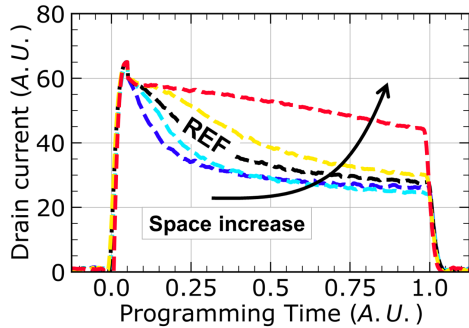


Fig. 9: Consumption versus space for standard conditions.

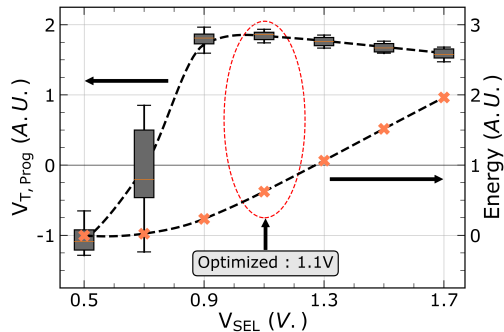


Fig. 10: Select Trench transistor bias optimization.

C. Programming dependence on Sense-to-Select distance

To study the impact of the distance between Sense and Select transistors, specific process operations and eSTM™ cell layouts have been processed to obtain different distances. Using standard conditions (see Fig. 2), the Fig. 8 enables us to affirm that a shorter space improves the programming window up to a maximum limit for a defined programming time. Besides, Fig. 9 shows the shorter the Sense-to-Select distance is the shorter the peak of Drain current during programming is. It means a faster and more efficient hot electron injection for a smaller Sense-to-Select distance. One can notice that a small extrinsic spread exists, on the space dimension, explaining why the dispersion is higher for a V_{SEL} variation (Fig. 8).

Thus, the proximity of Floating Gate with the vertical Select Trench allows the hot carriers, generated in the Select pinched-off region, to have the same direction of the vertical electric field in the tunnel oxide improving the programming efficiency. Moreover, for the shortest spaces, the Floating Implant is reduced and is less and less an obstacle for the hot electrons injection in the Floating Gate.

IV. ENDURANCE PERFORMANCES

To complete this study, endurance experiments have been performed. To optimize the programming scheme, we had to determine the best trade-off between programming window, its dispersion and the energy consumption for the eSTM™ cell. In Fig. 10, we demonstrate it is possible to find an optimized programming scheme to maximize the programming window and minimize the energy consumption with the lower possible

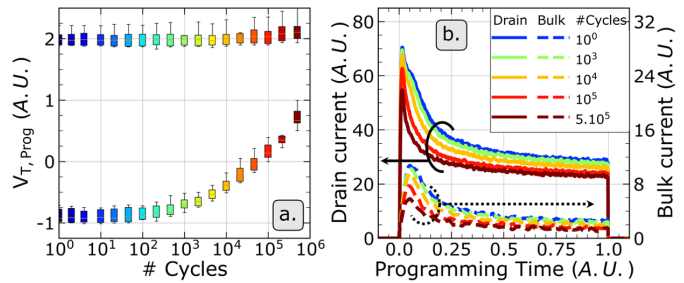


Fig. 11: Programming window (a.) and mean current consumption (b.) versus cycling. 10 samples tested.

dispersion. Regarding the endurance results (Fig. 11), 33% of the initial programming window is kept after 500k cycles [9]. It is interesting to see the low dispersion during the endurance experiments, due to the V_{SEL} optimization. The programming current decreases during the cycling [9], this is due to the Source Side Injection. Second, the current consumption decreases more and more quickly during the programming time, if the number of cycles increases. The Floating Implant, with its space charge region, masks the effect of charge trapping localization in the tunnel oxide [10] [11].

V. CONCLUSION

In this paper, the hot electron Source Side Injection programming operation of the embedded Select in Trench Memory (eSTM™) cell is investigated. Quasi-static measurements have been realized to optimize the programming scheme. Our results are supported and explained by dynamic Drain and Bulk current characterizations. A trade-off between the programming window, its standard deviation and the consumed energy is found. Different Sense-to-Select distances have been analysed corroborating that a shorter space allows to achieve a higher programming efficiency, this is suitable for the cell scaling. Finally, we demonstrate it is possible to maintain 33% of the initial programming window after 500k cycles. Moreover the energy saving is auto-improved during the cell degradation thanks to the Source Side Injection mechanism. This makes the eSTM™ memory cell a serious candidate to address low-power and high reliability applications market.

ACKNOWLEDGMENT

The authors gratefully acknowledge all manufacturing teams of STMicroelectronics for supporting this program.

REFERENCES

- [1] S. Niel et al., IEEE IEDM 2018, pp. 7.4.1-7.4.4
- [2] R. Strenz, IEEE IMW 2020, pp. 1-4
- [3] L. Masoero et al., IEEE IMW 2012, pp. 1-4
- [4] F. L. Rosa et al., IEEE 11th IMW 2019, pp. 1-4
- [5] Fowler Ralph Howard and Nordheim L. 1928, Proc. R. Soc. Lond.
- [6] M. Kamiya et al., IEEE IEDM 1982, pp. 741-744
- [7] J. Van Houdt et al., IEEE TED, vol. 39, no. 5, pp. 1150-1156 1992
- [8] Takeda, Hot-carrier effects in MOS devices. Chapter 2 1995.
- [9] V. Della Marca et al., Microelectronics Reliability, 2014, pp 2262-2265
- [10] D. Wellekens et al., IEEE TED, vol. 42, no. 11, pp. 1992-1998, 1995
- [11] V. Della Marca et al., IEEE ISCDG, 2012, pp. 65-68