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Morphology and reliability aspects of 40 nm eSTM™ architecture

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Floating Gate memory
Split-Gate memory
Endurance degradation
NVM
Reliability

Abstract

In this paper, we present an experimental study of a new architecture of the embedded Select in Trench Memory (eSTM™) cell. A first part is dedicated to a deep analysis of the overlap eSTM™ behaviour. A key fact is the possibility to achieve a large programming window thanks to tip effect enhanced erase. After the study on erase operation scheme, we demonstrate the impact of Select to Floating gate tip coupling on the endurance results. The endurance results are thus improved up to 500k cycles using the overlap eSTM™.

1. Introduction

Embedded scaled applications are increasing and push the evolvement of charge storage memory [1]. To address this topic, the embedded Select in Trench Memory (eSTM™) has been presented [2] [3]. As a 40 nm split-gate memory optimizing costs, area, and performances, the eSTM™ cell is a serious candidate to apply for low consumption and high reliability markets.

The overlap eSTM™ presented in this article is one of the architectures considered to address future scaled applications market. In a first part, this paper presents the specificities of its behaviour. A higher programming window due to a tip effect revealed by TEM cuts is reported. Impact of Select bias on read and erase operations is then realised. Finally, endurance reliability is carried out. Overlap eSTM™ has, after 500k cycles, a wider programming window than the standard one. Moreover, we studied in this paper the effect on the reliability of different erase schemes by splitting the biases between Control and Select gates. This makes the overlap eSTM™ suitable for scaled architectures and a serious candidate to address high reliability market.

2. Experimental description

2.1 Overlap eSTM

In Fig. 1, the sketch of the overlap eSTM™ cell and the associated TEM picture are presented. This cell consists in an overlap of the vertical Select transistor by the planar Sense transistor. Due to the process flow, a notch filled by Floating gate polysilicon appears at the edge between the substrate, the Select and the Floating gates. This shape, highlighted by red curve on Fig. 1, induces a tip effect in this area [4].

To realize this study, test structures with several dimensions have been fabricated. As shown on Fig. 1, "Space" refers to the Sense-to-Select distance. It is negative if the Sense transistor overlaps the Select transistor and positive if not. $L_{CHANNEL}$ is defined as the length of Sense transistor channel. All dimensions are resumed in Fig. 2

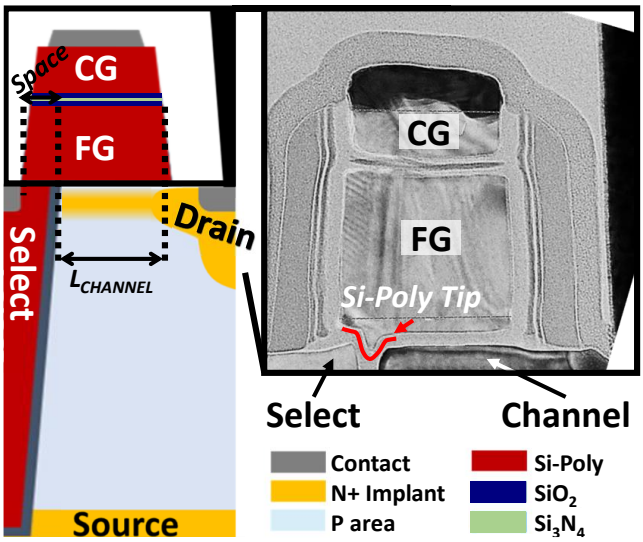

Fig. 1 Schematic of overlap eSTM™ and associated TEM picture.

This design of experiments allows us to address a large panel of dimensions and define three groups. First group, highlighted by red shape, enables us to study the impact of $L_{CHANNEL}$ at relatively fixed Space for overlap eSTM™. On the opposite, blue shape is for non-overlapped cells. Third group, green shape, is to study the impact of Space at a $L_{CHANNEL}$ close to the reference. Other dimensions were characterized, but only best results are presented here.

2.2 Standard electrical operations

The overlap eSTM™ is considered as a split gate memory programmed by Source Side Injection (SSI) [5] and erased by Fowler-Nordheim (FN). To program the cell, Control Gate (CG) is biased at 10 V (V_{CG}), drain at 4.5 V and Select gate at 1.1 V (V_{SELECT}). We consider the standard erase operation as performed with a pulse of -16 V on the CG. Finally, the threshold voltage (V_T) is read at a fixed current for a drain voltage of 0.7 V and a Select gate bias of 3.5 V.

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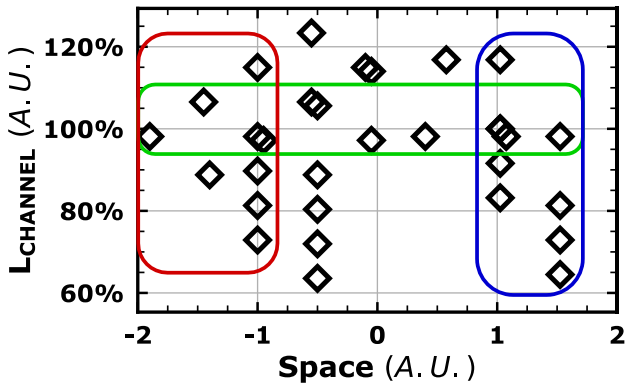

Fig. 2 Mapping of addressed dimensions. $L_{CHANNEL}$ 100% and Space 1 corresponds to the standard eSTM™.
Green shape: Study group as function of Space at fixed $L_{CHANNEL}$.
Red (respt. Blue) shape: Study group as function of $L_{CHANNEL}$ at fixed Space for overlapped (respt. non-overlapped) cells.

3. Overlap eSTM™ behaviour

All results presented in this part are obtained for standard electrical operations except when specific erase is mentioned. The threshold voltages are in arbitrary units and all are harmonised.

3.1 Programming window study

Fig. 3 represents the programming window of eSTM™ as a function of $L_{CHANNEL}$ and Space. The Space has no impact on the program threshold voltage ($V_{T,P}$). While, $L_{CHANNEL}$ has one for both cells with and without overlap. As illustrated by Fig. 4, this is only due to the variation of the threshold voltage of the equivalent Sense transistor ($V_{T,TREQ}$). This last is a memory cell where both Control and Floating gates are shorted. As for all MOSFET transistors, reducing the $L_{CHANNEL}$ induces a higher current for both cells. The threshold voltage being read at a fixed current, a higher current means a lower threshold voltage.

Concerning the erase operation, we demonstrate here that it highly benefits from the overlap. The programming window of overlap cell is two times larger than the standard one for same conditions. This over erase is explained by the tip effect described in Fig. 1 [4].

Three main paths of electrons during erase operation for an overlap eSTM™ are illustrated on Fig. 5. Path I is the classical band diagram for a Fowler-Nordheim erase on a planar MOS capacitor. This path also corresponds to the erase of the standard eSTM™. The electric field in the oxide is constant along the oxide thickness. On a P substrate, a part of the potential difference is lost in the accumulation region making the P Silicon band diagram curved. On II, the tip effect induces a localised and high electric field. It means a steeper slope on oxide band diagram and an increase of Fowler-Nordheim tunneling. Besides, tunnel oxide is slightly thinner than on I. On III, the tip effect is still present.

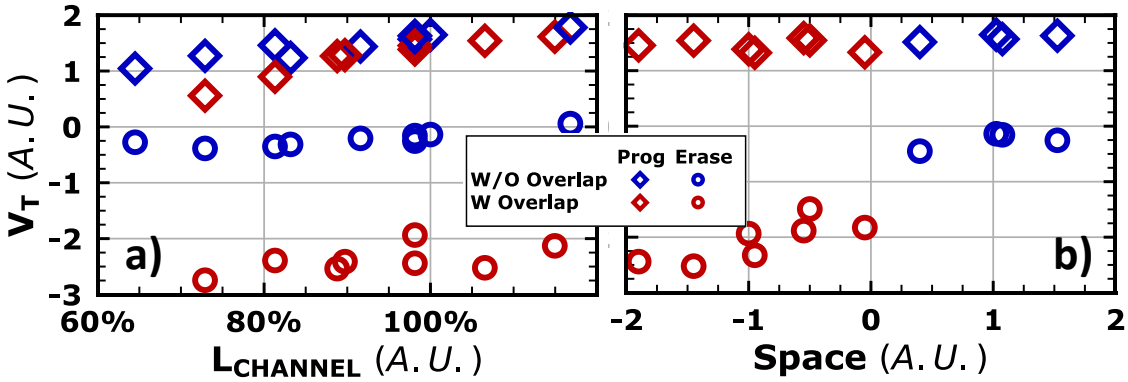

Fig. 3 Programming window versus $L_{CHANNEL}$ (a) and Space (b).
Samples on (b) correspond to green group on Fig. 2.

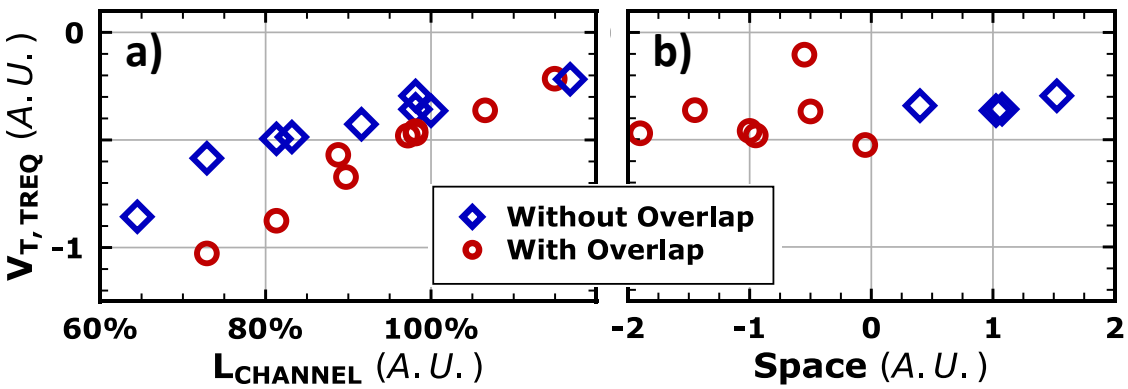

Fig. 4 Threshold voltage of equivalent transistor versus $L_{CHANNEL}$ (a) and Space (b).
Samples on (b) correspond to green group on Fig. 2.

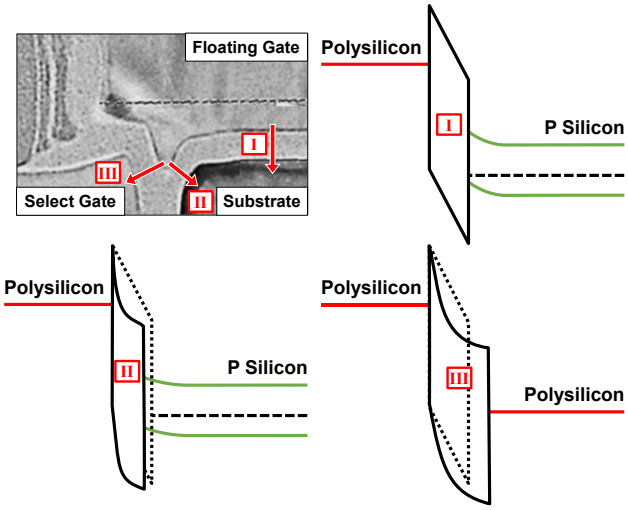

Fig. 5 Band diagram for the three main paths of electrons during erase operation.
The TEM figure is a zoom on the tip area illustrated on Fig. 1.

One can notice that even if the oxide is thicker than on I and II, the high localised electric field allows an erase using this path as it will be shown in 3.3. Especially, this path benefits from the absence of accumulation region thanks to a Polysilicon-Polysilicon erase where its high doping makes the Polysilicon acting as a metal gate.

As $L_{CHANNEL}$ has no clear impact on the programming window, we only study cells with a $L_{CHANNEL}$ close to the standard for the rest of this article. Since this specific morphology at the edge of Select and Sense transistors induces a great impact on programming window, a specific analysis of the impact of Select on read operation is needed.

3.2 Select gate impact on read operation

Fig. 6 represents the V_T obtained by read operations realised for various Select bias ($V_{SEL,\ Read}$) around the standard value defined in 2.2. These results are for a cell with a Space -2 and obtained for both program and erase states. The slope of V_T versus $V_{SEL,\ Read}$ is then calculated as well as the ratio of these two slopes. This experiment was repeated for each Space. It enables us to plot this ratio as a function of the Space on Fig. 7. For the samples with a negative Space (overlapped cells), the coupling between Select and Floating gates is increased. This attracts the stored electrons in the tip of the Floating gate inducing a gradient of surface potential in the Sense channel. This effect does not appear on erase state because the number of free charges is greatly lower.

3.3 Floating gate to Select gate split erase

As demonstrated before, the overlap eSTM™ induces a strong Floating-to-Select gates coupling. The possibility to erase with a potential difference split between the Select and the Control Gate is investigated [6]. We separated the -16 V used for the standard erase operation using: V_{CG} = -8 V and V_{SELECT} = +8 V. For the rest of this article, the standard erase will be referred as Er CG and the split method is called Er CG-SEL.

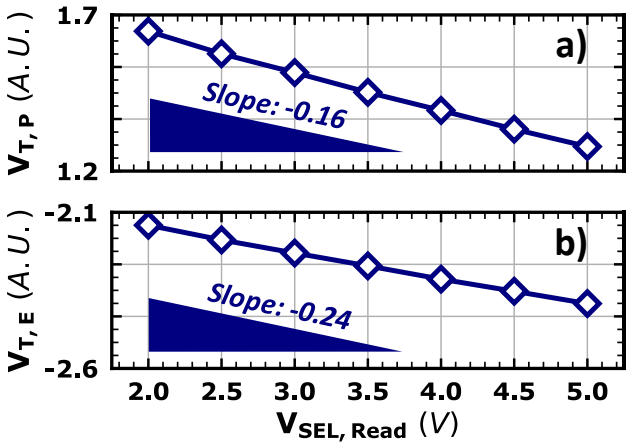

Fig. 6 Impact of Select bias on read operation for Program (a) and Erase (b) states. Overlap cell at Space -2.

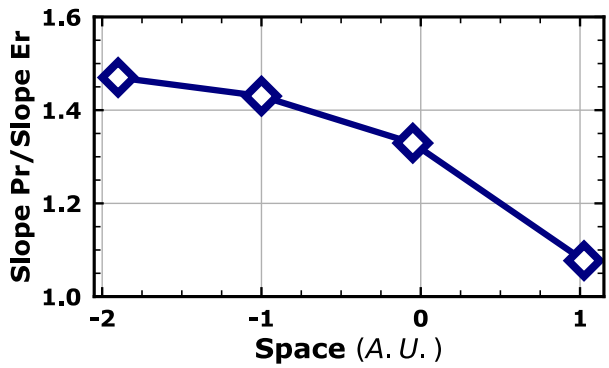

Fig. 7 Program/Erase slope ratio versus Space.

Fig. 8 represents the ratio of the Programming Window (PW) obtained after the split erase on the PW obtained after standard erase. Thus, increasing the overlap increases the erase efficiency through the Select gate. Indeed, during the erase operation for the standard cell, electrons leave Floating Gate all along the channel. In addition to this effect, the overlap eSTM™ benefits of an adding number of electrons leaving the Floating Gate at the interface between Select, Floating Gate and substrate thanks to the high electric field induced by the polysilicon tip.

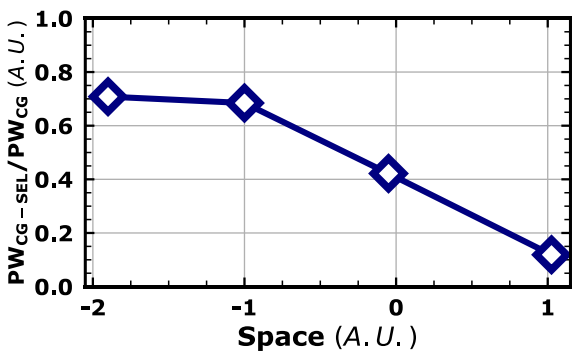

Fig. 8 Efficiency of split erase.

4. Endurance achievement

Best key criterion to study the reliability of the cell is to perform endurance experiments. eSTM^{TM} with different Space have been cycled using standard electrical operations described in 2.2. Overlap eSTM^{TM} cells have also been cycled using the split erase described in 3.3.

4.1 Programming window closure

The programming window closure is represented in Fig. 9. At the beginning of the cycling, overlap eSTM^{TM} presents a two times larger programming window than the cell with a positive Space. Moreover, with the Er CG-SEL method, it is possible to achieve 80% of the programming window obtained using the Er CG operation. It corroborates results discussed in 3.1 and 3.3.

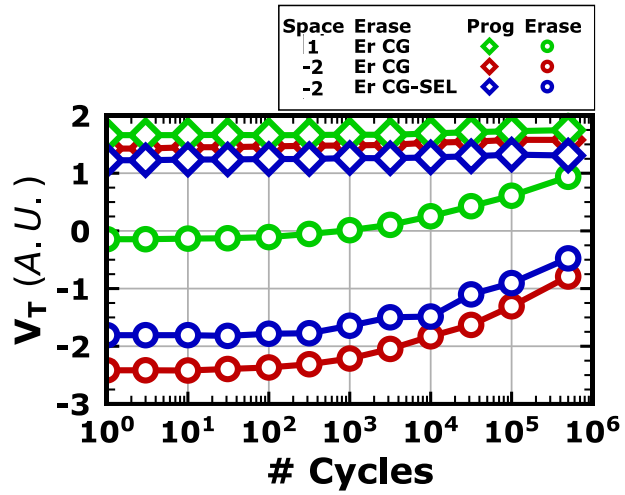

Fig. 9 Endurance for cells with different Space and erase methods.

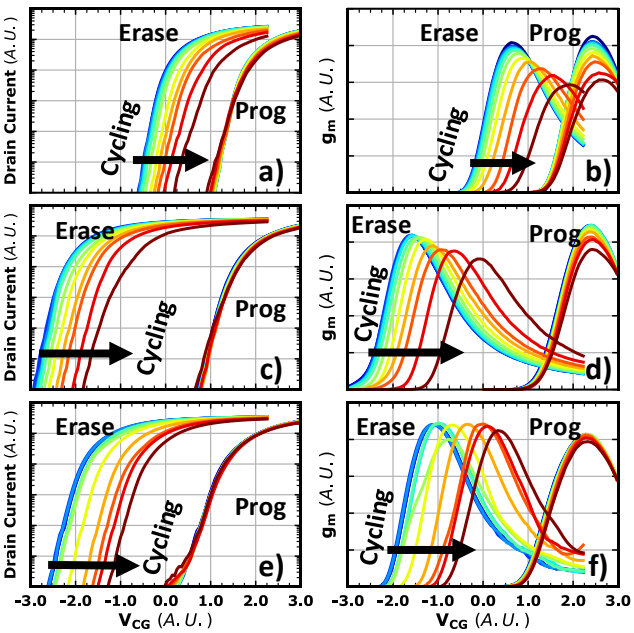

Fig. 10 Evolution of drain current (a, c, e) and transconductance (b, d, f) versus Control Gate bias for Space 1 (a ,b), and Space -2 with standard erase (c, d) and split erase (e, f).

An interesting thing is, whatever the cell or erase type, the program threshold voltage is almost constant during the cycling. Its evolution during cycling is balanced between two behaviours. First behaviour is the increase of equivalent transistor threshold voltage due to charges trapped in the oxide inducing an increase of the programming window centering [7]. Here, as the threshold voltage is read at a fixed current, it is also increase by interface traps reducing the cell gain. Second behaviour is the decrease of Source Side Injection efficiency due to interface traps and charges trapped in the bulk of oxide [8]. In these cases, behaviours quietly compensated themselves making the $V_{T,P}$ quietly stable. However, as it will be shown in next paragraphs, the equal evolution of $V_{T,P}$ for these three cycling does not mean that degradations are equal. [9]

The evolution of the erase threshold voltage is impacted, at the same time, by the increase of the Sense tunnel oxide degradation, the same as seen on program threshold voltage, and by the decrease of the Er CG efficiency. On the contrary of program threshold voltage, these two behaviours are added. It explains the high difference of threshold voltage degradation between programmed and erased state. The erase efficiency is mainly impacted by charges trapped at the Floating Gate tunnel oxide interface. This type of traps is principally generated by Fowler-Nordheim erase [10]. Whatever the cell or erase type, this degradation appears at the interface whatever if it is above the channel or at the edge between Sense and Select transistors. Thus, both curves show similar degradations on erase threshold voltage evolution during cycling. The slight lower degradation of overlap eSTM^{TM}, especially for Er CG-SEL, is explained by a drastically lower number of interface traps as explained in next subsection.

At the end of the cycling, the Space eSTM^{TM} -2 has a wider programming window after 500k cycles than the Space 1 at the beginning of the endurance. This is due to the more efficient erase operation due to the presence of Floating Gate tip. It can be transposed to the Space -2 cell erased by split erase. It shows the better endurance of overlap eSTM^{TM}.

4.2 Impact of endurance on Sense transistor characteristics

Fig. 10 represents the evolution of the main characteristics of cells during endurance. One can notice that the shape of the drain current curve for both states, cells and erase types show a weak variation during the cycling. The erase curves also suffer from a shift. It shows that the main degrading phenomenon is a charge trapping in the bulk of oxide inducing a decrease of programming efficiency and a shift of programming window centering as explained above.

However, a low decrease of transconductance (g_m) of the Sense transistor still exits making the drain current slope less steep. Since threshold voltages are read at a fixed current, it induces a low increase of program threshold voltage. One can notice that the transconductance of the sample Space -2 erased by Er CG-SEL is the less impacted by endurance degradation as seen on Fig. 10.f. Thus, for this sample, this increase of program threshold voltage is lower.

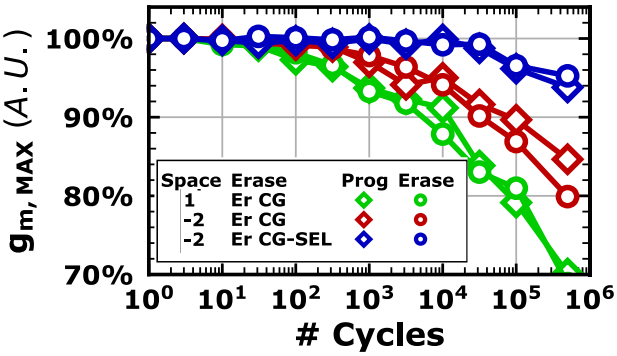

Fig. 11 Maximum of transconductance during endurance.

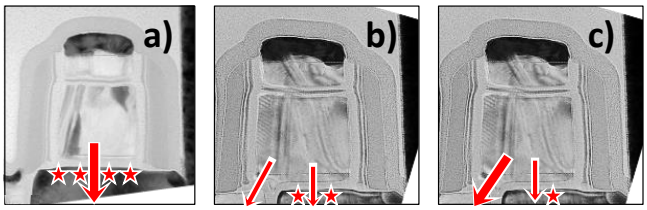

Fig. 12 Schematics of erase method and degradation for: a) Space 1 cell ER CG, b) Space -2 cell Er CG, c) Space -2 cell Er CG-SEL. Red arrow: Electrons path during erase. Red stars: Interface traps

Fig. 11 sums up the evolution of the maximum transconductance of the Sense transistor during the endurance. It clearly appears that the g_m of the Space -2 cell is less degraded. Indeed, for the standard cell, erase is made only through the tunnel oxide and causes the interface degradation in the channel inducing a decrease of the cell transconductance [11].

On the contrary, the Space -2 cell Er CG method however benefits from a partial erase through the oxide at the interface between the Select and Floating gates. This induces a lower degradation along the tunnel oxide/Sense channel interface, thus on the cell g_m. This effect is even more visible for the Space -2 cell using Er CG-SEL, the best case in this endurance analysis. Except the stress due to the V_{CG} = -8 V, the transconductance remains almost constant because of weak degradation of tunnel oxide/channel interface. These statements are summed up in Fig. 12.

4.3 Impact of endurance on Select transistor characteristics

Fig. 13 represents the evolution of main characteristics of Select transistor during endurance for both cells and erase schemes. Although the degradations in endurance are quietly negligible regarding the drain current versus V_{SELECT} characteristics, the gain of the Select of the standard eSTM^{TM} is more degraded than the other ones. One can say that only the current at high Select bias is degraded as shown in the insets of Fig. 13. It indicates an increasing of the channel resistance for both Select and Sense transistors because they are in series. Therefore, this degradation is surely only due to the Sense channel degradation described above.

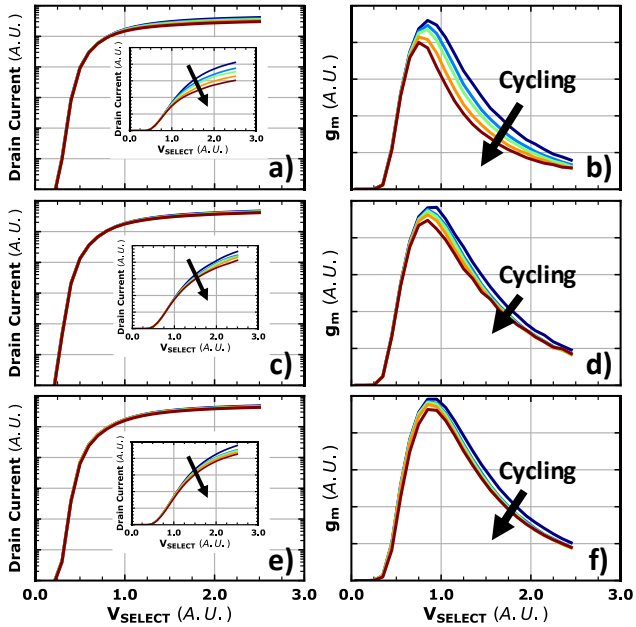

Fig. 13 Evolution of drain current (a, c, e) and g_m (b, d, f) versus Select gate bias for Space 1 cell (a, b), Space -2 cell with Er CG (c, d) and Er CG-SEL (e, f). Inset of figure a), c), e), is the drain current in linear scale.

4.4 Overlap eSTM^{TM} specific behaviour during endurance

Finally, to conclude this study, we present in Fig. 14 the evolution of program/erase slope ratio during the cycling using Er CG scheme for different Space cells (seen in 3.2) in order to show the impact of Select bias on read operation. Fig. 15 shows the variation of the split erase efficiency (seen in 3.3) during the endurance. After each cycle burst of Fig. 14, the cells are characterized using a pulse of Er CG and ER CG-SEL to verify erase method efficiency.

In these two last figures, the shape of the programming window closure during endurance test has no impact. Indeed, for each figure, data are ratio of slopes and programming windows. Thus, they do not illustrate degradations occurring along the channel. They only illustrate the evolution of Floating-to-Select gates high electrical coupling induced by the polysilicon tip.

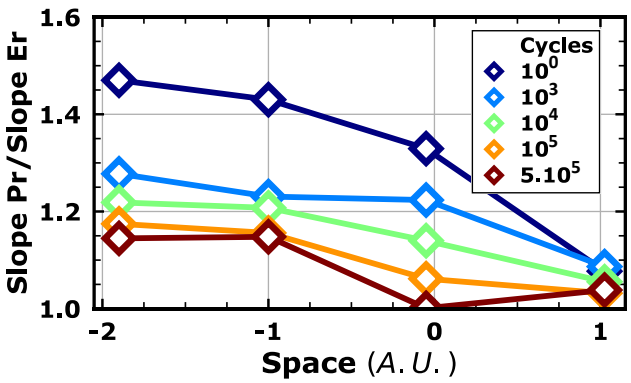

Fig. 14 Evolution during endurance of the Program/Erase slope ratio versus Space.

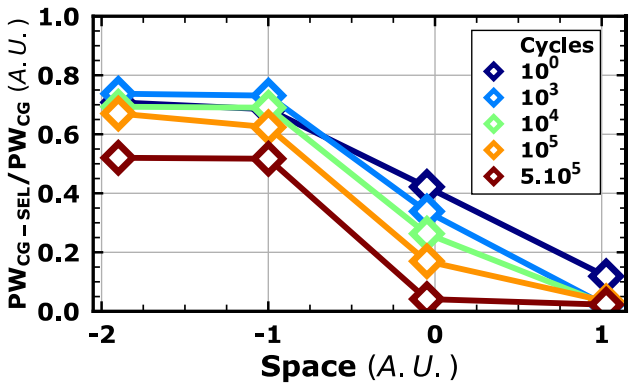

Fig. 15 Evolution during endurance of the split erase efficiency.

Specific behaviour appearing with negative space tends to disappear with cycling. Indeed, due to partial Fowler-Nordheim erase through the oxide at the interface between Floating and Select gates due to Polysilicon tip, charges are trapped there. These charges screen the electric field making the Floating gate to Select gate coupling decreases [12]. In other words, a part of charges trapped in Select-to-Floating gate oxide interface by Fowler-Nordheim erase operation induces both a decrease of erase efficiency and a reduction of the electrical specific behaviour of overlap eSTM™ during the endurance tests [13].

5. Conclusion

In this paper, an overlap eSTM™ architecture is investigated. A preliminary comparison with the standard eSTM™ for same electrical conditions showed a two times larger programming window. Specific behaviours as the impact of Select on read and erase operation of the overlap eSTM™ were demonstrated. Then, endurance results have been presented for each eSTM™ cell and for the specific split erase scheme. Whatever cycling conditions, overlap eSTM™ showed an improved programming window at 500k cycles. The Select and Sense drain current and transconductance characteristics have been presented, demonstrating that the degradations are also greatly improved thanks to the overlap eSTM™ and even more for the erase method through Select.

Acknowledgements

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