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Temperature Compensated Power Detector towards Power Consumption Optimization in 5G Devices

Issa Alaji, Etienne Okada, Daniel Gloria, Guillaume Ducournau, and Christophe Gaquière

Abstract— The design and characterization of a real-time temperature compensated power detector are presented in this article. The working frequency band of the detector is (40.5 – 42.5) GHz, dedicated to optimize power consumption in 5G devices. A novel and simple technique is proposed in this work in order to compensate the variation of the voltage sensitivity value (γ) with temperature. This technique is based on adding a passive circuit which acts as a resistor with positive temperature coefficient, which absorbs less of input power at higher temperatures. As a result, the measurements show that the degradation of sensitivity value with temperature is suppressed by more than 55%, and therefore, this value - at the frequency 41 GHz- has a small variation ($\gamma = 1530 \text{ V/W} \pm 6\%$) over the temperature range (20~100)°C. Compared to recent published works, the proposed detector circuit is quite simple with no power consumption. In addition, it is operated at higher frequencies in order to be suitable for 5G applications.

Index Terms — 55-nm BiCMOS, power detector, power consumption, temperature compensated, zero bias.

I. INTRODUCTION

POWER detectors (PDs) are considered as the key elements in wireless communication and energy harvesting systems [1]. PDs are commonly used in transmitters to optimize the power consumption and the efficiency of power amplifiers (PAs). Envelope tracking (ET), Envelope Elimination and Restoration (EER), and Average Power Tracking (APT) are the most common techniques used to enhance the efficiency of RF PAs [2-4]. PDs are also used to stabilize the gain of PAs against the effect of temperature variation, where automatic level control circuit is used [5-6]. Varying the ambient temperature of a PD leads to deviate its performance, and so, error of power measurement is produced. In this context, several techniques are proposed to design temperature compensated power detectors. The technique proposed in [7] is to add a dummy detector which is not fed by input RF power. The output of the dummy detector is used as a temperature dependent offset in order to compensate the effect of temperature variation. A PD

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circuit is proposed in [8], where the temperature effect is compensated by subtracting two temperature dependent DC currents, producing a temperature independent current. In [9], the proposed detector has a differential output structure using directional couplers; a subtractor circuit is also added to cancel the process and temperature effect. In [10], the proposed compensation circuit is based on current mirror and operational amplifier, this circuit is used as a current source for the detector.

However, the techniques mentioned above [7-10] increase the power consumption, circuit area and complexity.

In [11], it is proposed to add a temperature-sensitive voltage divider (including diode and resistors) at the detector's output. However, adding those elements can significantly increase the noise equivalent power (NEP) value.

In this article, we propose a novel technique for the design of temperature compensated power detector, in the frequency band (40.5 – 42.5) GHz, using a simple and innovative circuit, integrated in SiGe 55-nm BiCMOS technology from STMicroelectronics. The intended application of this detector is to optimize the power consumption in 5G devices using the average power tracking (APT) technique [12]. In this technique, power detector is employed to track the slow (average) variations of the envelope signal in order modulate the biasing levels of power amplifiers.

II. DETECTOR DESIGN

A. Theoretical background

The 55-nm BiCMOS technology from STMicroelectronics provides NMOS transistors with low threshold voltages. In this work, those transistors are used in diode connected configuration as zero bias diodes, and so, the exponential dependence between the voltage and current of the drain is used for square-law detection as in [12].

Increasing the temperature leads to decrease the sensitivity value (the response V/W) of the NMOS transistors in our technology; this is due to the variations in their characteristics with temperature. In order to compensate the decrease of sensitivity values with temperature (temperature effect), we

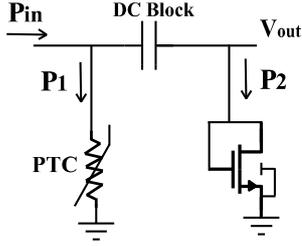


Fig. 1. Proposed temperature compensation technique by adding a PTC resistance.

propose to increase the power delivered to the NMOS with temperature. This can be established by adding a resistor with positive temperature coefficient (PTC) as illustrated in Fig. 1. As the temperature increases, the parallel PTC resistor exhibits higher resistance value, and therefore, smaller power (P_1) is absorbed. Consequently, higher power (P_2) is absorbed in the NMOS transistor, and the sensitivity value is compensated.

B. Detector design and simulation

The schematic of the proposed temperature compensated power detector is shown in Fig. 2. This schematic was designed and simulated using Cadence virtuoso. The 55-nm BiCMOS technology does not provide thermal elements, which are dedicated to change their characteristics with temperature (e.g., thermistors). A simple passive circuit (named PTC circuit) is designed in this work to act as a PTC resistor, this circuit includes the transistor (T_2), the stub (l_5) and the capacitor (C_2).

For small RF signal, the impedance of the diode connected transistor (T_2) can be represented by a channel resistance (R_{DS}) in parallel with a capacitor (C_{DS}). The inductive stub (l_5) is connected in parallel with the transistor (T_2) in order to compensate the capacitive effect of (C_{DS}) in the frequency band of interest (40.5 – 42.5) GHz. According to simulation, the R_{DS} value is decreased as increasing the temperature. Therefore, the capacitor (C_2) is added in series with the transistor (T_2) to produce the opposite behavior of (R_{DS}) over the temperature, i.e. producing a parallel resistance ($R_{PTC}=1/\text{real}(Y_{PTC})$) which increases with temperature. The designed PTC circuit has several advantages: 1) The value of the parallel real part impedance R_{PTC} increases with temperature in order to compensate the temperature effect in the frequency band (40.5 – 42.5) GHz. 2) It is isolated from the output circuit at DC and low frequencies due to the DC block capacitor (C_1), and therefore, it does not impact neither the video resistance nor the noise voltage (V_{noise} at low frequencies). 3) it can be considered as a passive circuit, and so, no biasing source is required.

The stubs (l_1 , l_2 , l_3) represent the matching network, which guaranties that the detector absorbs the maximum of input power signal. The transistor (T_1) is used as a zero bias diode, which generates a DC output voltage as a response to the input RF power (P_{in}). The capacitor C_1 is used as a DC block, this helps to avoid shorting the output DC voltage to the ground through the matching network. The polysilicon resistor (R of 15 k Ω) is used as a high impedance to avoid transmitting the input

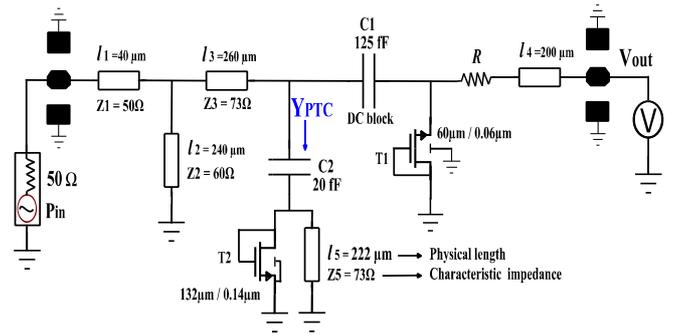


Fig. 2. Schematic of the proposed temperature compensated detector.

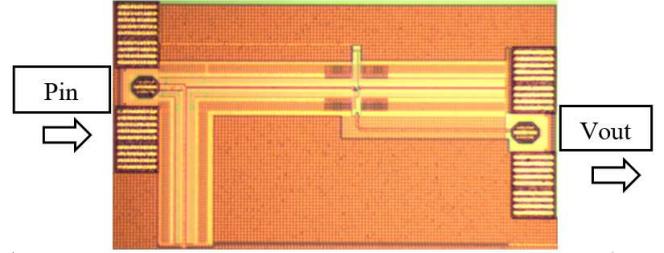


Fig. 3. Microphotograph of the detector.

RF power (P_{in}) to the output. The stub l_4 is used as an access transmission line for the output DC voltage, and therefore, its characteristics (dimensions) are not critical. It is worth to mention that all the stubs used in this design are microstrip lines, and the transistors (T_1 and T_2) are low threshold NMOS transistors.

Fig. 3 shows the detector chip microphotograph, the chip size is 0.16 mm² without the pads.

III. MEASUREMENT RESULTS

A. Measurement of the reflection coefficient

Fig. 4 shows the test bench used to measure the S_{11} parameters of the detector (in one port configuration), in the frequency band (39 - 50) GHz, and for several temperatures in the range (20 - 100) $^{\circ}$ C. This measurement was established using the PNA network analyzer N5245A (10 MHz to 50 GHz)

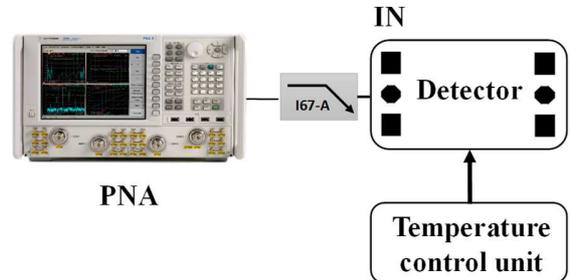


Fig. 4. Test bench used to measure the S_{11} parameters.

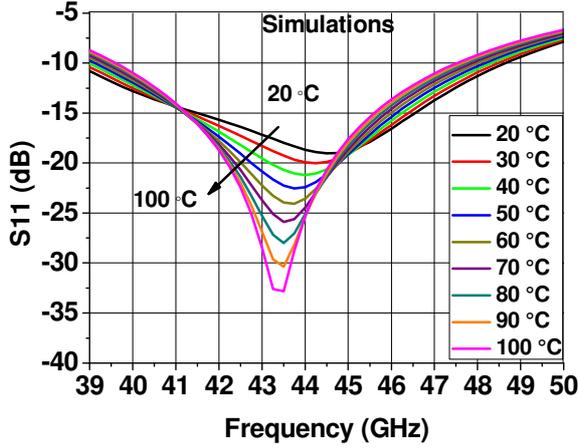


Fig. 5. Simulated S_{11} of the proposed detector for different temperatures.

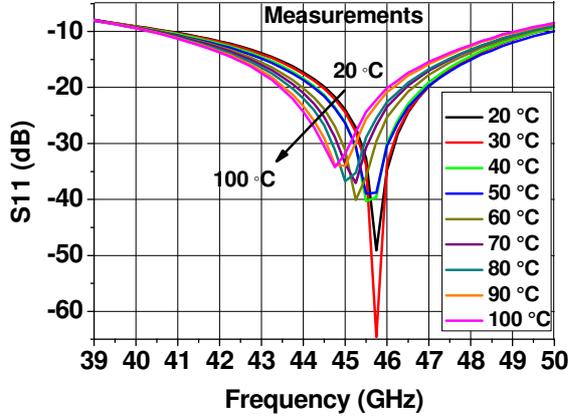


Fig. 6. Measured S_{11} of the proposed detector for different temperatures.

[13], and a PID temperature control unit which helps to vary the temperature of the detector circuit. The detector was probed at the input using a coplanar probe I67 from Infinity[14]. Figs. 5 and 6 show the simulated and measured $|S_{11}|$ of the proposed detector for several temperatures. The simulation and the measurement results show that the detector is matched in the frequency bands (39.5 - 47.5) GHz and (41 - 49) GHz respectively, for the temperature values between (20 - 100) °C, where $|S_{11}| \leq -10$ dB. It can be noticed that there are small discrepancies between the simulation and measurement results. This can be due to the model accuracy used in the simulation, and also the measurement accuracy and calibration.

B. Measurement of the PTC Circuit

The S_{11} parameters of the PTC stand-alone circuit were extracted (one port configuration) in the frequency band (39 - 46) GHz. The extracted S parameters are transferred into Y parameters, which represent Y_{PTC} . The following formula can be applied in order to extract the equivalent parallel resistance value (R_{PTC}):

$$R_{PTC} = \frac{1}{\text{real}(Y_{PTC})}$$

(1)

Figs. 7 and 8 show the simulated and measured R_{PTC} values, which are exhibited by the PTC circuit for several temperatures. Three conclusions can be mentioned based on these figures:

1) The variation ratio ($\Delta R_{PTC} / \Delta T$) in the measurement is

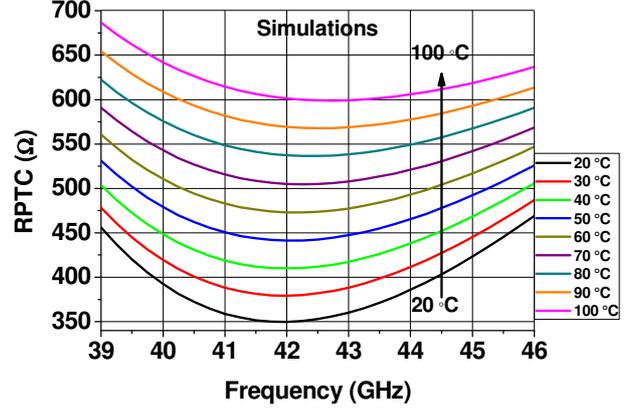


Fig. 7. Simulated R_{PTC} values for different temperatures.

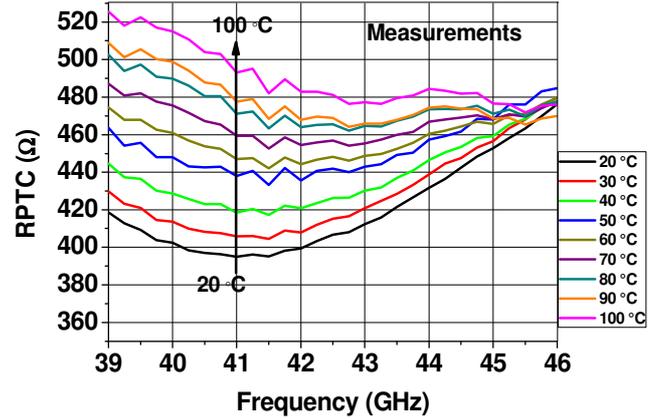


Fig. 8. Measured R_{PTC} values for different temperatures.

smaller than the simulation. For example, at 41 GHz and for $\Delta = 80^\circ\text{C}$, the simulated ΔR_{PTC} is 260 Ω , while the measured ΔR_{PTC} is 100 Ω . This difference is due to the inaccuracy of the NMOS thermal model.

2) Based on the measurements, the temperature effect is compensated around the frequency 41 GHz, since the R_{PTC} value increases with temperature.

3) At 45.5 GHz, the measured value R_{PTC} is nearly constant with temperature variation, thus the temperature effect is not compensated at this frequency.

C. Measurement of voltage sensitivity

The measurement of the voltage sensitivity values (γ) is established using the test bench shown in Fig. 9. The PSG (Performance Source Generator E8257D) [15] is used to apply the input RF power in continuous waveform (CW), at the frequency band (39 - 46) GHz. The input and the output of the detector are probed using the I67 probes. In order to shift

the input RF power reference from the PSG plan (P_{in}') to the input detector's plan (P_{in}), the losses of the RF cable and the input probe are subtracted from the PSG injected power (P_{in}'). The voltmeter Agilent 34461A is used to measure the output DC voltage of the detector when (P_{in}) is applied, and so, the voltage sensitivity value (V/W coefficient) is extracted. This voltmeter has an internal impedance about 10 G Ω . A PID temperature control unit is used to vary the temperature of the chuck in the range (20 – 100) $^{\circ}$ C, and so, the detector circuit.

Figs. 10 and 11 show the simulated and measured sensitivity values versus frequency, and for several temperatures. Two main conclusions can be mentioned based on these figures:

1) Based on the simulations, the temperature effect is completely compensated at the frequencies 39.5 and 44.5 GHz

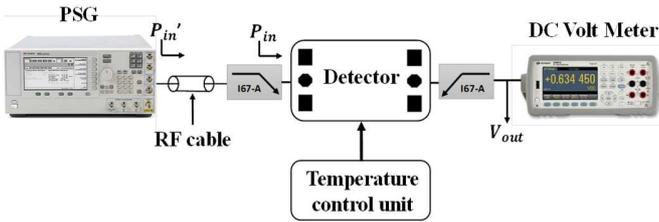


Fig. 9. Test bench used to extract the voltage sensitivity values.

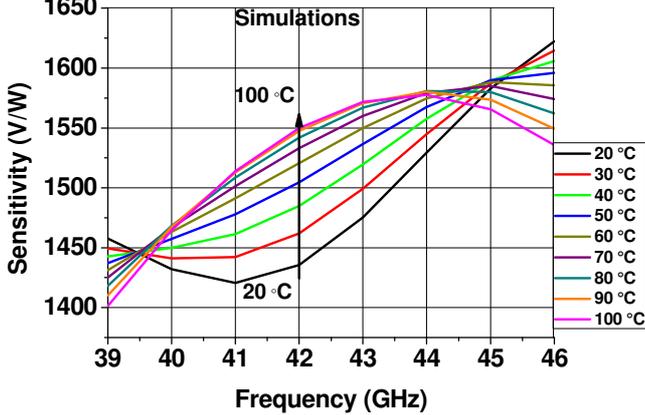


Fig. 10. Simulated voltage sensitivity curves at $P_{in} = -25$ dBm.

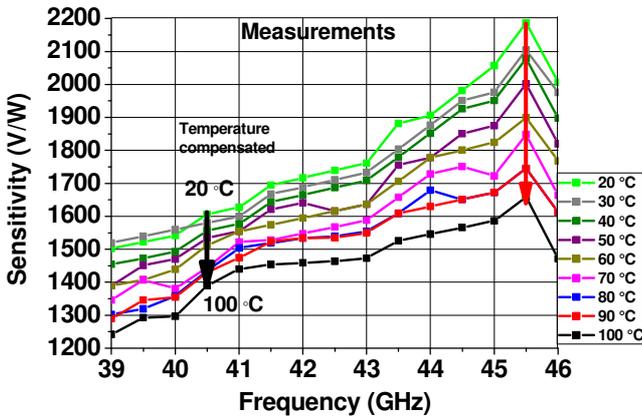


Fig. 11. Measured voltage sensitivity curves at $P_{in} = -25$ dBm.

(γ is nearly constant over temperature variation). On the other hand, the temperature effect is over compensated in the frequency band (40 - 44) GHz (γ increases with temperature),

this is because that the ratio ($\Delta R_{PTC} / \Delta T$) in this frequency band is higher than the ratio at the frequencies 39.5 and 44.5 GHz.

2) Based on the measurements, a significant degradation of γ over temperature is obtained at 45.5 GHz (about 25% of degradation for $\Delta T = 80$ $^{\circ}$ C), meanwhile, this degradation is much smaller at the frequency 41 GHz (about 11% of degradation for $\Delta T = 80$ $^{\circ}$ C). This is because that the temperature effect is compensated at 41 GHz, and not compensated at 45.5 (as explained in III.B). As a conclusion, the temperature compensation circuit reduces the degradation of the sensitivity value (γ) with temperature by more than 55 %.

In order to determine the compression point ($P_{in,max}$), the sensitivity values were measured for different input power levels, and several temperatures as shown in Fig. 12. The compression point $P_{in,max}$ is defined as the input power level for which the sensitivity value is degraded by 10% as compared to its value in the linear zone. Based on the obtained results, it can be noticed that $P_{in,max}$ occurs at about -17 dBm.

D. Extraction of the video resistance and noise floor

The video resistance of detector (R_V) represents the detector output impedance at DC and baseband frequencies. This parameter is required to determine the minimum load value

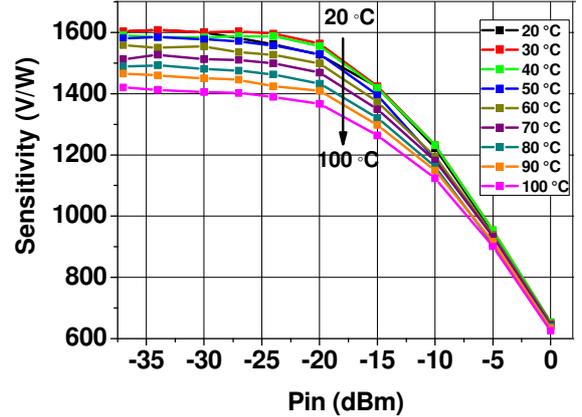


Fig. 12. Measured voltage sensitivity curve vs input power at 41 GHz.

with which the output voltage drop is not significant, and also to determine the noise floor of the detector. The noise equivalent power (NEP) represents the detector noise floor normalized to 1 Hz of video bandwidth. The R_V and the estimated NEP values can be extracted as in the following formulas [12]:

$$R_V = R_L \left(\frac{V_{unloaded}}{V_{loaded}} - 1 \right) \quad (2)$$

$$NEP = \frac{\sqrt{4 \cdot K \cdot T \cdot R_V}}{\gamma} \quad (3)$$

The V_{loaded} and $V_{unloaded}$ represent the output DC voltage for the loaded and unloaded detector respectively. R_L is the load value of the loaded detector. K is the Boltzmann constant, T is the absolute temperature in kelvin.

Table I presents the extracted values of the video resistance (R_V) and the estimated NEP for several temperatures. It can be

noticed that the R_V and the NEP values are decreased as increasing the temperature.

In Table II, some parameters of our detector are compared to other published temperature compensated detectors. Our detector has higher working frequency band, and it is operated with no power consumption, and therefore, it is autonomous detector. In addition, the proposed detector circuitry is quite simple as compared to the other works.

IV. CONCLUSION

The synthesis and characterization of a real-time temperature compensated power detector were presented in this article. This detector is based on low threshold NMOS transistors, operated in the frequency band (40.5-42.5) GHz, integrated in SiGe 55-nm BiCMOS technology from STMicroelectronics. A novel

TABLE I
EXTRACTED VALUES OF VIDEO RESISTANCE AND ESTIMATED NEP FOR SEVERAL TEMPERATURES

Temp. (°C)	20	30	40	50	60	70	80	90	100
R_V (M Ω)	4	3.4	1.7	1.3	1.1	1	0.5	0.33	0.25
NEP (pW/ \sqrt{Hz})	158	148	108	96	91	90	66	57	51

TABLE II
COMPARISON WITH PUBLISHED TEMPERATURE COMPENSATED POWER DETECTORS

Ref.	Technology	Frequency (GHz)	Temperature range (°C)	Power consumption (mW)
[7]	180-nm CMOS	23	25 to 100	0.098
[8]	90-nm CMOS	0.82-0.84, 1.92-1.98	-35 to 55	0.3 @ 0 dBm 0.63 @ 26.5 dBm
[9]	65-nm CMOS	2.35-2.55	0 - 100	1
[10]	130-nm CMOS	5	-40 to 100	-
[11]	Commercial Schottky diode	0.9	-25 to 75	0
This work	55-nm BiCMOS	40.5 - 42.5	20 to 100	0

temperature compensation technique was proposed by adding a passive circuit which acts as a resistor with positive temperature coefficient. The proposed detector circuit is quite simple as compared to the other published works. In addition, it works at higher frequency band with no power consumption, this fact makes it suitable to be used with 5G devices, where high power efficiency is required. At the frequency 41 GHz, the measured voltage sensitivity value is compensated, showing small variation ($\gamma = 1530 \text{ V/W} \pm 6\%$) in the temperature range (20~100)°C. Thanks to this original and autonomous design, which can truly eliminate the degradation of sensitivity value due to temperature change.

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