

Functional packaging of RF, mmW and photonic functions based on femtosecond laser micromachining

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Functional Packaging: context and objectives

2

Electro-Optical Packaging for Silicon Photonics

3

Packaging for mmW and sub-THz electronics

4

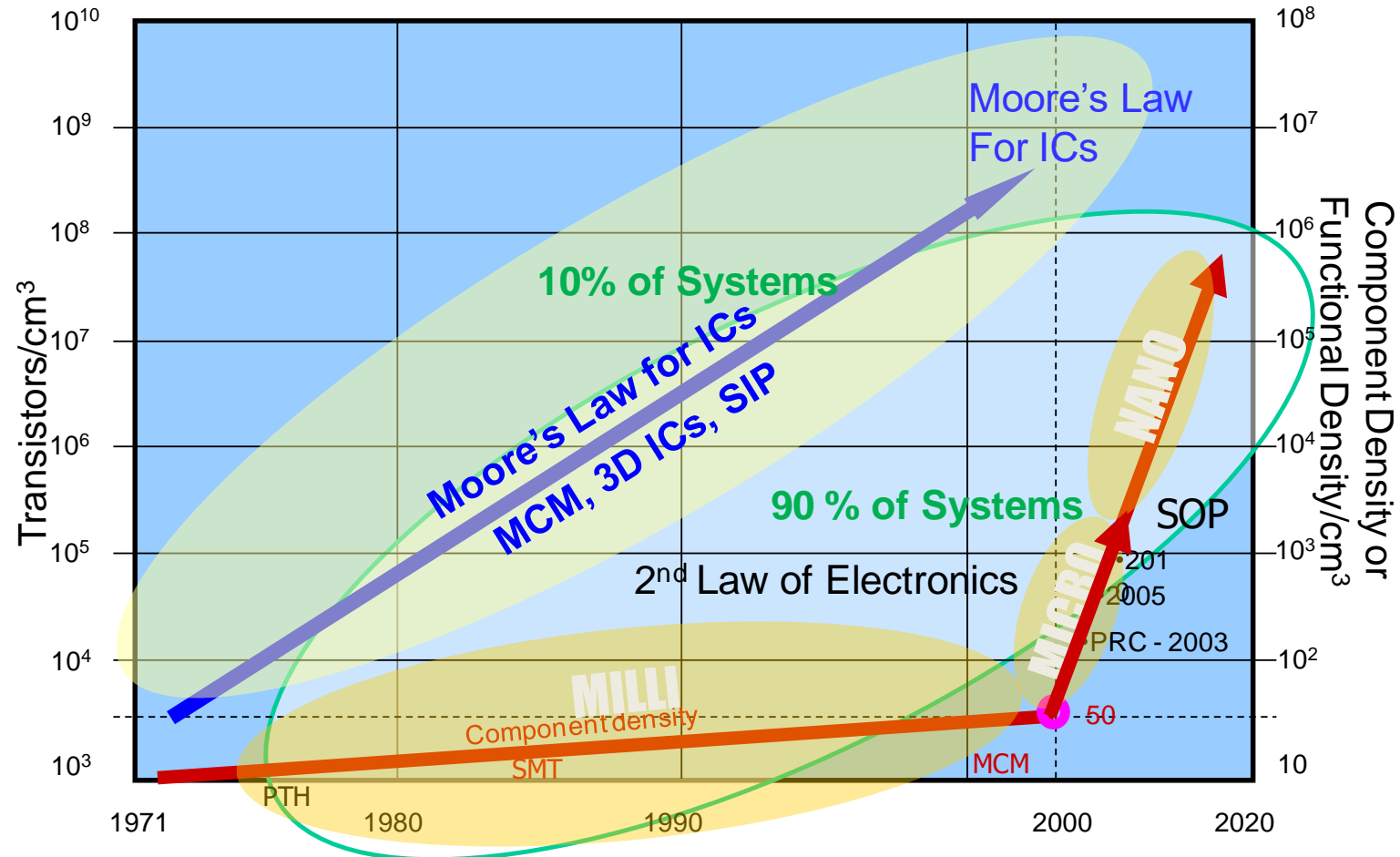
Improved RF SOI-CMOS using laser substrate engineering

5

Perspectives - Summary & Roadmap

Functional Packaging: Context & Objectives

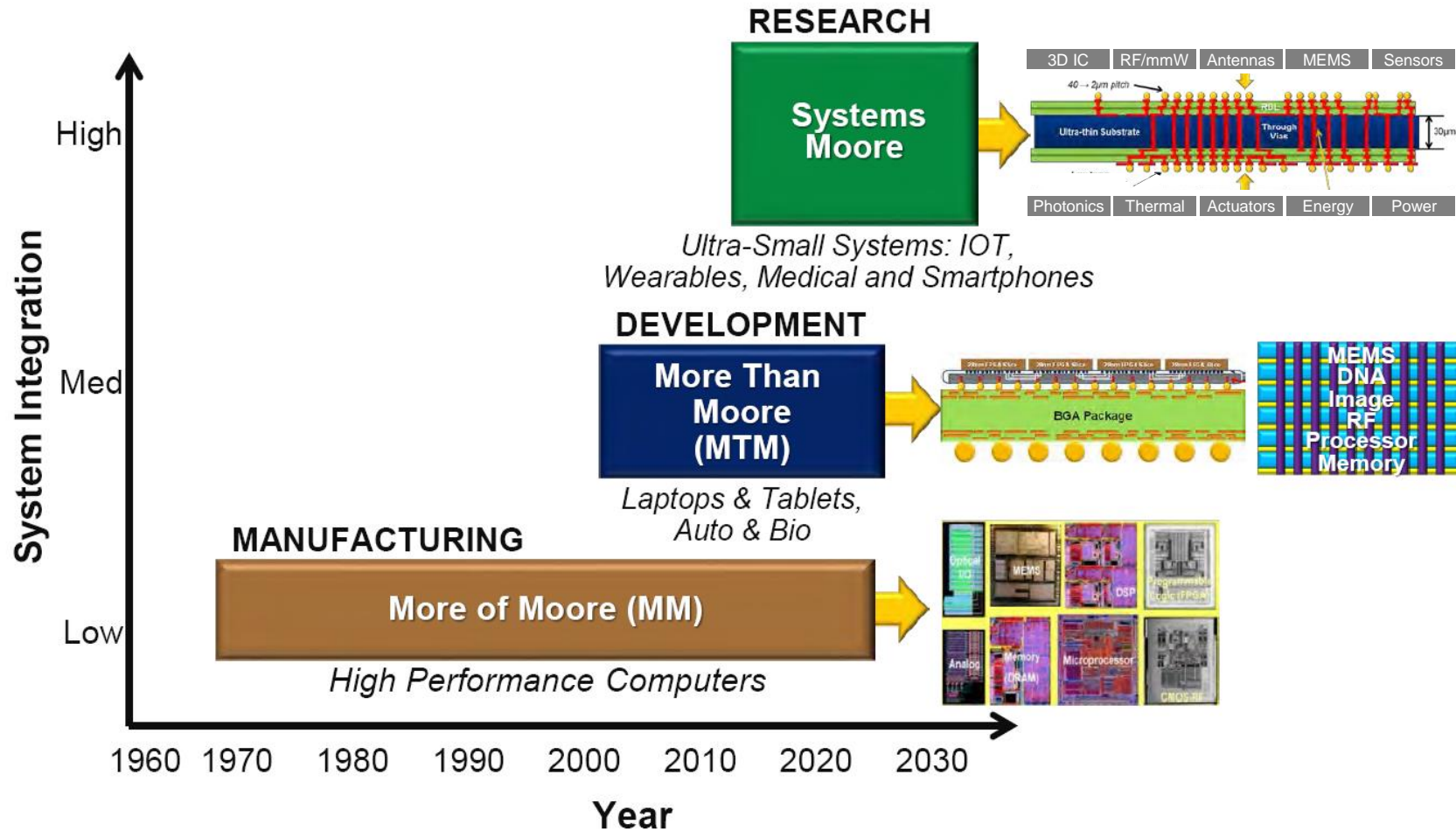
System Moore Paradigm



Sources: IBM, Intel

R. Tummala, System-On-Package (SOP) Mc Graw-Hill 2008

Functional Packaging: Context & Objectives

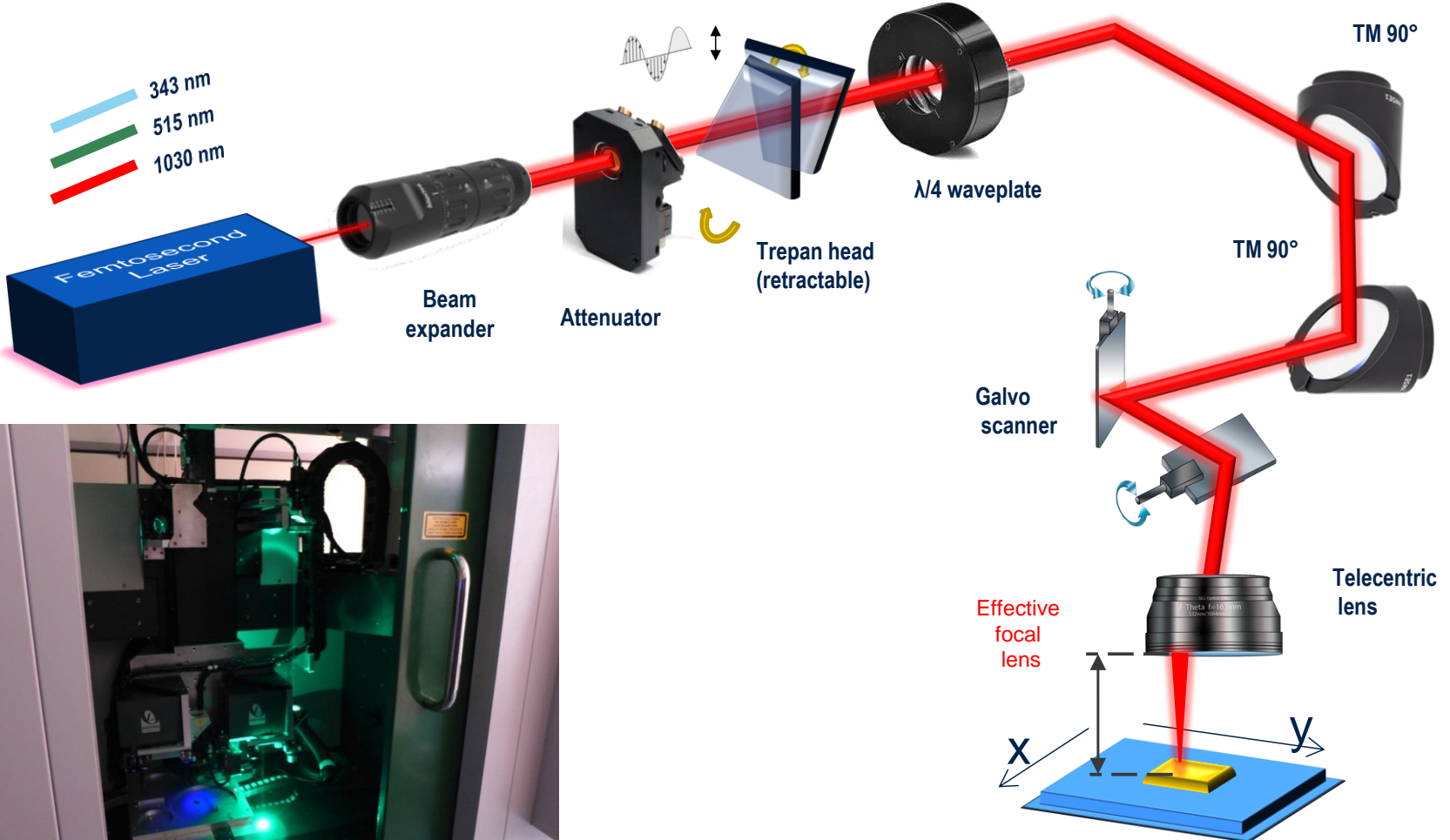
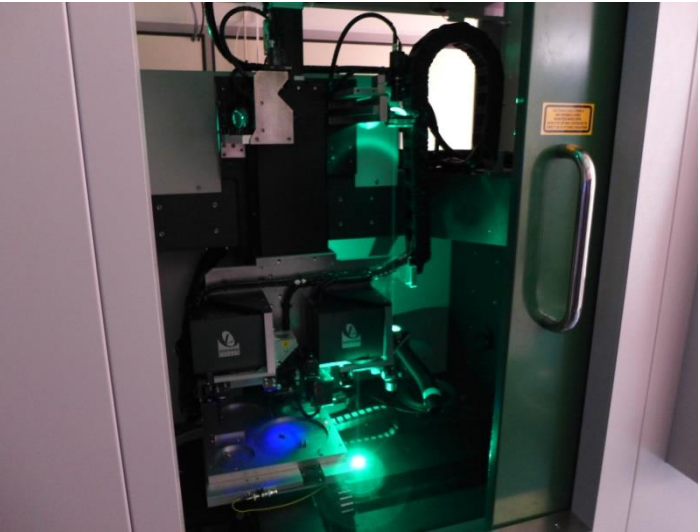
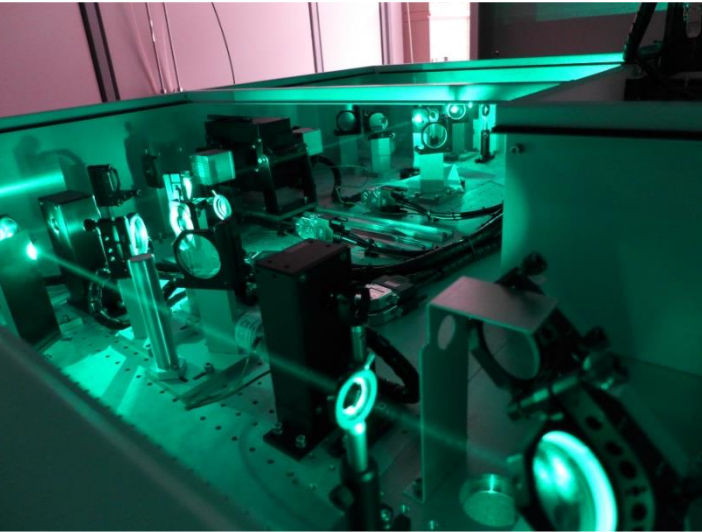
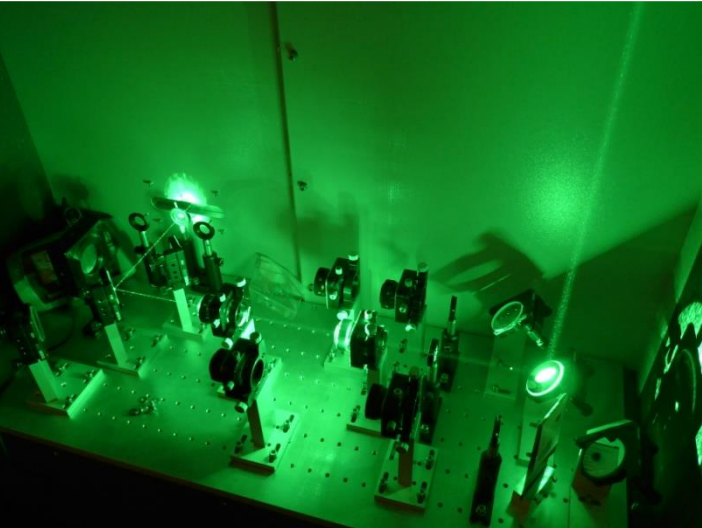


Objectives

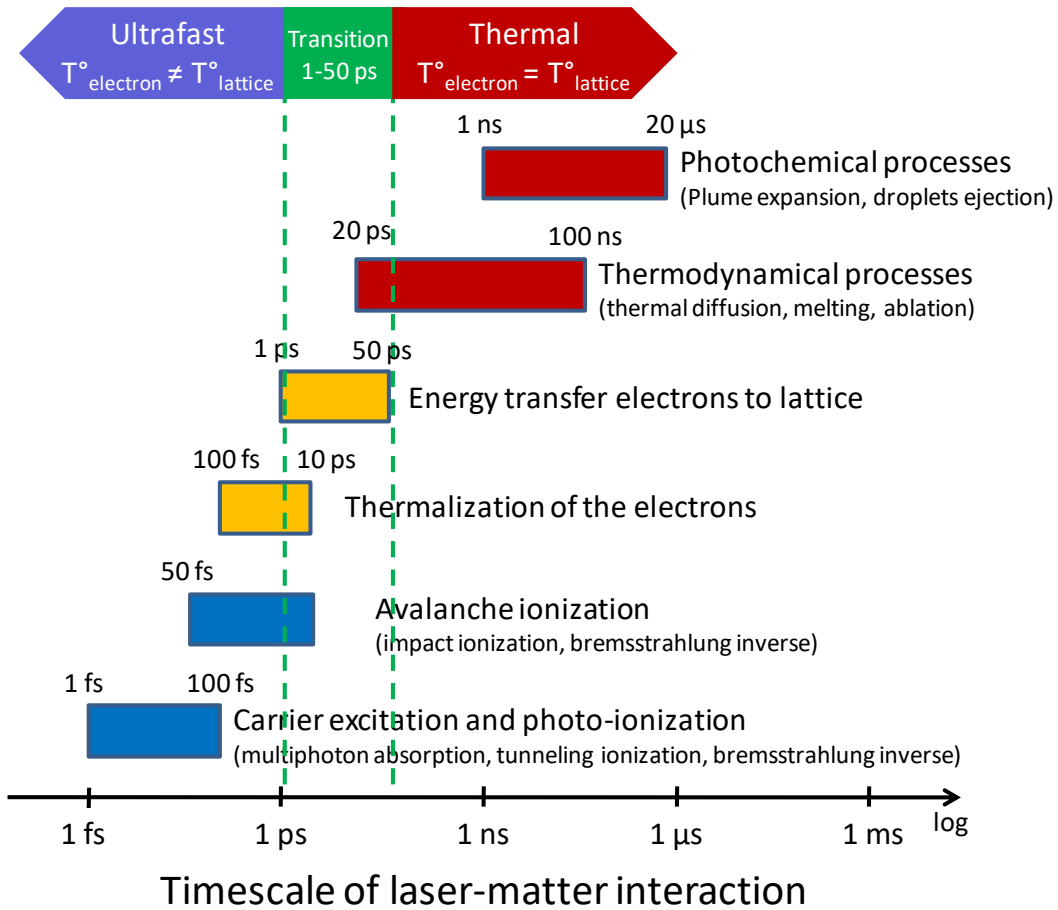
- Fill the technology gap between sub- μm -sized devices and mm-sized system packages
- Support RF, mmW, Photonics technology developments for:
 - Augmented performance
 - New functionalities
 - Device/Circuit/System optimization

R. Tummala, System-On-Package (SOP) Mc Graw-Hill 2008

Femtosecond laser micromachining

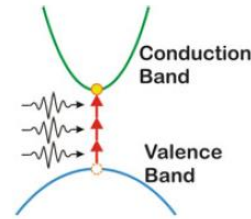


Advantages of femtosecond laser micromachining

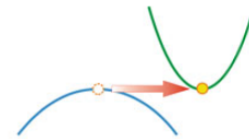


Courtesy : J. Lopez ALPHANOV CELIA UMR 5107

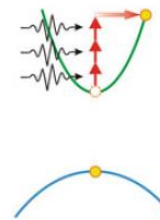
Multiphoton ionization



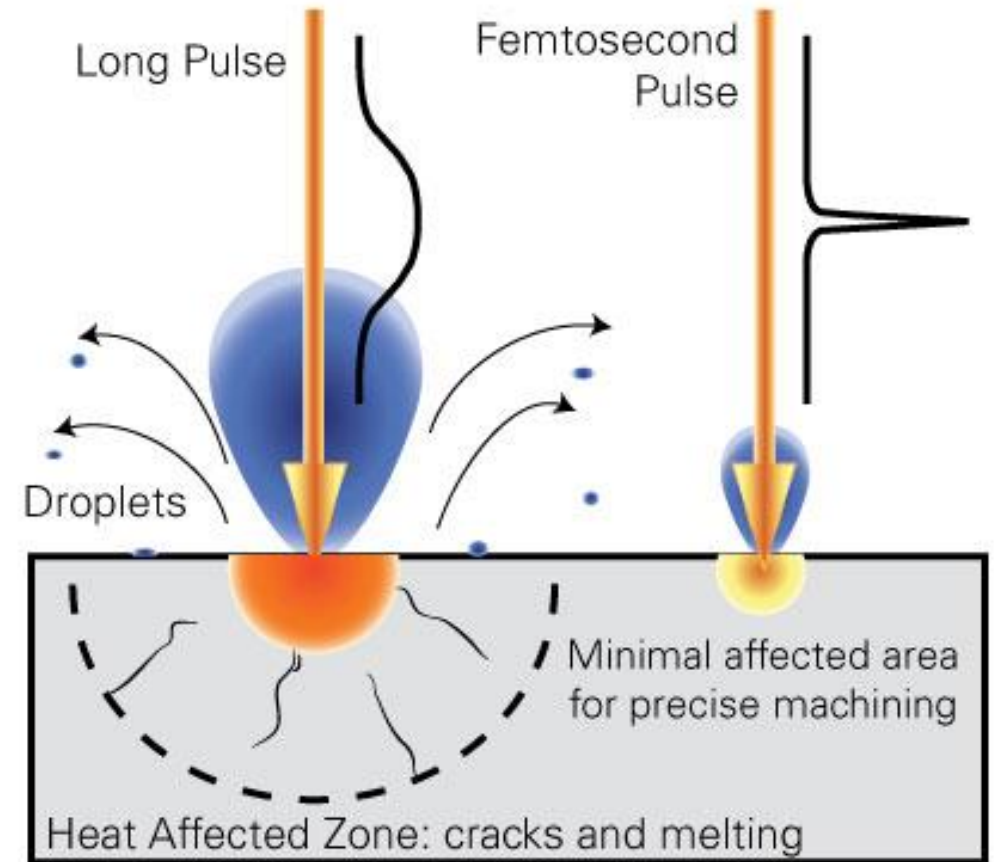
Tunneling ionization



Avalanche ionization



Impact ionization



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2 Electro-Optical Packaging for Silicon Photonics

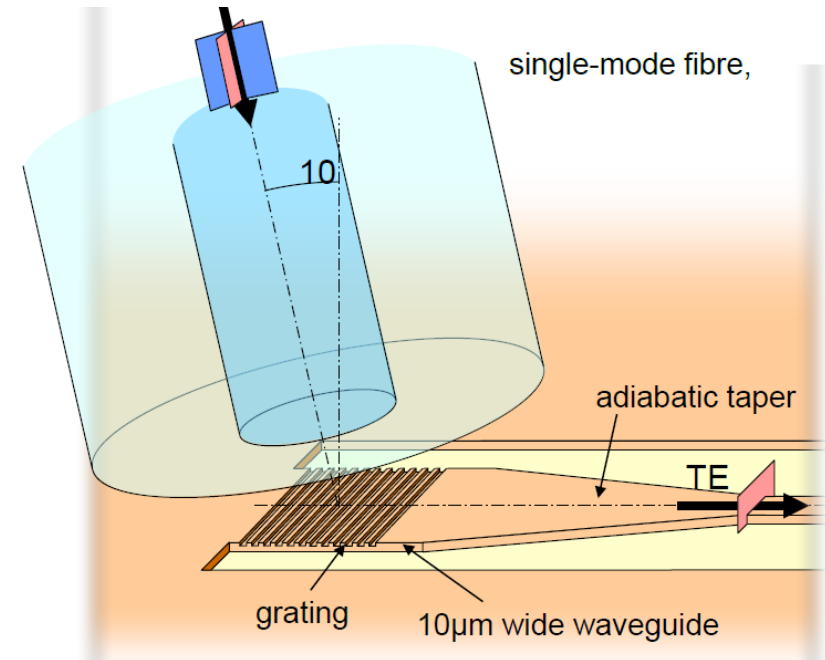
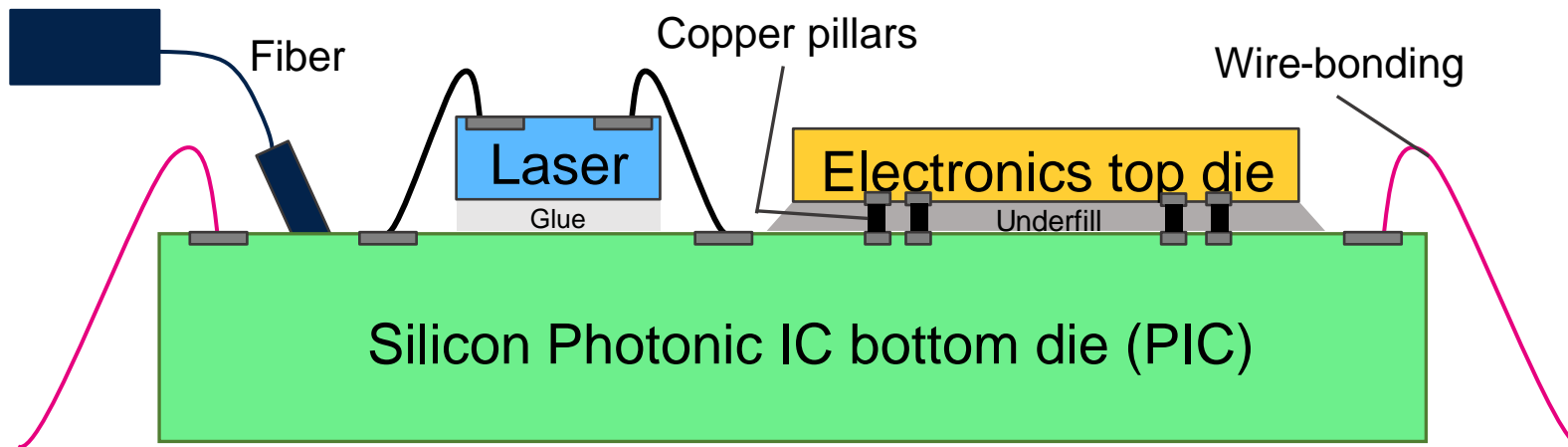
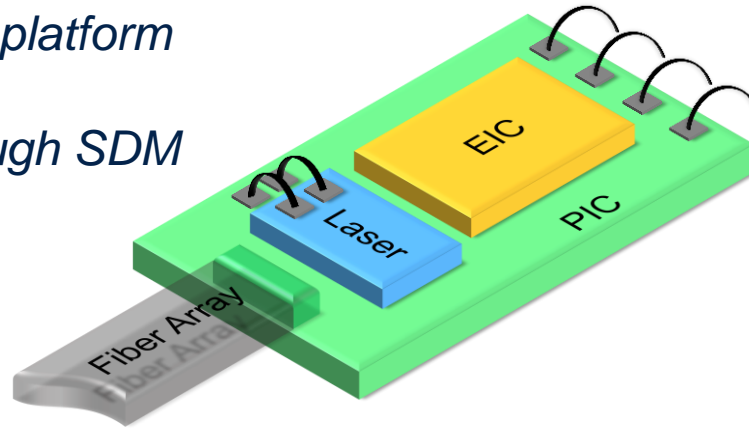
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4 Improved RF SOI-CMOS using laser substrate engineering

5 Perspectives - Summary & Roadmap

Electro-Optical Packaging for Silicon Photonics: motivation

- Silicon photonics
 - Low cost & derived from CMOS platform
 - Single mode communication
 - Addressing 100G standard through SDM
- Limitations
 - Active fiber alignment
 - Narrow optical I/O bandwidth



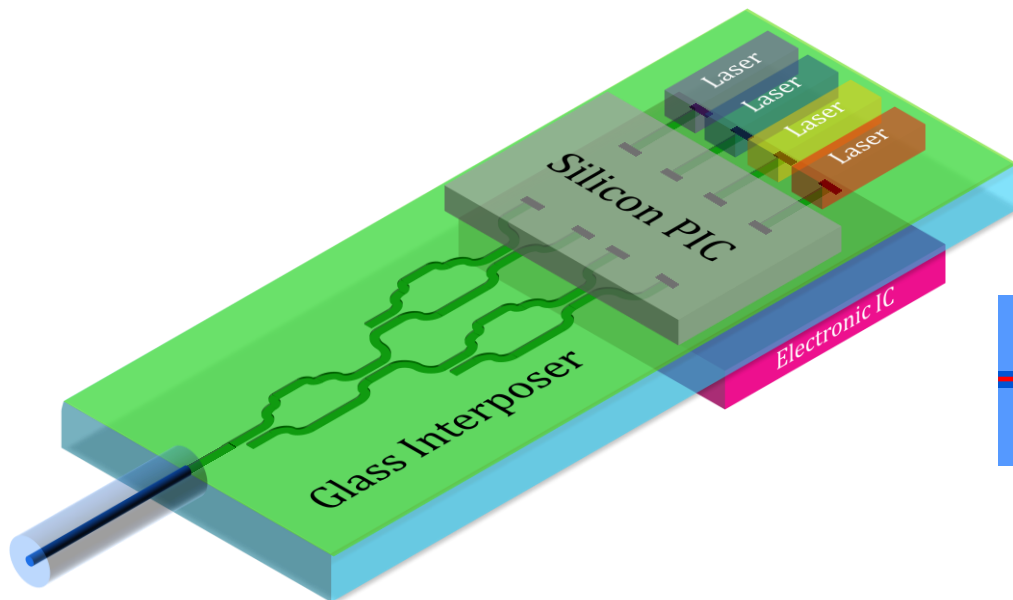
Source: *Coupling light to silicon photonic circuits*, Wim Bogaerts

Source : F. Boeuf *et al.*, IEEE IEDM, 2013

Electro-Optical Packaging for Silicon Photonics

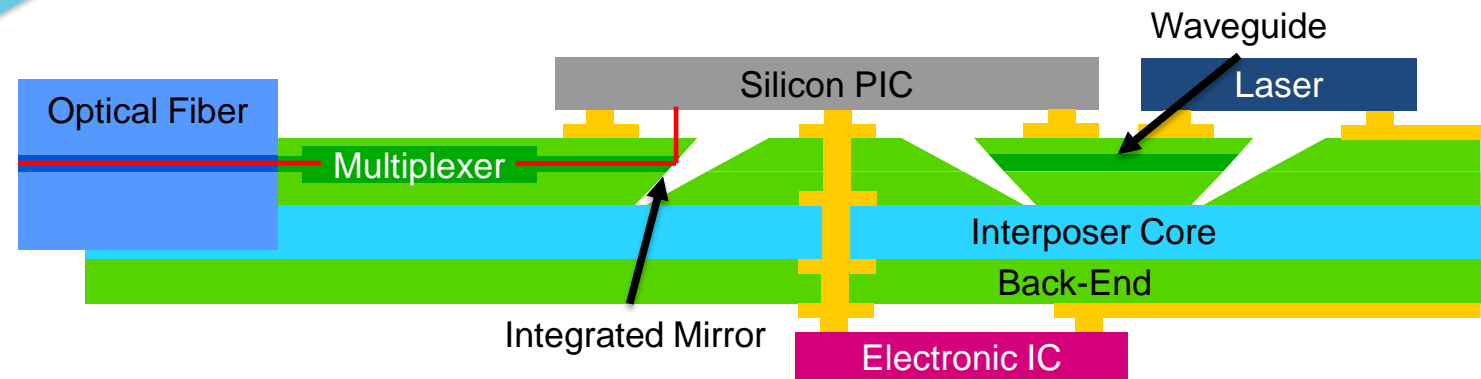
Interposer Added-Value

- Passive alignment fiber butt-coupling
- CWDM Multiplexer on interposer
 - Potentially temperature insensitive
 - Enable wavelength specific grating couplers



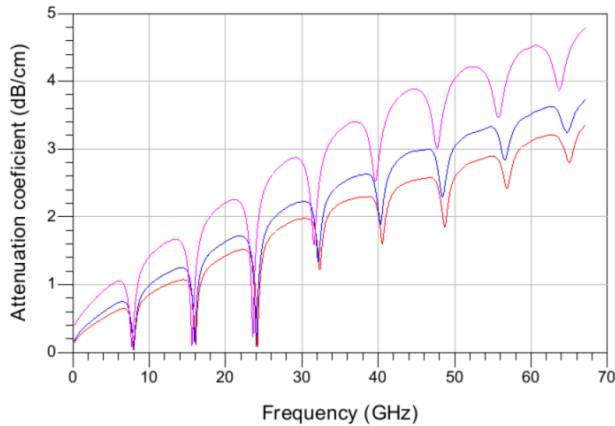
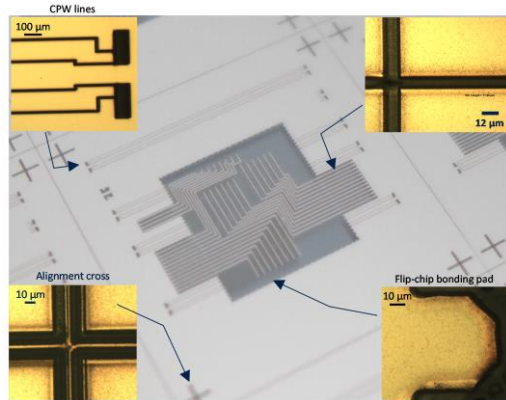
Objectives: packaging of silicon transceivers

- Single mode polymer waveguides
- RF transmission lines
- A slanted mirror for interposer/PIC coupling
- Demonstration of the optical coupling with a flip-chip bonded PIC25G IC

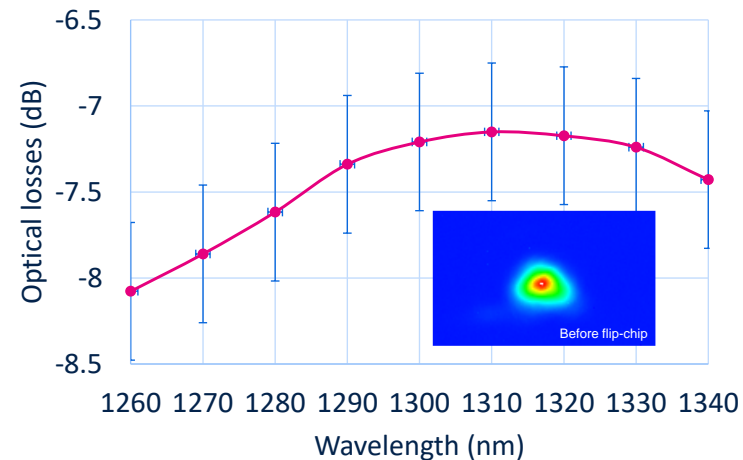
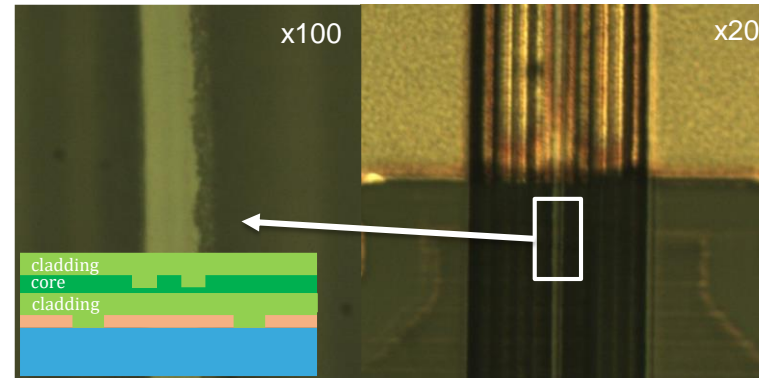


EO Packaging for Si Photonics: technological blocks

RF/mmW transmission lines

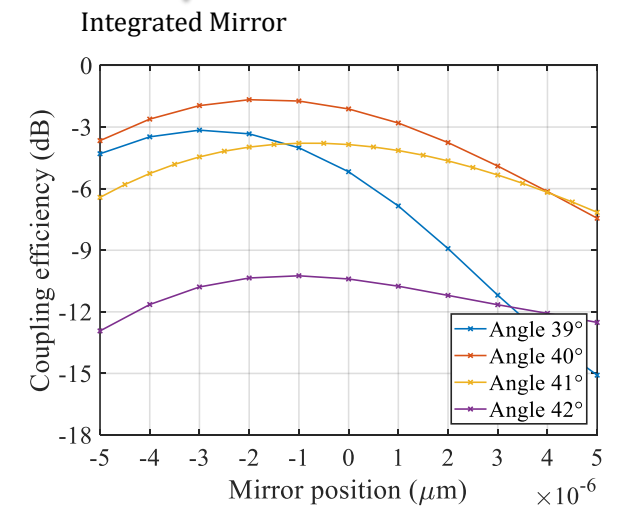
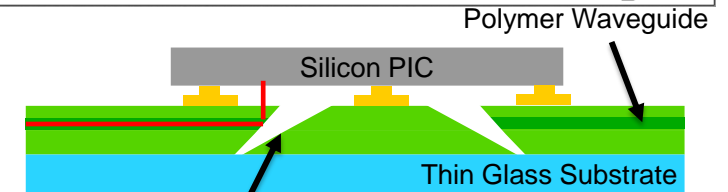
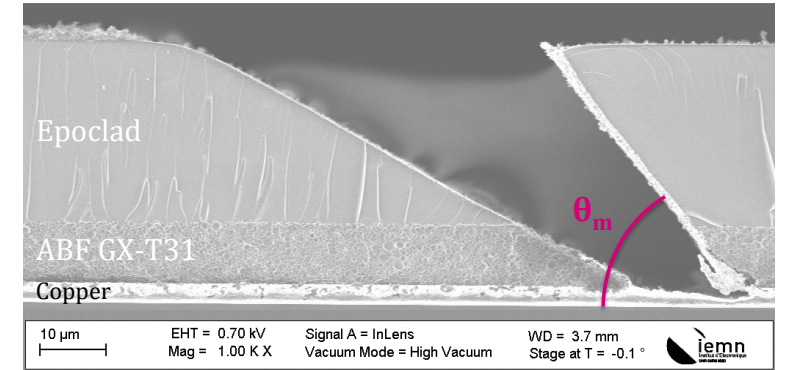


Polymer optical rib waveguides

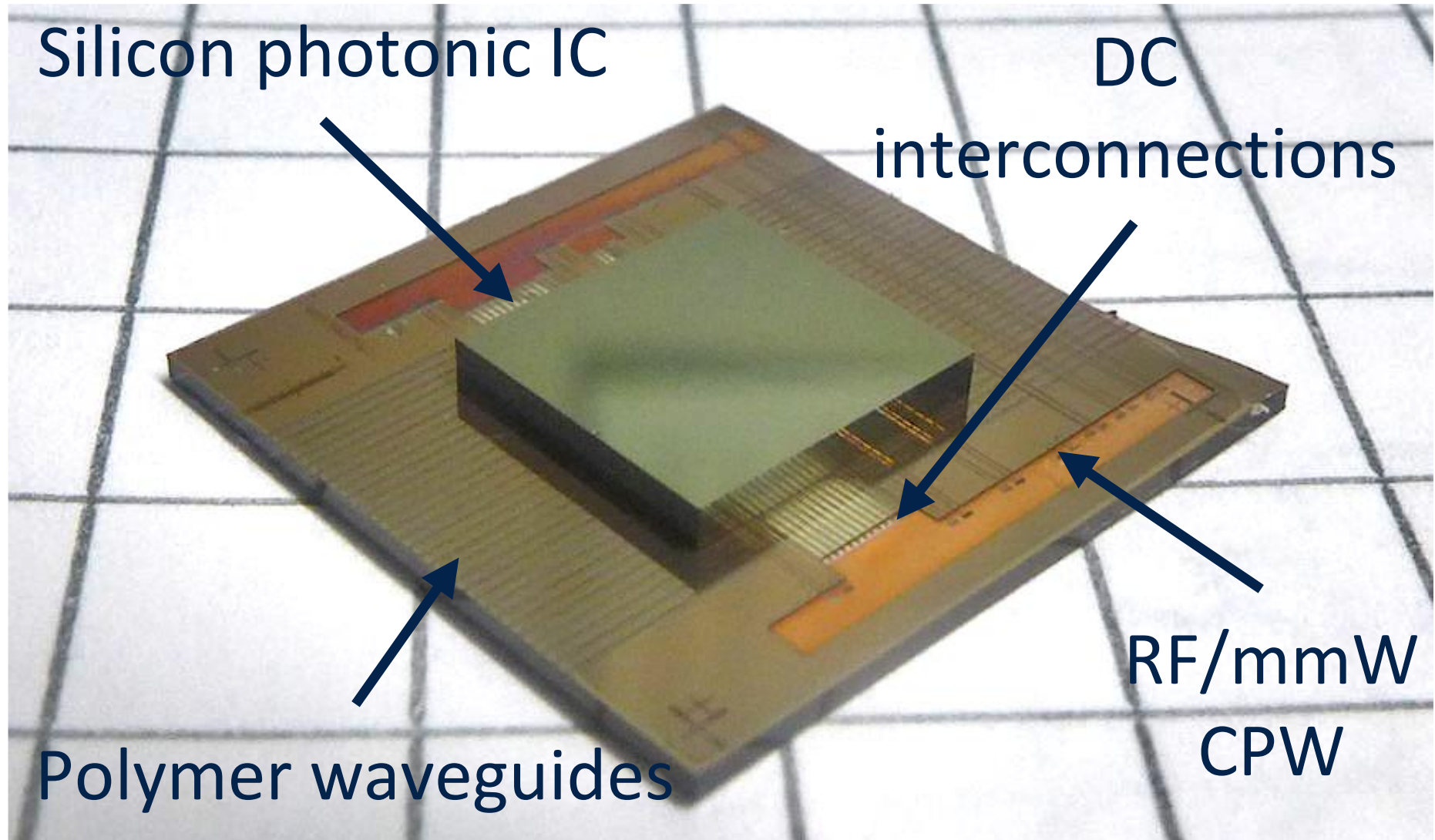


<1 dB variation over CWDM band
 Propagation losses: $4.4 \pm 0.25 \text{ dB.cm}^{-1}$

RF/mmW transmission lines

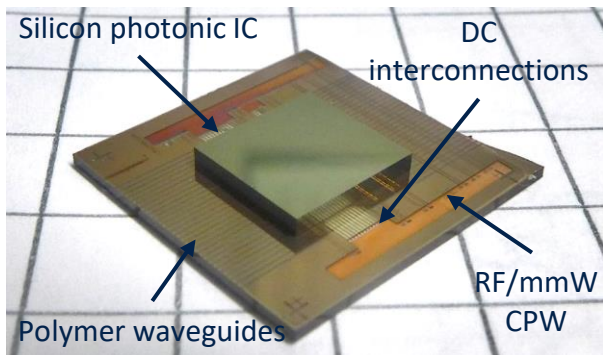


EO Packaging : Assembly and characterization

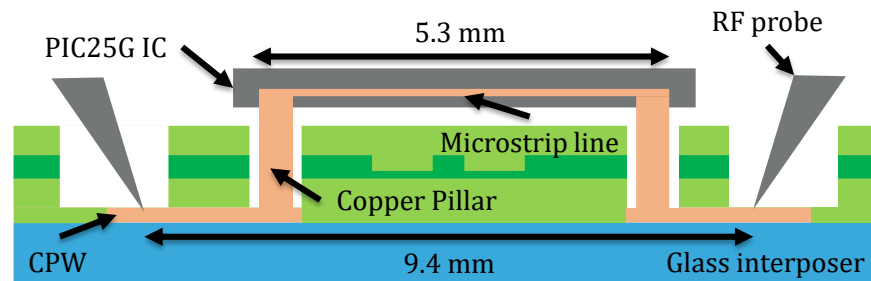


EO Packaging : Assembly and characterization

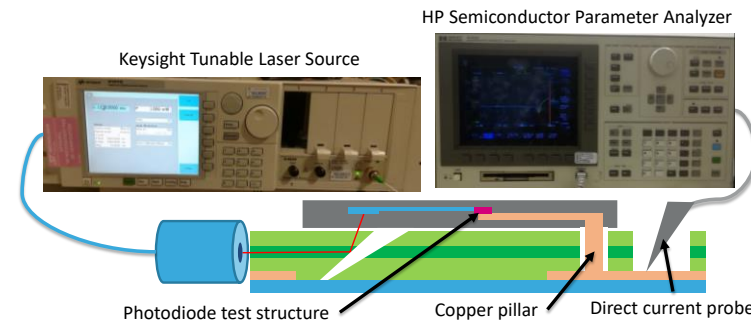
Flip-chip assembly



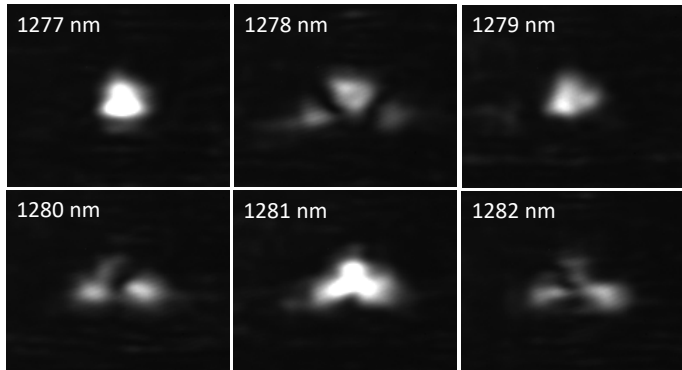
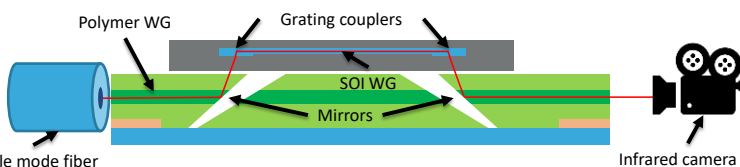
RF/mmW routing



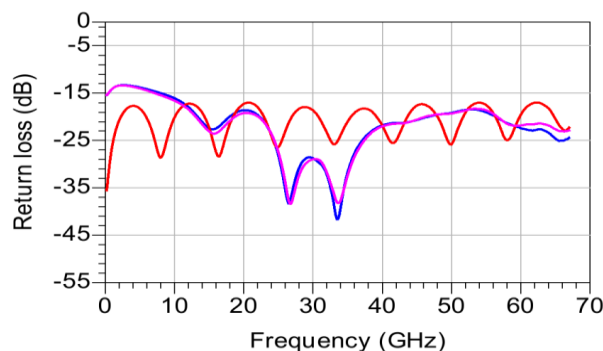
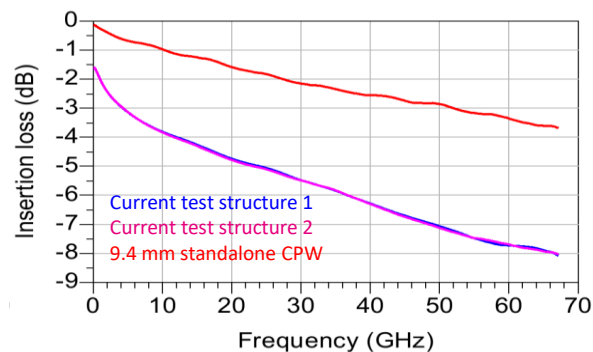
Optical-Electrical conversion



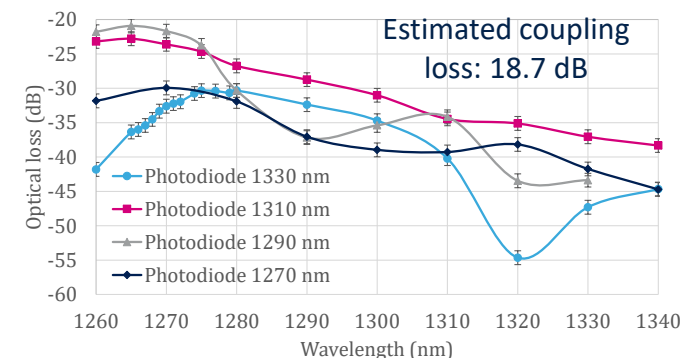
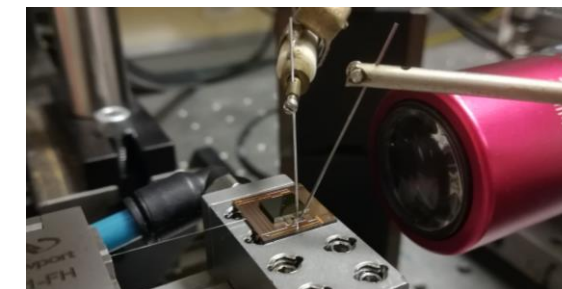
Optical routing



Losses due to mirror & wavelength dependence



High frequency coupling validated
No significant impact on loss



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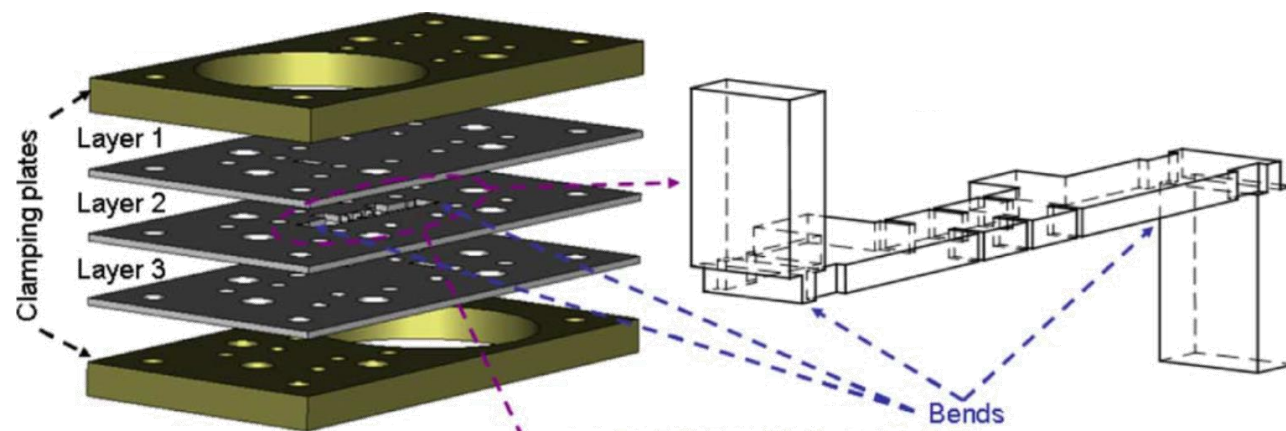
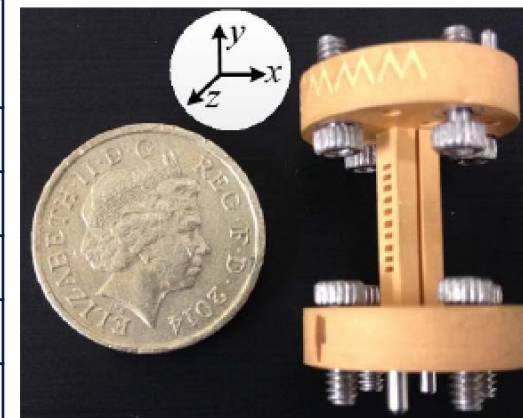
Perspectives - Summary & Roadmap

Packaging for mmW and THz electronics: motivation

Microfabrication Objectives

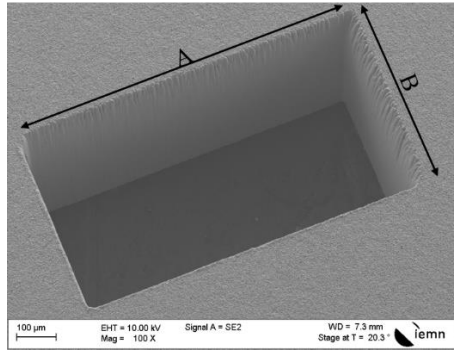
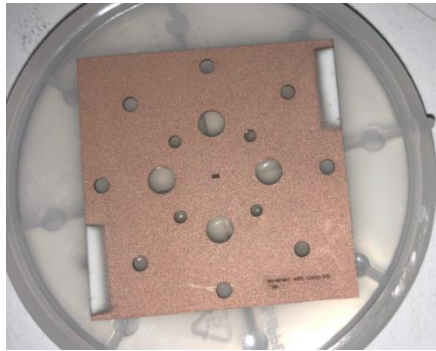
- Need to couple tiny Silicon chips to rectangular waveguides in mmW frequency range
- mmW waveguides fall in the gap between advanced CNC machining and clean room microfabrication
- Use laser micro-machining for low cost and compact planar waveguide architecture

Freq. (GHz)	Band / WG Standard	Dimensions (μm^2)
140-220	G / WR-5	1295x648
220-325	J / WR-3	864x432
325-500	Y / WR-2	508x254
500-750	Y / WR-1.5	381x190
750-1100	Y / WR-1	254x127

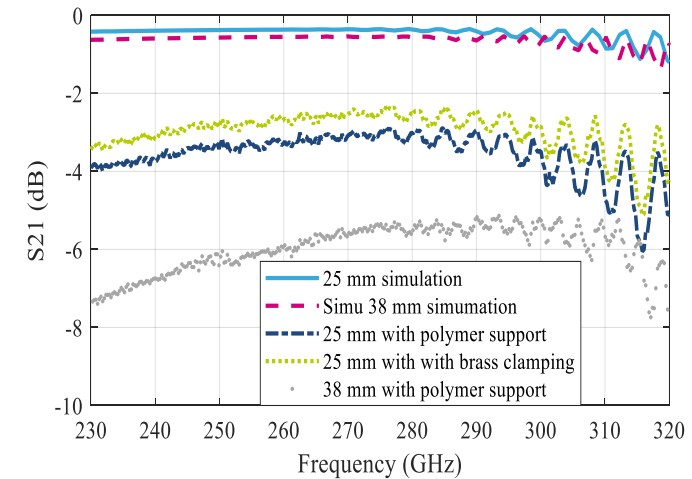
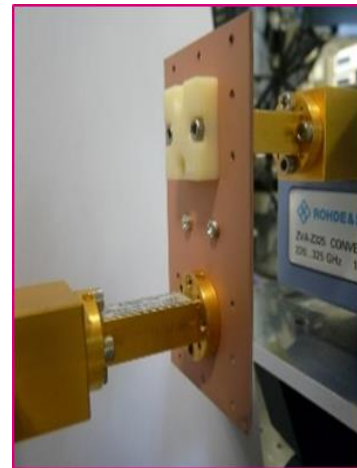
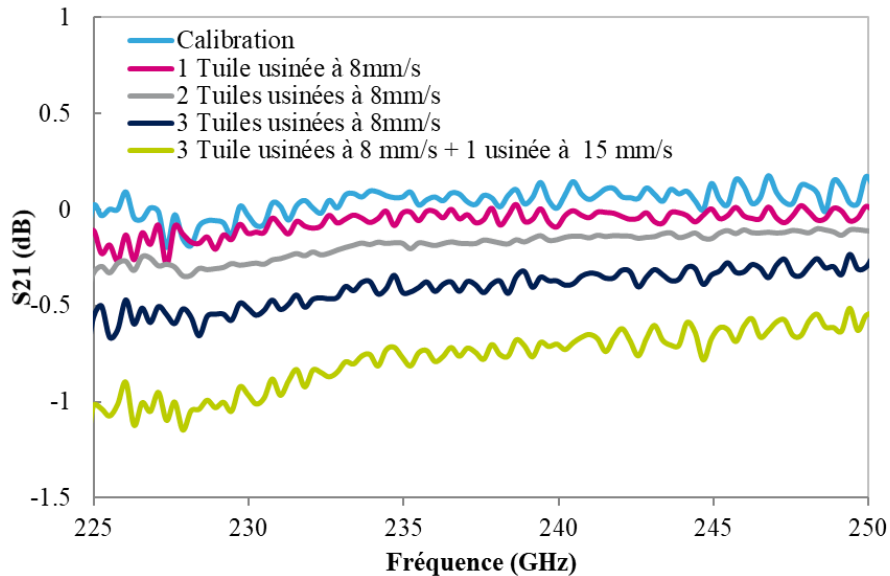
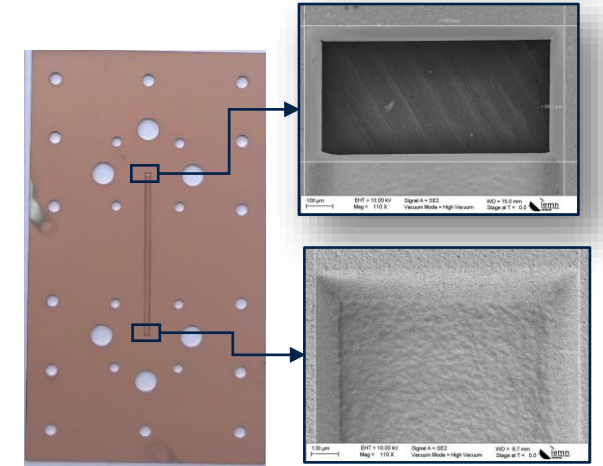
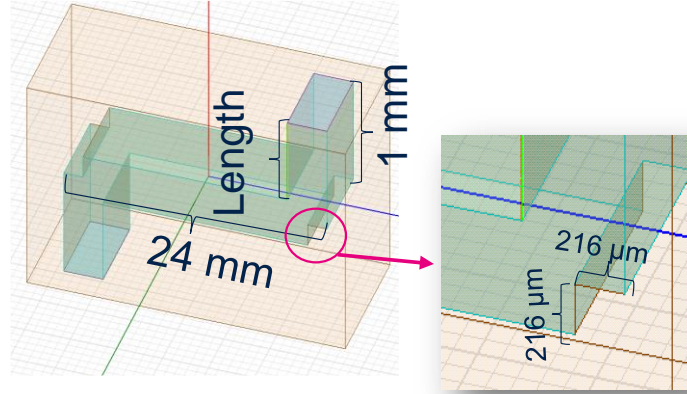


Packaging for mmW and THz electronics

Al₂O₃ Straight Waveguide



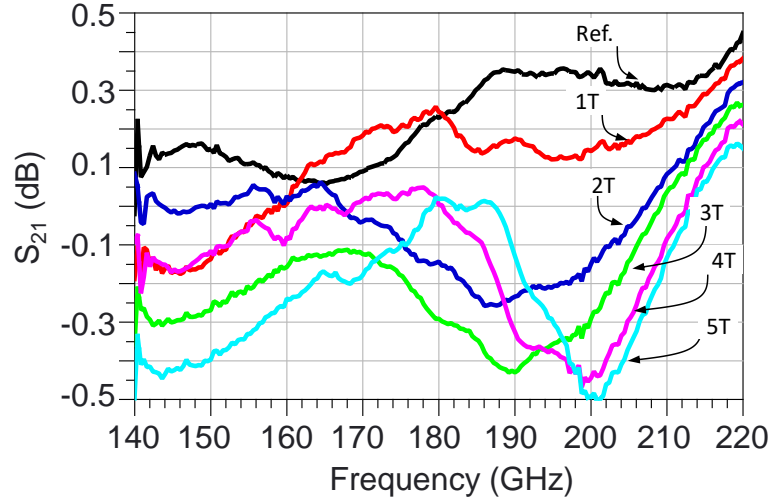
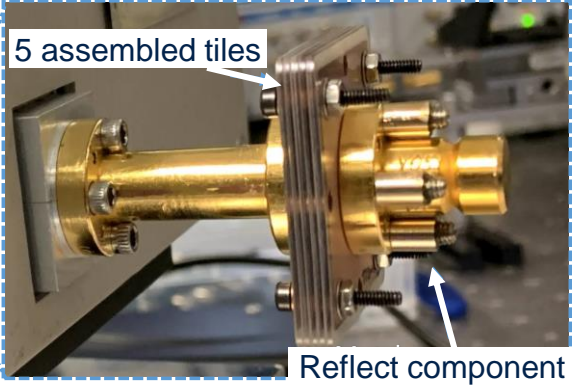
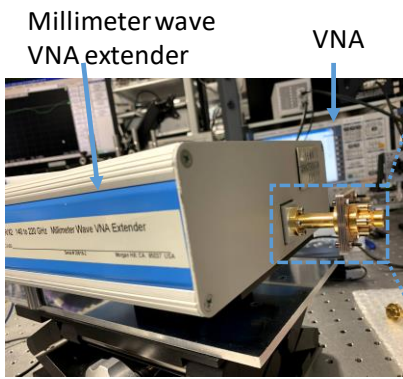
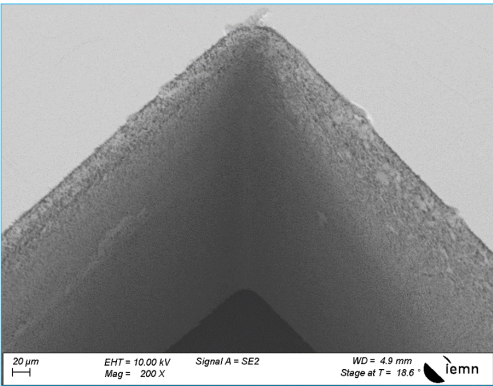
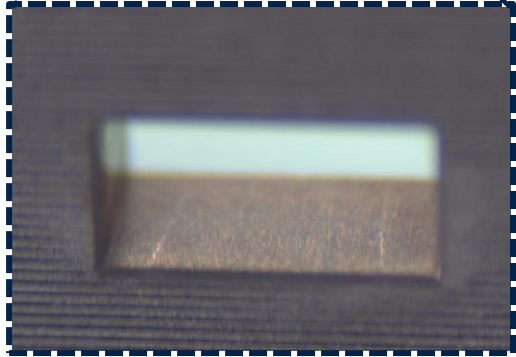
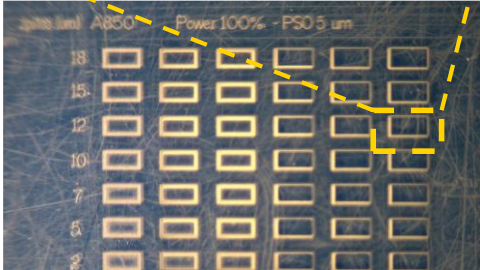
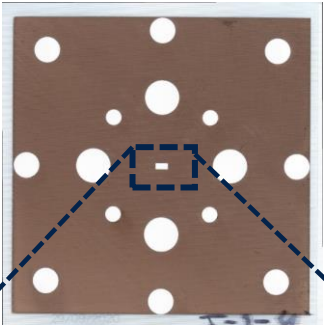
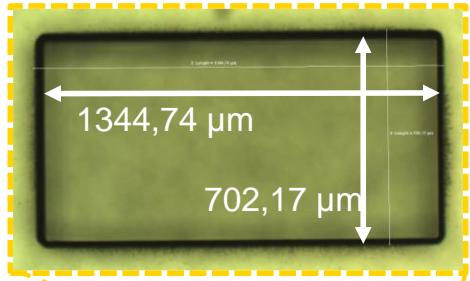
J-Band Tile-Style Planar Waveguide



Packaging for mmW and THz electronics

New material exploration: PMMA

G-band (140-220 GHz) measurements



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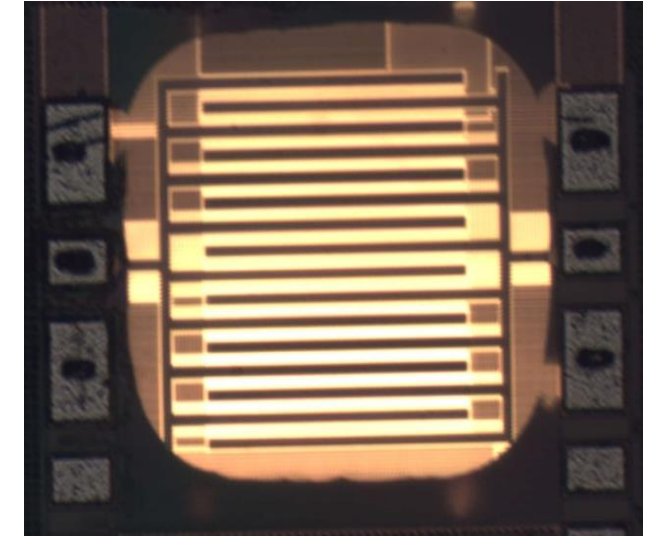
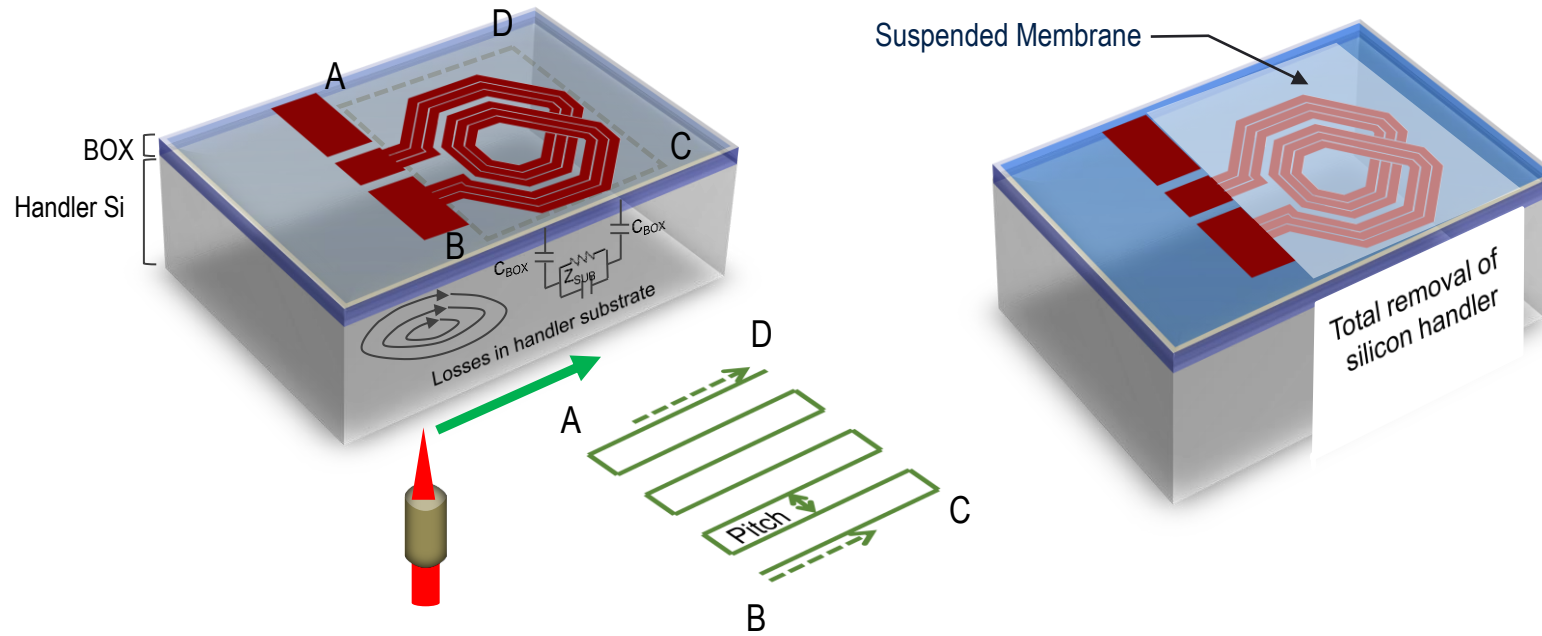
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Improved RF SOI-CMOS using laser substrate engineering

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Perspectives - Summary & Roadmap

Improved RF SOI-CMOS using substrate engineering



Laser Processing Results

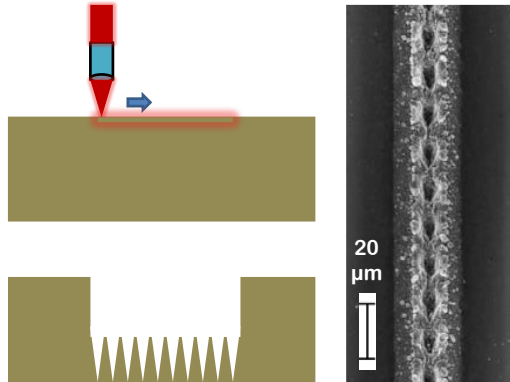
- Efficiency of the silicon laser ablation process
- Study of scribing of trenches for optimal choice of process parameters
- Extrapolation to surface milled cavities
- Fabrication of ultimate membranes on SOI

RF Performance Results

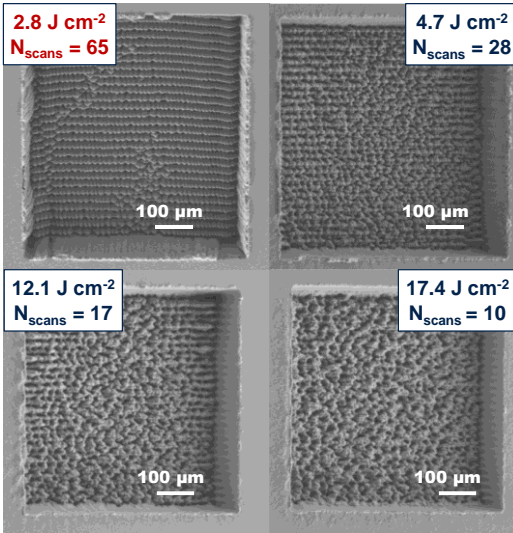
- Study of RF losses (small signal) and linearity (large signal) of SP9T switch
- Study of Q-factor of inductors with compact modelling
- Noise figure study of inductor membranes used in LNA circuits

Laser ablation of silicon in infrared

Trench Analysis

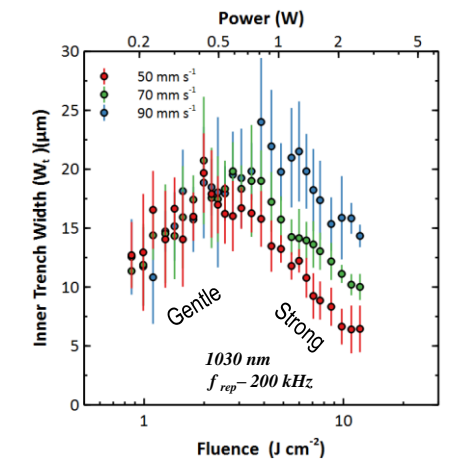
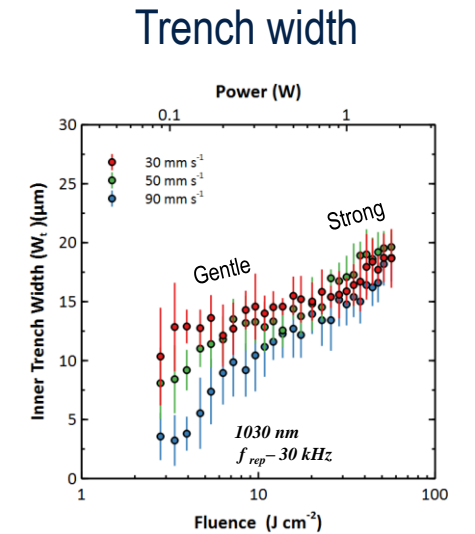
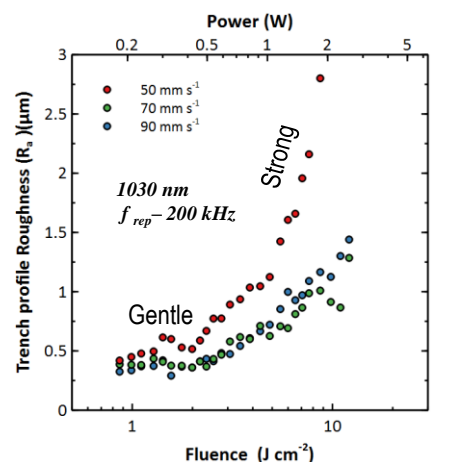
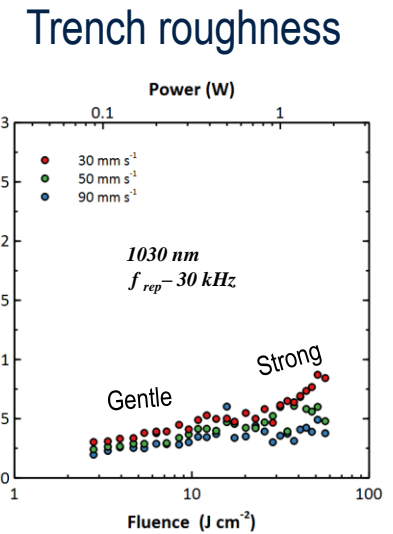
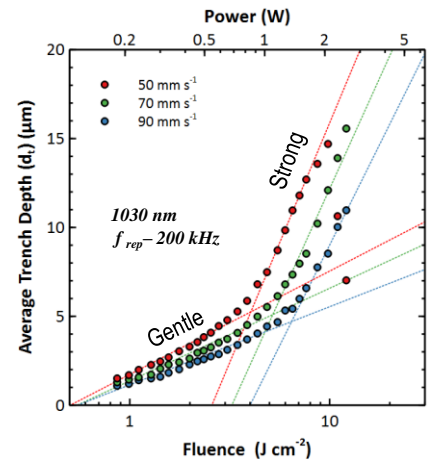
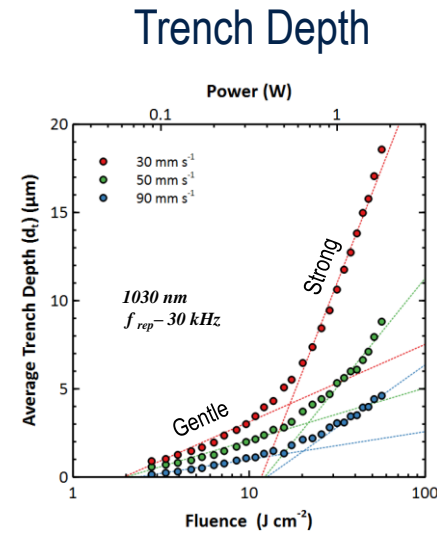


30 kHz



Surface milling optimization

200 kHz



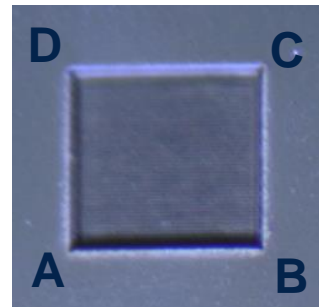
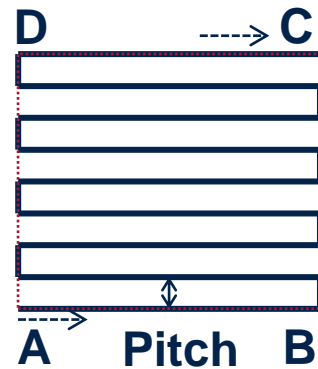
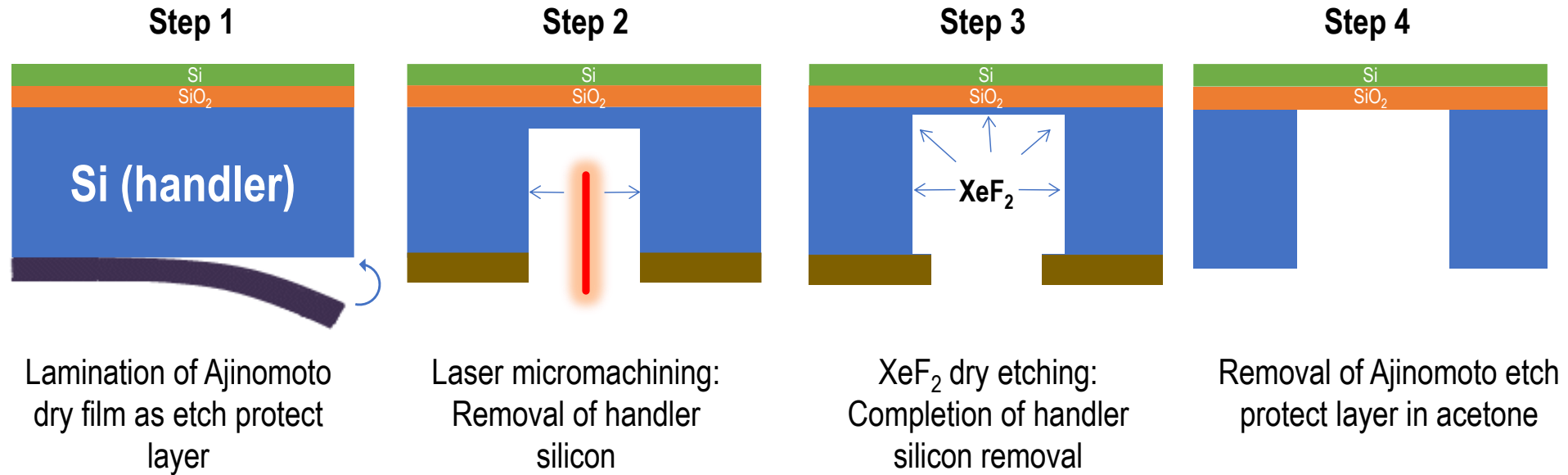
The removal rate can be as high as 20 μm per pass and up to $7 \times 10^6 \mu\text{m}^3 \text{s}^{-1}$

FLAME Process

(Femtosecond Laser Assisted Micromachining and etching)

Application of the FLAME process

Femtosecond Laser Assisted Micromachining and Etch

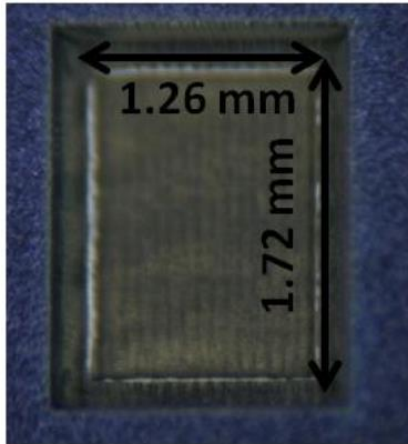


$\text{Area}_{ABCD} \approx \text{Active area of RF component}$

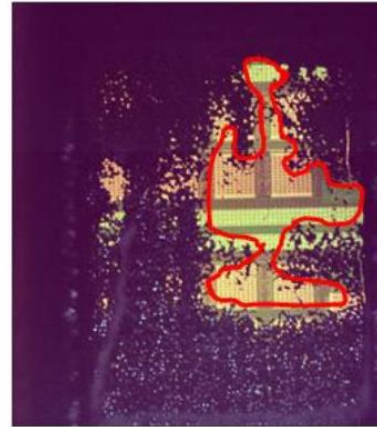
Application of the FLAME process

Femtosecond Laser Assisted Micromachining and Etch

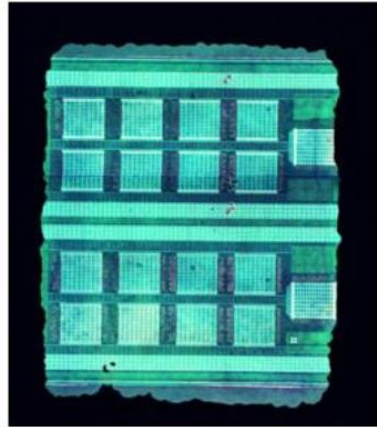
Milled cavity



25 cycles



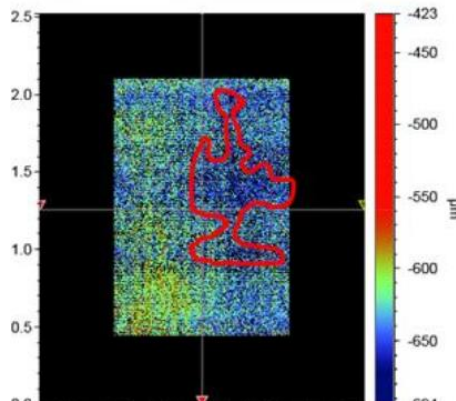
75 cycles



XeF₂ etching

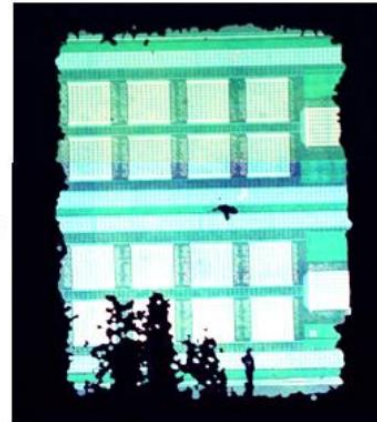


- Selective isotropic etchant of Si over SiO₂ (selectivity of 1000:1)
- Etch parameters (with typical values used)
 - Cycle time: 10 s
 - XeF₂ pressure: 2 Torr
 - Temperature: 40 °C
 - No. of cycles: 30 - 100

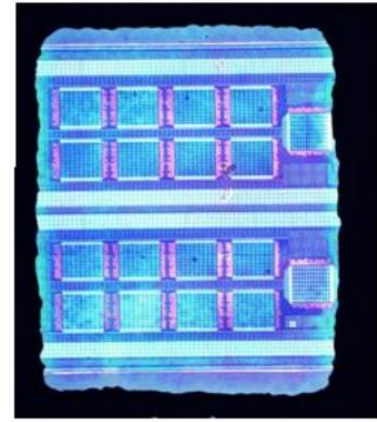


Depth profile

50 cycles

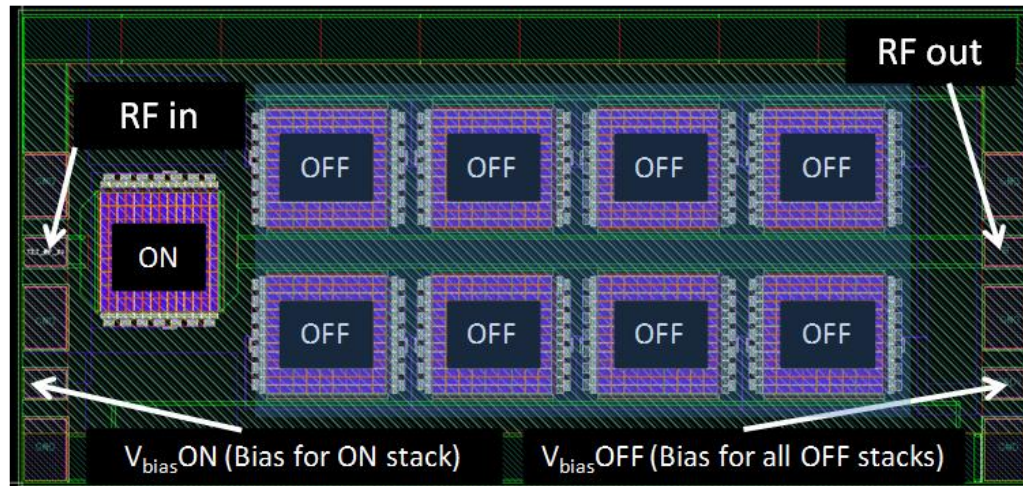
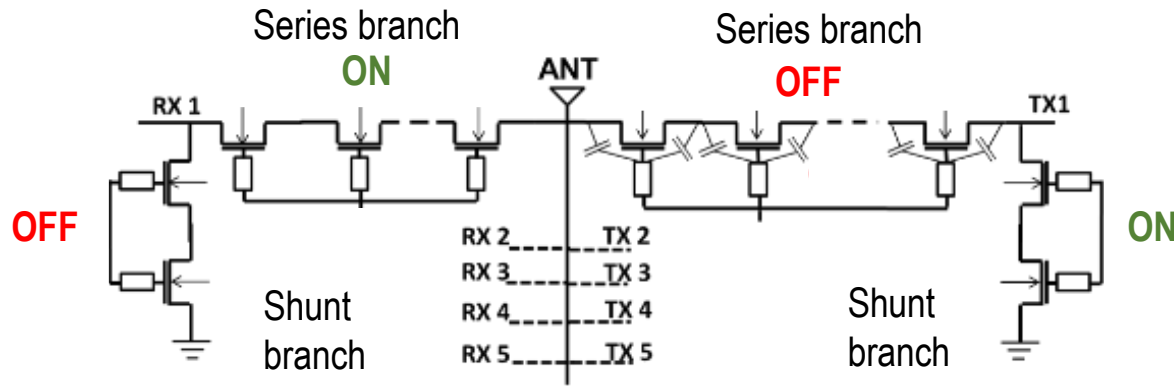


100 cycles



Flame Application to RF switch

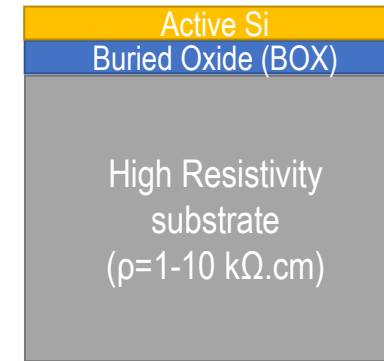
Typical switch architecture



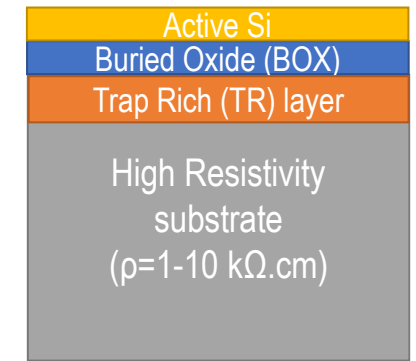
SP9T switch test structure

RF-specific SOI substrates

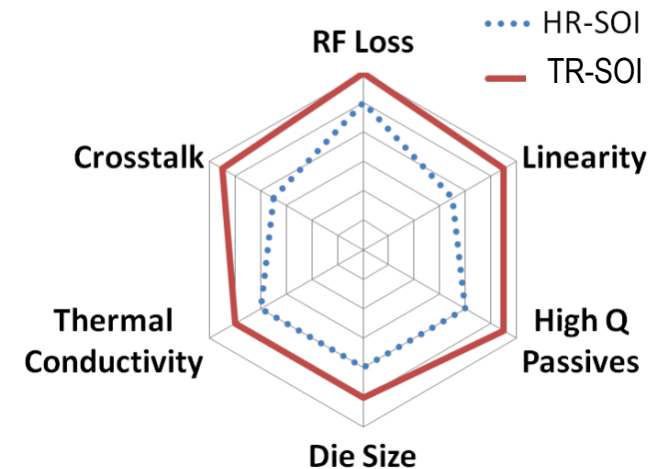
High-resistivity (HR)



Trap-rich (TR)

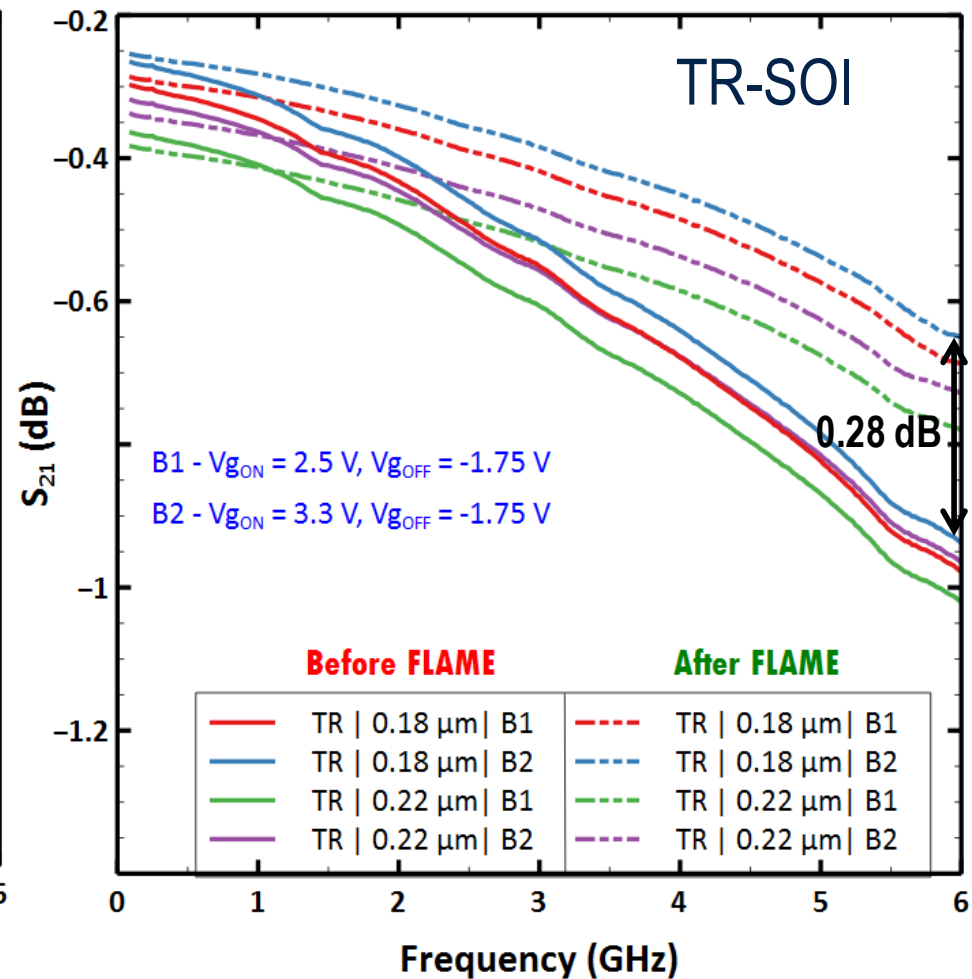
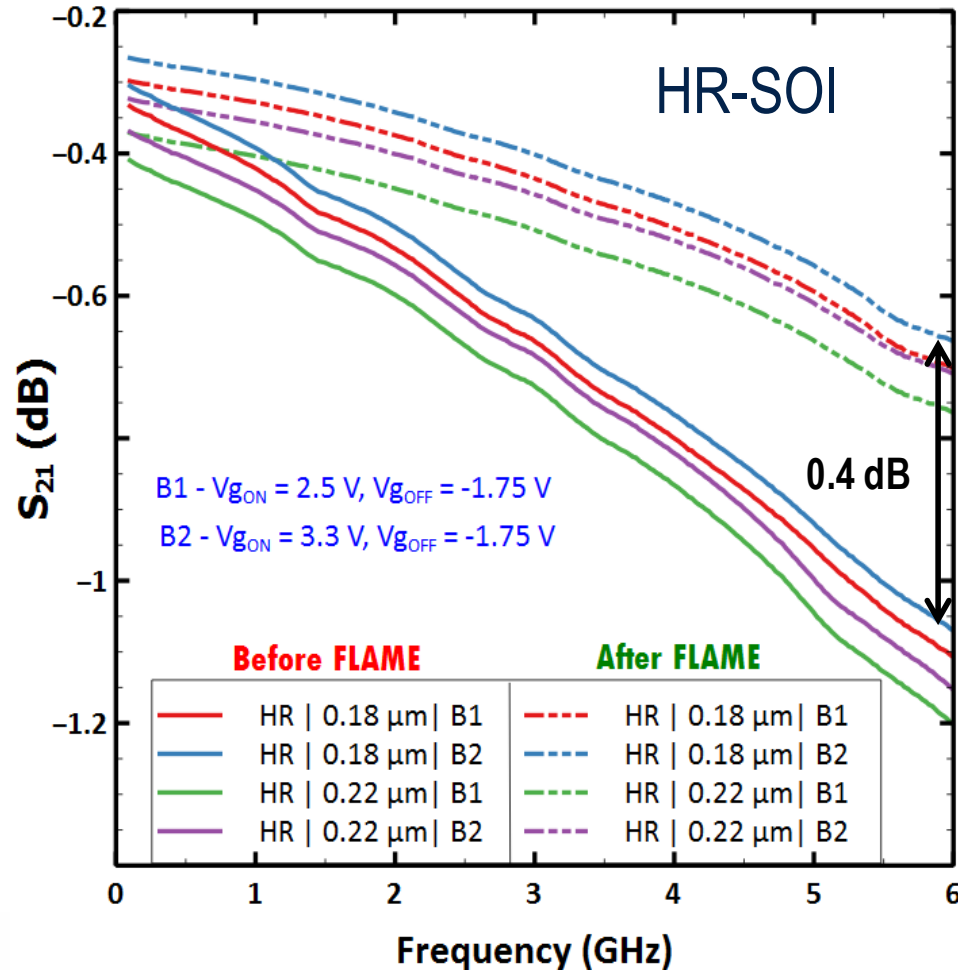


TR-SOI vs HR-SOI performance



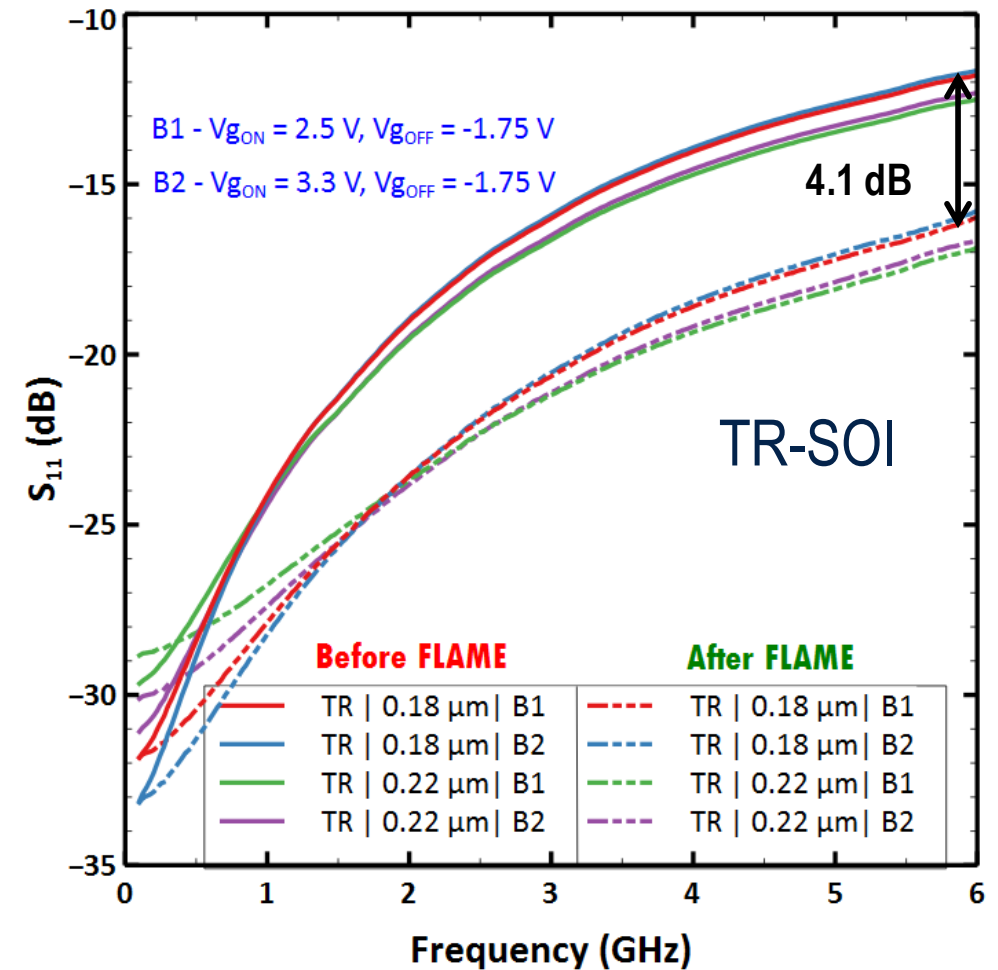
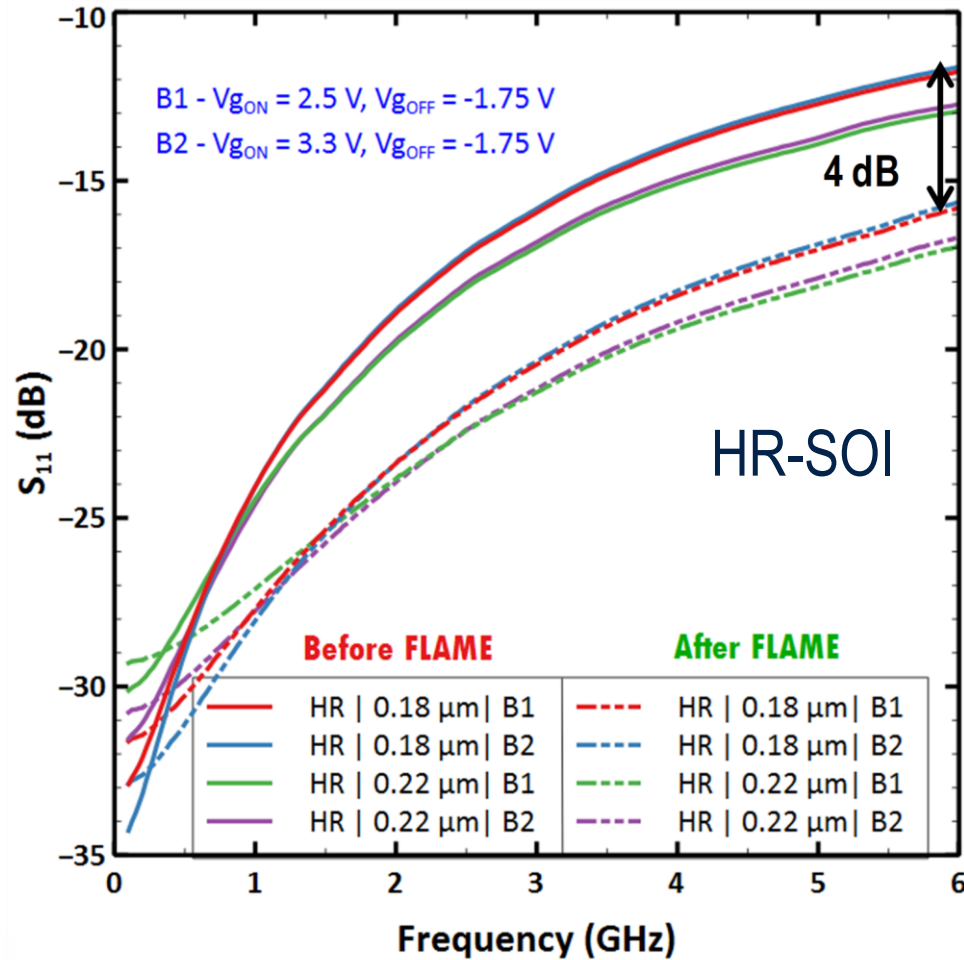
Improved RF SOI-CMOS switch: insertion losses

SP9T switch



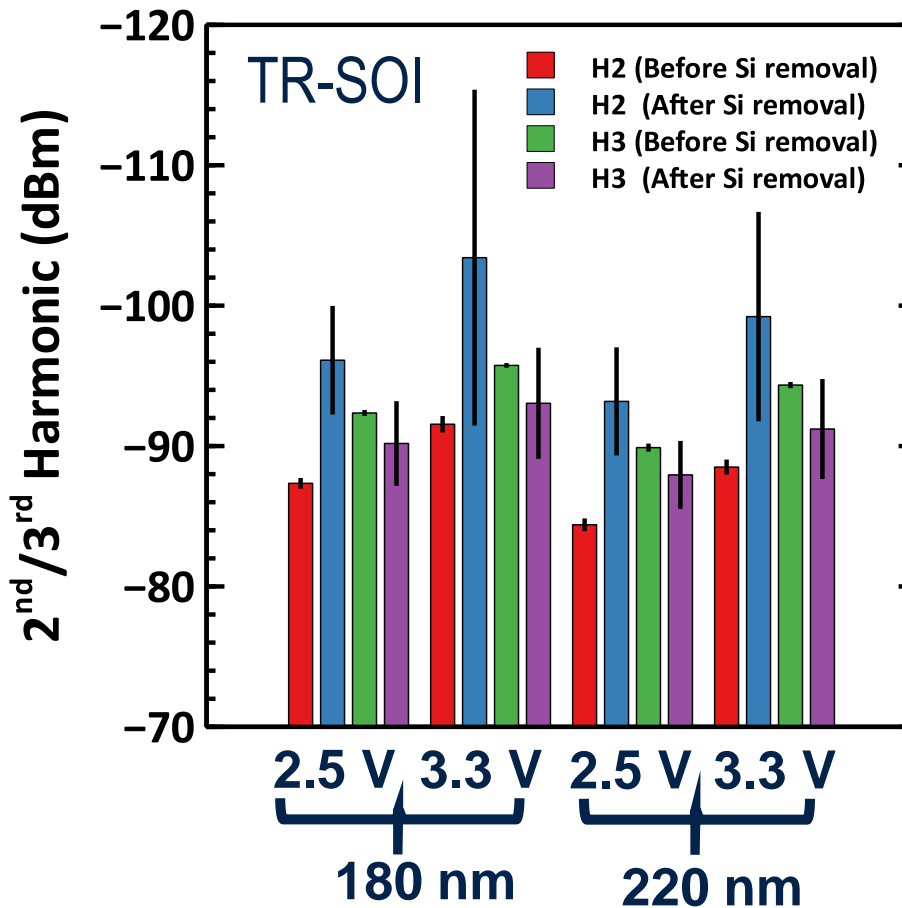
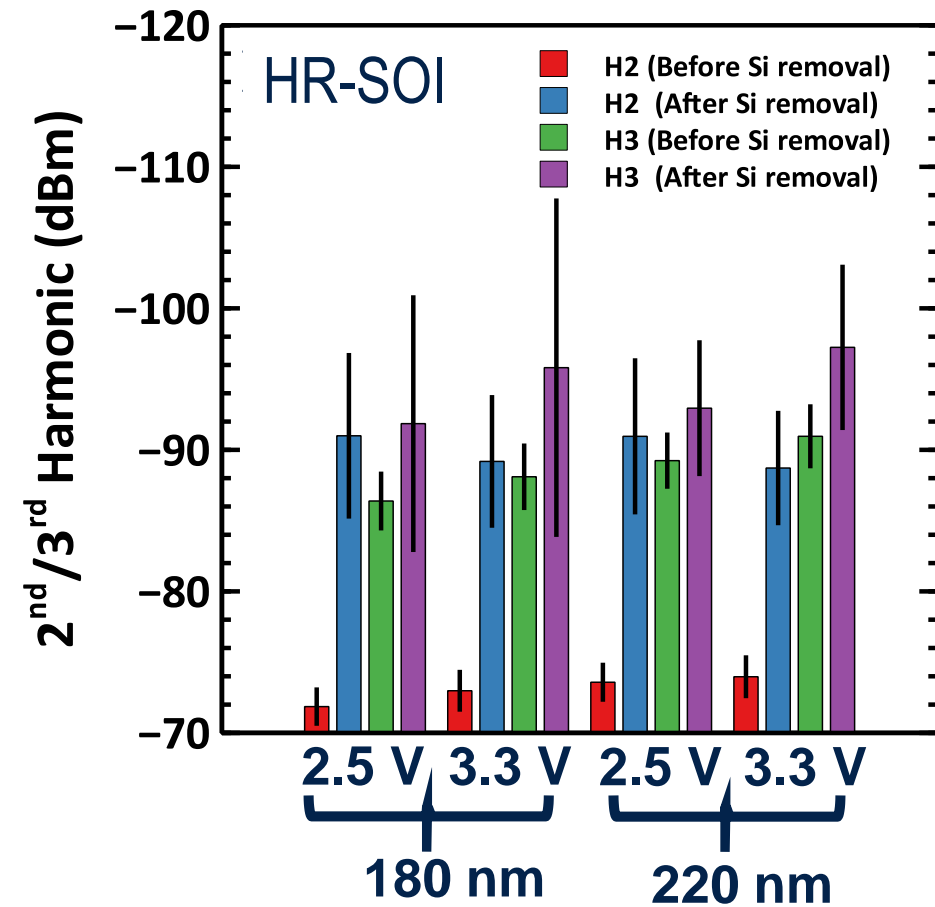
Improved RF SOI-CMOS switch : return losses

SP9T switch



Improved RF SOI-CMOS: large signal harmonic distortion

SP9T switch at fundamental $f=1\text{GHz}$



$L_g = 180\text{ nm}$

HR-SOI substrate

- H2 reduces by 22.7 dB
- H3 reduces by 5.6 dB

TR-SOI substrate

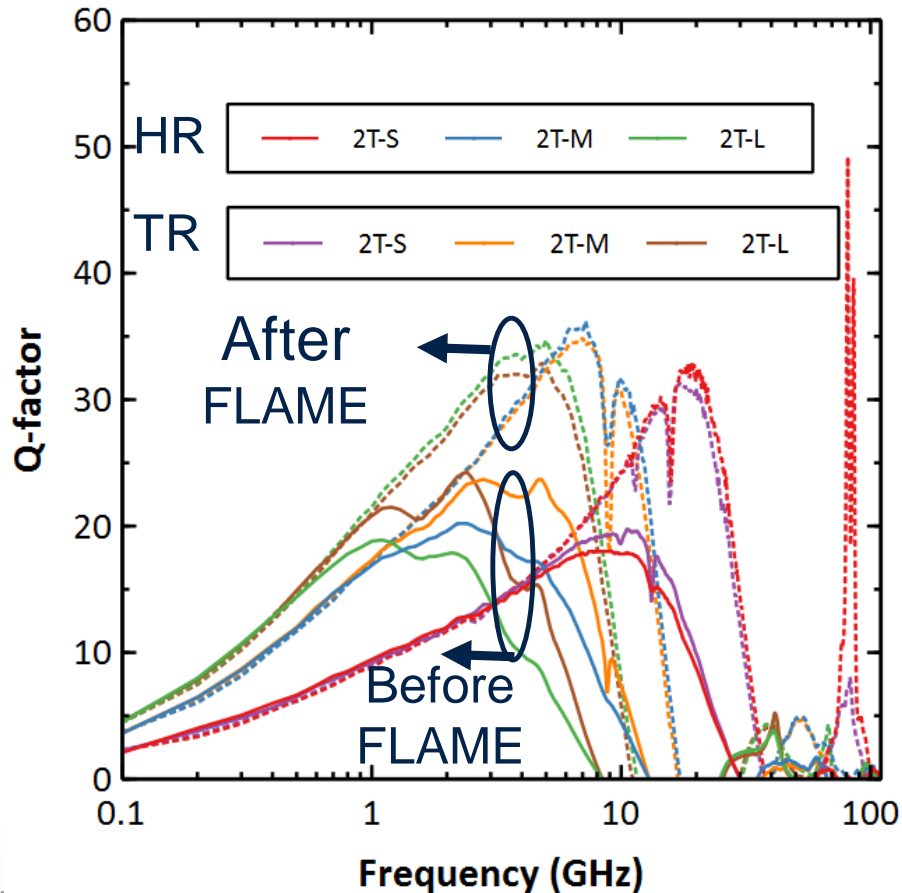
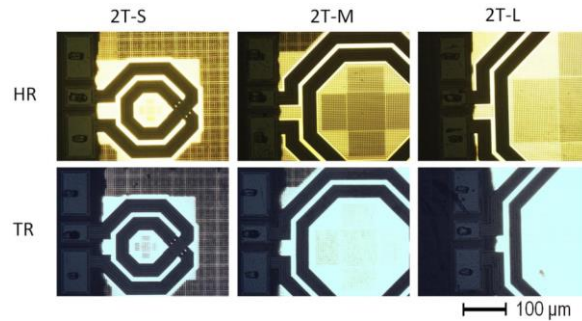
- H2 reduces by 7.8 dB
- H3 does not change

Improved RF SOI-CMOS: inductance Q-factor

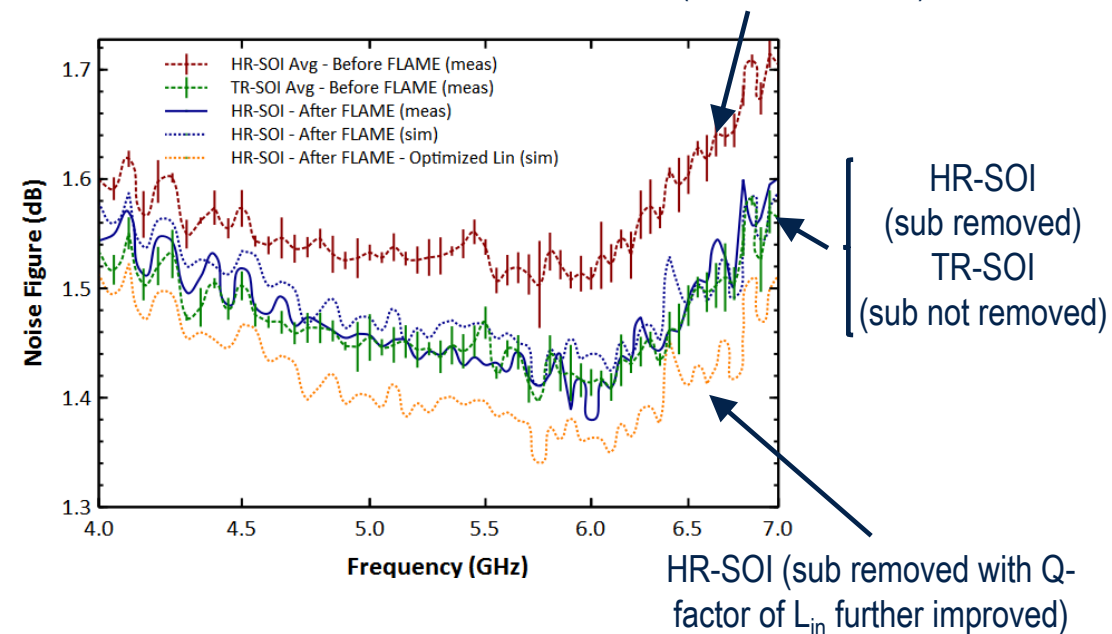
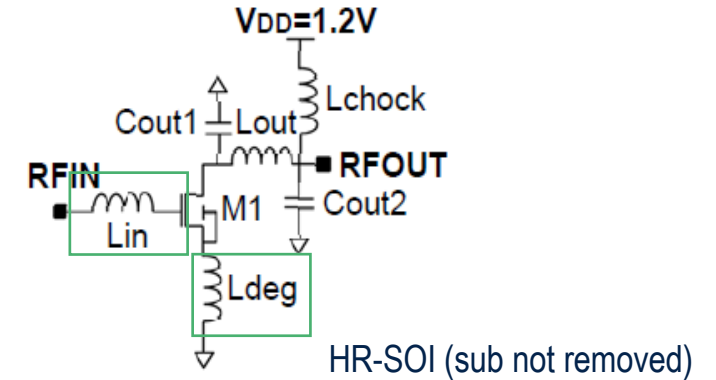
Q-factor improvement

$$Q_{SR}/Q_{TR} = 1.5$$

$$Q_{SR}/Q_{HR} = 1.8$$



Low Noise Amplifier
Noise Figure improvement



Summary

- Laser micromachining fully addresses the 1 μ m-1mm packaging range
- Functional Packaging fully takes advantages of laser techniques
 - Electro-optical interposer for Si-photonics applications
 - Optimal tool for microstructuring waveguides in the mmW and sub-THz bands
 - Substrate engineering to investigate ultimate performance of RF/mmW/photonics devices/circuits/systems

