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RESEARCH ARTICLE

A linear group delay filter with tunable positive slope for analog signal processing

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91192 Gif-sur-Yvette CEDEX.
Email: emilie.avignon@centralesupelec.fr**Summary**

This article describes the design of a tunable positive slope linear group delay filter dedicated to analog signal processing applications. The designed filter is composed of eight second-order all-pass cells which have been optimized to obtain a highly linear global group delay characteristic over a specified bandwidth for a specified dispersion. Each of these second-order cell is designed with a dedicated $G_m - C$ topology to fit the ideal group delay characteristic with a high efficiency. Based on the sensitivity analysis of the topology the possibility of tuning the group delay slope is highlighted. The design is achieved at transistor level with the ST CMOS 55nm technology and has a maximum bandwidth of 3 GHz, a maximum reachable delay of 4.45 ns, and a group delay swing of 3 ns. The positive slope of the group delay can be tuned in the range from 1.2 ns/GHz up to 1.4 ns/GHz.

KEYWORDS:

dispersive filter, phaser, analog signal processing, group delay

1 | INTRODUCTION

The dispersive filter is a device which is still rarely discussed in the electronic designer community. Most of the time, designers are trying to reduce the group delay dispersion in components and devices to avoid the creation of harmonic distortion in electronic systems. This is due to the fact that most of the receivers and transmitters nowadays are built on the idea that they are only dedicated to digital signal processing, with an analog front end only dedicated to the signal conditioning before the analog-to-digital conversion (low noise amplifiers, mixers, analog-to-digital converters) or dedicated to the amplification before transmission (digital-to-analog converter, power amplifier). However, a new research trend consists in rethinking the transceiver architectures in order to include Analog Signal Processing (ASP), and dispersive devices are a key component for such architectures¹.

Among possible real-time ASP application based on dispersive devices many of them concern spectrum analysis. They are referred as with various name in the bibliography, implying different properties. In the Real-Time Spectrum Sniffer (RTSS)^{2, 3}, the spectrum is decomposed into subchannels to identify if there is an activity in a communication channel or not. It requires a stepped group delay response. The Analog Chirp Fourier Transformer (ACFT)⁴ achieves a mathematical function close to the Fourier transform, meaning that the spectral resolution depends on the temporal window of observation. But contrary to the Fourier transform, and because of the time-frequency correspondence, the signals with the lowest frequency components will be represented in the spectrum with a poor resolution compared to the signals with the highest frequency component. Also, the spectral resolution will depend on the slope of the group delay characteristic of the dispersive filter in the ACFT architecture.

The Real-Time Spectrum Analyzer (RTSA)⁵, is based on the architecture of the ACFT itself coming from the family of the Multiply-Convolve-Multiply (M-C-M) architectures⁶.

Apart from spectral analysis, other ASP applications which requires dispersive devices, are Time-Stretching⁷ to potentially release the constraints on digitization, or Time-Reversal Mirror (TRM) for ultra-wideband communication⁸ or compressive receiver⁹. All these applications needs Linear Group Delay (LGD) devices which have been designed through very different kind of technology: with optical processes⁸, Surface Acoustic Wave (SAW) filters⁶, microstrip C-section structures¹⁰.

LGD devices are now also considered for integration in order to obtain compact, low-power, analog signal processors^{5, 7, 11, 12, 13}. The design of integrated LGD dispersive filters is mainly achieved in two steps. The first step is the mathematical synthesis to obtain an arbitrary group delay with a mastered amplitude. This aspect is not discussed in this article but the reader can refer to numerous works^{14, 15, 16}. The second step of the design of an integrated dispersive filter is the choice of integrated technology and topology: active or passive. For few-GHz applications, active topologies are more suitable as at these frequencies the sizes of passive components are prohibitive. Furthermore, an active topology allows tuning point to correct Process-Voltage-Temperature (PVT) variations, and more generally to tune certain properties. This was the main motivation to propose an integrated active topology of dispersive filter in this paper.

In this paper, we propose the design process of an integrated LGD dispersive filter with a dedicated $G_m - C$ topology which allows fitting of the optimized group delay characteristic and the proposition of tuning the group delay slope. To the best of authors' knowledge it is the first integrated dispersive filter with tunable group delay slope. This could be useful to significantly improve resolution in spectral analysis architecture in ASP. The designed filter is composed of eight second-order all-pass cells which have been optimized to obtain a highly linear global group delay characteristic over a prescribed bandwidth for a specified dispersion. The design is achieved by utilizing the ST CMOS 55nm technology to reach bandwidth of 3 GHz and a total group delay swing of 3 ns. Also, the positive slope of the group delay characteristic can be tuned between 1.2 ns/GHz up to 1.4 ns/GHz.

The paper is organized as follows. Section 2 proposes an all-pass second order Gm-C topology to fit the ideal group delay characteristic with a high efficiency. This section also provides the sensitivity analysis of the topology highlighting the possibility of tuning the slope of the group delay characteristic. Section 3 describes the LGD dispersive filter at transistor level, and section 4 shows simulation results of the dispersive filter in the frequency domain and in the time-domain. Section 5 brings final concluding remarks.

2 | PROPOSED SECOND ORDER ALL-PASS TOPOLOGY

2.1 | All-pass filters parameters

The dispersive filter presented in this article is composed of eight all-pass second order cells. The transfer function $T_i(s)$ of the i -th second order all-pass cell is:

$$T_i(s) = \frac{s^2 - \frac{\omega_{0i}}{Q_i}s + \omega_{0i}^2}{s^2 + \frac{\omega_{0i}}{Q_i}s + \omega_{0i}^2} \quad (1)$$

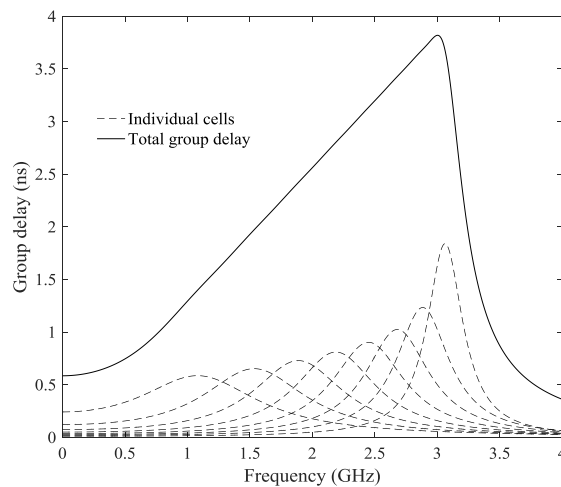
where ω_{0i} is the pole frequency and Q_i the pole-Q of the all-pass cell. The group delay associated to each cell has the following form:

$$\tau_i(\omega) = 2\omega_{0i}Q_i \frac{\omega^2 + \omega_{0i}^2}{\omega^2\omega_{0i}^2 + Q_i^2(\omega^2 - \omega_{0i}^2)^2} \quad (2)$$

If the eight cells have matched input and output impedances, the group delay of the cascade of these eight cells is the sum of the eight group delays. Thus, to obtain a linear group delay based on eight cells, it is mandatory to determine an optimal set of values for the pole frequencies f_{0i} ($\frac{\omega_{0i}}{2\pi}$) and the pole-Q Q_i . To do so, several methods have been published by now. Some mathematical approaches are either based on optimization with gradient-based approach^{14, 15}, or through evolutionary algorithm approach¹⁷ or on mathematical recursive calculation method¹⁶. In this work, a Newton-based optimization process is used aiming for dispersion of 3 ns over the bandwidth from 0.5 GHz up to 3 GHz and providing the set of values presented in Table 1 which consequently results in the group delay characteristic presented in Fig. 1.

TABLE 1 Set of optimized values

Cell i	f_{0i} (GHz)	Q_i
Cell 1	1.233	1.065
Cell 2	1.615	1.614
Cell 3	1.939	2.192
Cell 4	2.223	2.809
Cell 5	2.475	3.494
Cell 6	2.698	4.330
Cell 7	2.894	5.599
Cell 8	3.066	8.858

**FIGURE 1** Total group delay resulting of optimization with eight cells contribution

2.2 | Dimensioning methodology

The choice of topologies and technologies to achieve second order all-pass filters vary a lot depending on the frequency range of applications. Millimeter wave application down to 6 GHz applications leads preferably to passive topologies or one transistor LC topology¹⁸. Low gigahertz down to megahertz range application leads preferably to active inductorless implementation^{19, 20, 21}, because at these frequencies analog passive LC filters have a prohibitive size for integrated circuits, especially for large order filters. In this article the few-GHz frequency range is considered, which justifies the utilization of inductorless current-mode approach, i.e. a $G_m - C$ (transconductance-capacitor) architecture. If the transconductance circuit has a differential input and a single (or differential) output it is then a basic OTA (Operational Transconductance Amplifier). With such OTAs, the high level topology of the OTA-C filter can be obtained with the signal flow graph (SFG) based design²² or various other methods²³. In the case of SFG design the biquadratic filter would be composed of eight OTAs²². Then, the OTAs can be designed with one of the circuits proposed in²⁴, and dedicated to different requirement such as low power budget requirement^{25, 26}. Considering more complex OTA, i.e. with multiple outputs of the same sign has led to many new possibilities in terms of architecture synthesis²⁷. For a second-order all-pass filter, a relevant example of reduced components universal biquadratic filter is presented in²⁸. This example contains only two OTAs including four positive outputs. To obtain such an OTA with multiple outputs, a typical circuit is proposed in²⁹. It is composed of a differential pair and several common source stages at the output of the differential pair. When a significant number of common source stages are added at the output of the differential pair, the parasitic capacitance in the internal node of the OTA increases significantly. Then, there is a trade-off between the reduced complexity of the architecture and the expected bandwidth. It is worth mentioning also another type of current-mode filters, based on current conveyors. These

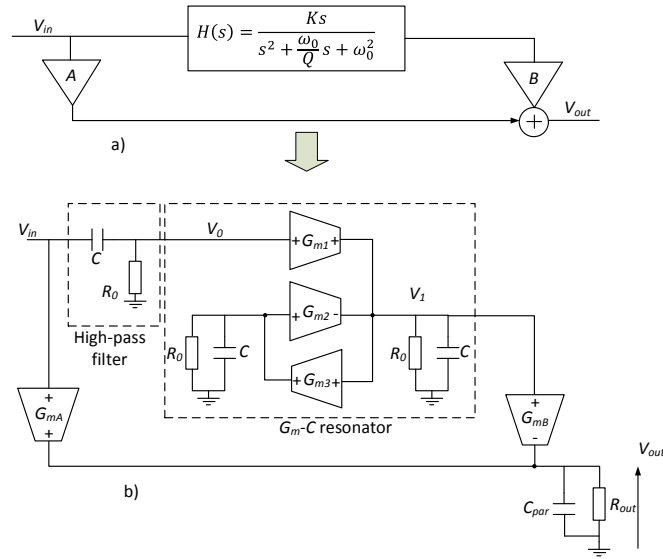


FIGURE 2 Proposed high level architecture, a) Block diagram view, b) Architectural view.

current conveyors are not tunable like traditional OTA through a bias current. Nevertheless the work in²⁰ shows the possibility to tune automatically the performances of an all-pass second-order delay network through a varying resistor implemented with N-channel MOS devices operating in the triode region inside the current conveyor.

In this work the purpose is to design second-order all-pass filters with relatively low values of pole-Q and a bandwidth as large as possible. It is then chosen to use a Gm-C resonator topology with limited quality factor as the main block. It has been extensively discussed in the literature that Gm-C resonator topology with limited output impedance of OTAs leads to limited value of the quality factor³⁰. To increase the quality factor there are several possibilities: increasing the output impedance of the OTA with a cascode topology²⁴ or adding an appropriate negative resistance at the output of the OTA with a control feedback²¹. In what follows, due to low values of pole-Q factor, instead of compensating the output impedance of the OTA we will simply use this property of limited Q-factor of the Gm-C resonator to obtain the required pole-Q for each cell. To do so the transconductances are loaded with appropriate values of R_0 (cf Fig.2 b), and the unwanted term is removed by a $C - R_0$ filter. Fig. 2. shows the decomposition of the all-pass second order filter using block diagram. The transfer function of this configuration is:

$$\frac{V_{out}}{V_{in}} = \frac{A \left(s^2 + \frac{\omega_0}{Q} s + \omega_0^2 \right) + BKs}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \quad (3)$$

To obtain a perfect second order all-pass filter, the transfer function introduced in (1) is needed, so A and B must be dimensioned the following way:

$$\begin{aligned} A &= 1 \\ B &= -\frac{1}{K} \left(\frac{2\omega_0}{Q} \right) \end{aligned} \quad (4)$$

The Figure 2. b) then shows the decomposition with a lower level of abstraction. To synthesize the transfer function $H(s)$, which is:

$$H(s) = \frac{Ks}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \quad (5)$$

a $G_m - C$ resonator is proposed. In a $G_m - C$ resonator the limited output impedance of the transconductances limits the quality factor. In the present case, the optimized values of pole-Q (Q_i) provided in Table 1 are moderate, so a resistor R_0 is added at the output of the transconductances to obtain the desired value of Q . The transfer function of the $G_m - C$ resonator shows that

we can obtain the wanted Q , thanks to R_0 , but a low-pass term also appears:

$$\frac{V_1(s)}{V_0(s)} = \frac{G_{m_1} R_0 (1 + R_0 C s)}{s^2 R_0^2 C^2 + 2 R_0 C s + (1 - R_0^2 G_{m_2} G_{m_3})} \quad (6)$$

This is the reason we propose adding of a high-pass filter composed of R_0 and C before the resonator, with the same values as in the resonator, which is shown in Fig. 2 b). In this way, we obtain the prescribed Q -factor at the specified frequency and the low-pass term is removed. The transfer function is then provided by (7).

$$\frac{V_{out}}{V_{in}} = R_{out} G_{mA} \left(\frac{s^2 + \left(\frac{2}{R_0 C} + \frac{G_{m_1} G_{mB}}{C G_{mA}} \right) s + \frac{1 - R_0^2 G_{m_2} G_{m_3}}{R_0^2 C^2}}{s^2 + \frac{2}{R_0 C} s + \frac{1 - R_0^2 G_{m_2} G_{m_3}}{R_0^2 C^2}} \right) \quad (7)$$

At this point the signs of different transconductances should be noted: $G_{mA} > 0$, $G_{m_1} > 0$, $G_{m_3} > 0$, $G_{m_2} < 0$ and $G_{mB} < 0$.

2.3 | Dimensioning methodology

By identifying equation (1) with equation (7), the second-order all-pass cell can be dimensioned with the following steps:

1. Dimensioning of the pole- Q : The expression of Q resulting from (1) and (7) is:

$$Q = \frac{\sqrt{1 - G_{m_2} G_{m_3} R_0^2}}{2} \quad (8)$$

Where G_{m_2} is < 0 . For implementation simplicity R_0 should be chosen smaller than few $k\Omega$. For that matter, a strategy to improve the output impedance as in²¹ is not necessary, because R_0 will be much less than the output impedance. After choosing the appropriate R_0 value, the product of G_{m_2} and G_{m_3} is then deduced.

2. Dimensioning of the pole frequency: The expression of pole frequency resulting from (1) and (7) is:

$$\omega_0^2 = \frac{1 - G_{m_2} G_{m_3} R_0^2}{R_0^2 C^2} \quad (9)$$

The $G_{m_2} G_{m_3}$ product and R_0 have been fixed in the previous step. So theoretically only C has to be determined. But it should be noticed at this point that there is an important dimensioning trade-off between power consumption, area and sensitivity to parasitics. If the $G_{m_2} G_{m_3}$ product is large it leads to a large power consumption with a greater value of C leading to a larger implementation area but less sensitive to layout parasitics. And if the $G_{m_2} G_{m_3}$ product is small, it reduces power consumption and area, but makes the circuits more vulnerable to layout parasitics.

3. Dimensioning of the numerator: To insure a true all-pass behavior the even term of 's' in the numerator must have the opposite sign as the even term of 's' in the denominator. From equation (7), it is obtained with the following condition:

$$\frac{G_{m_1} G_{mB}}{G_{mA}} = -\frac{4}{R_0} \quad (10)$$

where $G_{mB} < 0$. Based on this dimensioning process, a set of values of transconductance G_{mB} , R_0 and C is proposed in Table 2. The product $G_{m_2} G_{m_3}$ is considered fixed for all the cells and can be implemented with an infinity of combinations of G_{m_2} and G_{m_3} . Here it is fixed equal to $-9mS^2$. Then it could be $G_{m_2} = -3mS$ and $G_{m_3} = 3mS$ or $G_{m_2} = -1.75mS$ and $G_{m_3} = 5.14mS$ or any other combination providing a product of $-9mS^2$. Further, in this dimensioning $G_{mA} = G_{m_1} = 1mS$ and $R_{out} = 1k\Omega$ have been fixed for all the cells. The value of R_{out} must be chosen sufficiently low to keep the expected bandwidth, due to the presence of parasitic capacitance at the output node C_{par} (presented in Fig. 2).

TABLE 2 High level dimensioning of $G_m - C$ all-pass cells

Cell i	R_0 (Ω)	C (fF)	G_{mB} (mS)
Cell 1	627.3	438.4	-6.4
Cell 2	1023	310.8	-3.9
Cell 3	1423	252.8	-2.8
Cell 4	1843	218.2	-2.2
Cell 5	2305.5	194.9	-1.7
Cell 6	2868	178.1	-1.4
Cell 7	3717	165.6	-1.1
Cell 8	5896	155.9	-0.678

2.4 | High level sensitivity analysis

Theoretically the previous dimensioning allows to obtain the prescribed group delay characteristic as well as an all-pass magnitude. But practically, due to layout parasitic, process, voltage and temperature variation (PVT) the performances will change. In what follows it is analyzed the sensitivity of the topology to parameters variation (G_{m1} , G_{m2} , G_{m3} , G_{mA} , G_{mB}), to determine how these variations impact one cell performance and the cascaded eight-cell performances. The two main performances in our case are the group delay and the magnitude of the filter. The complete expression of the group delay of the topology given in Fig. 2 is provided by (11). But as long as the condition expressed by (10) is fulfilled, then expression of the group delay is given by (12). The expression of the magnitude can be obtained directly from (7).

In what follows we propose a high-level sensitivity analysis based on the dimensioning of the eight cells proposed in Table 2. This sensitivity analysis focuses transconductance variation. In a circuit, when the voltage supply (V_{DD}) is higher than nominal, or if both transistors (NMOS and PMOS) have lower values of threshold voltage (V_{tN} and V_{tP}) than predicted, it results in higher values of transconductances than predicted. On the contrary, if we have a smaller V_{DD} than nominal or the threshold voltages higher than nominal, it results in smaller values of transconductances. In what comes next, to better understand the impact of variation, we consider first the variation of $\pm 20\%$ of G_{m2} and G_{m3} which are identical for all the cells, and then the variation of $\pm 20\%$ for G_{mB} for each cell.

2.4.1 | Sensitivity to G_{m2} and G_{m3} variation

If the condition in (10) is fulfilled, the equation of the group delay is given by (12). In that case, it appears from equations (12) and (7) that the variation of G_{m2} and G_{m3} will impact only the group delay but not the magnitude response of the filter. A $+20\%$ and -20% variations are applied on both $|G_{m2}|$ and $|G_{m3}|$ in the same time. Figure 3 shows the evolution of the group delay characteristic with the variations of G_{m2} and G_{m3} . When $|G_{m2}|$ and $|G_{m3}|$ are greater than nominal, the frequency f_0 of each cell increases and the quality factors Q of each cell decreases. As a result, the bandwidth of the total group delay increases and the dispersion decreases. When $|G_{m2}|$ and $|G_{m3}|$ are smaller than nominal, the frequency f_0 of each cell decreases and the pole-Q Q_i increases. As a result, the bandwidth of the total group delay decreases and the dispersion increases. To evaluate linearity error, we did a linear fitting and plotted the difference between the obtained linear characteristic and the filter group delay characteristic (see Fig. 4). A difference of $50ps$ is tolerated between the fitted linear characteristic and the filter group delay

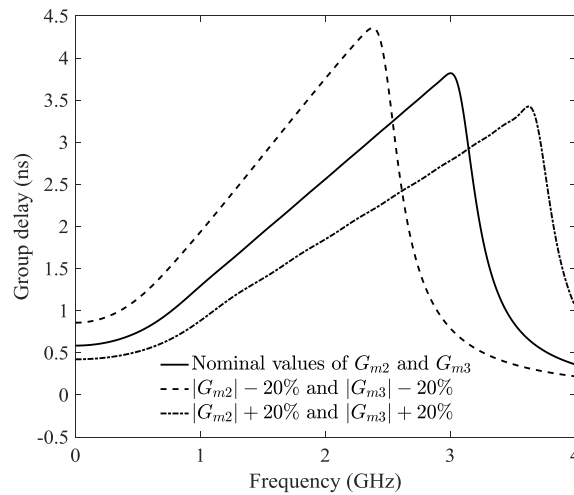
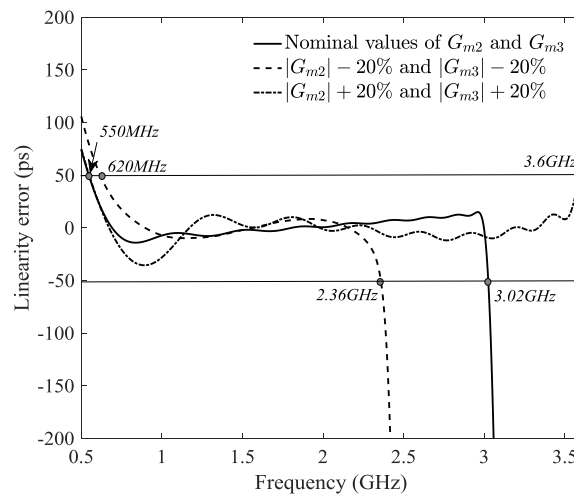
$$gd(\omega) = \frac{\rho\mu R_0 (1 - \sigma + \rho^2\omega^2) (-2\rho^2\mu R_0\omega^2 + G_{mA} (1 + \sigma^2 - 6\rho^2\omega^2 + \rho^4\omega^4 + 2\sigma(-1 + \rho^2\omega^2)))}{(\sigma^2 + 2\sigma(-1 + \rho^2\omega^2) + (1 + \rho^2\omega^2)^2) (4\rho^2 G_{mA}\mu R_0\omega^2 + C^2\mu^2\omega^2 + G_{mA}^2 (\sigma^2 + 2\sigma(-1 + \rho^2\omega^2) + (1 + \rho^2\omega^2)^2))} \quad (11)$$

where : $\rho = R_0C$, $\sigma = G_{m2}G_{m3}R_0^2$ and $\mu = G_{m1}G_{mB}$

$$gd(\omega) = \frac{4CR_0 (1 - G_{m2}G_{m3}R_0^2 + C^2R_0^2\omega^2)}{G_{m2}^2 G_{m3}^2 R_0^4 + 2G_{m2}G_{m3}R_0^2 (-1 + C^2R_0^2\omega^2) + (1 + C^2R_0^2\omega^2)^2} \quad (12)$$

TABLE 3 Group delay performances for G_{m2} and G_{m3} variations

	Nominal G_{m2} and G_{m3}	$ G_{m2} + 20\%$ $ G_{m3} + 20\%$	$ G_{m2} - 20\%$ $ G_{m3} - 20\%$
Slope (ns/GHz)	1.3	0.94	1.8
Bandwidth (GHz)	[0.55-3.2]	[0.55-3.6]	[0.62-2.36]

**FIGURE 3** Group delay characteristic with G_{m2} and G_{m3} variation**FIGURE 4** Absolute linearity error on the group delay with G_{m2} and G_{m3} variation

characteristic, it leads to the bandwidths listed in Table 3, together with the slopes of the group delay. These results highlight the possibility of tuning the slope of the group delay characteristic on a certain range without damaging the linearity.

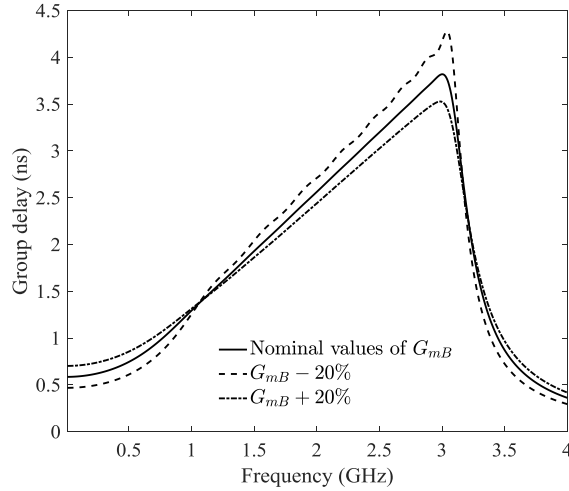


FIGURE 5 Group delay characteristic with G_{mB} variation

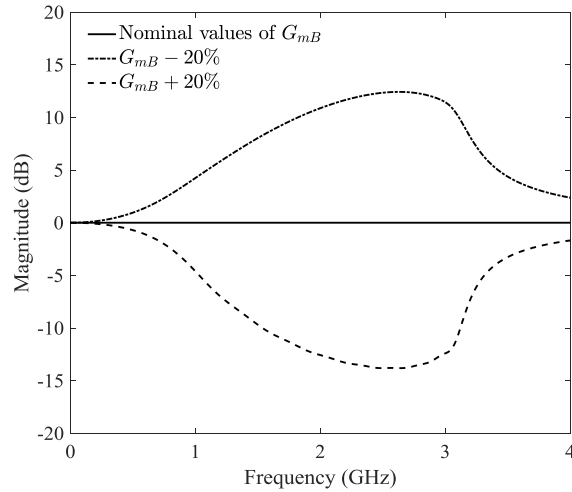


FIGURE 6 Magnitude of the filter with G_{mB} variation

2.4.2 | Sensitivity to G_{mA} , G_{mB} and G_{m1} variation

In this scenario, it cannot be considered that condition (10) is fulfilled, due to the variation of one of the parameter G_{mA} , G_{mB} or G_{m1} . Then, the complete expression of the group delay given by (11) must be considered. For sensitivity analysis, we consider a variation of $\pm 20\%$ on G_{mB} . From (11) and (7) it can be seen that it will impacts the group delay as well as the magnitude response of the global filter. Figure 5 shows the group delay characteristic with variations of G_{mB} and Fig. 6 shows the global magnitude response of the filter varying with G_{mB} . For G_{mB} variations, the slope of the group delay characteristic changes, but unfortunately the magnitude of the filter also changes significantly. So, G_{mA} , G_{mB} and G_{m1} could not be used as tuning parameters for the slope of the group delay. On the contrary, these parameters should remain as close as possible to the nominal values in order to keep a flat magnitude.

2.5 | Discussion on variations and tuning

The implementation of $G_m - C$ topology or more generally active inductorless implementation are subjected to PVT variations and need a strategy to compensate for the effect of these variations. Several of these strategies have been published already.

In [19], in the same context of an active implementation of a second-order all-pass filter for analog signal processing, a post-production tuning mechanism, based on an automated local optimiser, compensate for CMOS process variation. More generally, for the stabilisation of G_m values regarding PVT variations, some strategies are based on a feedback control loop. Variations are measured, for example across an off-chip resistor and will allow to adjust a biasing voltage or current thanks to the feedback, as for example in [30]. In what follows in this work, the PVT variations are corrected manually with a tuning voltage, provided that one of the previous strategy could be implemented in a similar way. Also, based on the results on the sensitivity to G_{m2} and G_{m3} , a tuning voltage on G_{m2} will be used to adjust the slope of the group delay characteristic.

3 | TRANSISTOR LEVEL CIRCUIT DESCRIPTION

All the circuits described below have been designed with the ST CMOS 55nm technology. The transistors used for all circuits are the plvtlp and nlvtlp, which are low V_t (threshold voltage) transistors. The voltage supply (V_{DD}) is 1.2V. For each block, transistors sizes are provided on the schematic with (W/L) in μm . This section discusses the design of negative transconductors (G_{m2} , G_{mB}), positive transconductors (G_{m1} , G_{m3} , G_{mA}) and presents the results obtained for the all-pass cells with the previous transconductors. From the theory of analog circuit design it is known that using topologies with several transistor stages leads to a reduced bandwidth because of the successive grounded parasitic capacitances creating poles. The well-known Miller OTA, composed of two stages, leads to difficult gain-bandwidth tradeoff to reach few GHz bandwidth whatever the integrated technology. In order to reach a 3 GHz bandwidth, one-stage topologies have been preferred, when possible. The idea of using one-stage inverter based OTA has been introduced by Nauta in early nineties³¹. Despite their very high transconductance efficiency and bandwidth capability, inverter-based OTA are susceptible to process, voltage and temperature variation. To benefit the prescribed properties while remaining robust to variation is still an interesting subject discussed in state-of-the art^{32, 31, 33}. The approach we propose here for the design of the transconductors is to have tuning voltages to tune the values of transconductances. Moderate values of transconductance are achieved with one-stage when large values of transconductance are achieved with several stages in accordance with the gain-bandwidth trade-off. For PVT variations, we consider the usual process corners, namely: FF (Fast NMOS, Fast PMOS), SS (Slow NMOS, slow PMOS), FS (Fast NMOS, Slow PMOS), SF (Slow NMOS, Fast PMOS). Nominal case is typical (TT). For voltage variation, we consider the voltage supply (V_{DD}) with a +/- 10% variation. And for the temperature, we consider: 27°C, 0°C, 85°C.

3.1 | Tunable negative transconductors

The negative transconductor circuit is presented in Fig. 7. Transistors sizes for G_{m2} and G_{mB} are provided on the schematic. In this circuit M3 and M4 compose the inverter-based OTA. They are dimensioned to obtain the wanted order of magnitude of transconductance with an output around $V_{DD}/2$. M2 and M5 are biased in the ohmic region resulting in an equivalent resistor given by:

$$r_{on} = \frac{1}{g_{mM2}} = \frac{1}{g_{mM5}} \quad (13)$$

If V_C increases, g_{mM5} increases and M5 will absorb more current. If V_{SG2} is also equal to V_C , then g_{mM2} increases equally leading to more bias current and a greater transconductance value with a constant bias point at the output. To get V_{SG2} equal to V_C , M6 must be dimensioned properly, ie. to obtain approximately $V_{D1} = V_{DD} - V_C$. Transistor sizes are provided in the Fig. 7. The load is the R_0C tank from the architecture. R_0 is implemented with two $2R_0$ in parallel connected to the voltage supply and the ground. This way the resistors help maintaining the bias point, at the cost of increasing power consumption.

The bandwidth of the negative tunable transconductor is evaluated (without the load) with several control voltage V_C and is presented in Fig. 8 a). From the figure, where the absolute value of transconductance G_m is presented, it appears that the value of the transconductance is maintained up to 3 GHz and further. In figure 8 b), the DC characteristic of the circuit is presented. For $V_C = 800mV$ the bias current is $I_{B0} = 145.1\mu A$ to obtain $G_m = -1.42$ mS. For $V_C = 900mV$ the bias current is $I_{B0} = 155.9\mu A$ to obtain $G_m = -1.59$ mS. For $V_C = 1V$, the bias current is $I_{B0} = 162\mu A$ to obtain $G_m = -1.68$ mS. Power consumption of this tunable transconductor is $194 \mu W$ for the right branch and 1 mW for the left branch leading to a total of 1.2 mW.

The process corner simulation in DC is presented in figure 9 a). The FF corner leads to a greater of transconductance value than typical, when SS corner leads to a lowest value of transconductance than typical but the bias point is maintained (600 mV as in the typical case). On the contrary, FS corner leads to a bias point shifted to the right (about 660 mV) and SF corner leads to a corner shifted to the left (about 540 mV). The DC simulations of the transconductor with V_{DD} variation and temperature

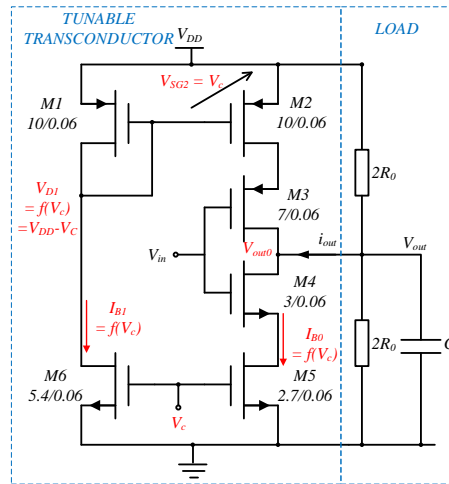


FIGURE 7 Tunable negative transconductor. Transistors sizes are provided on the schematic with (W/L) in μm .

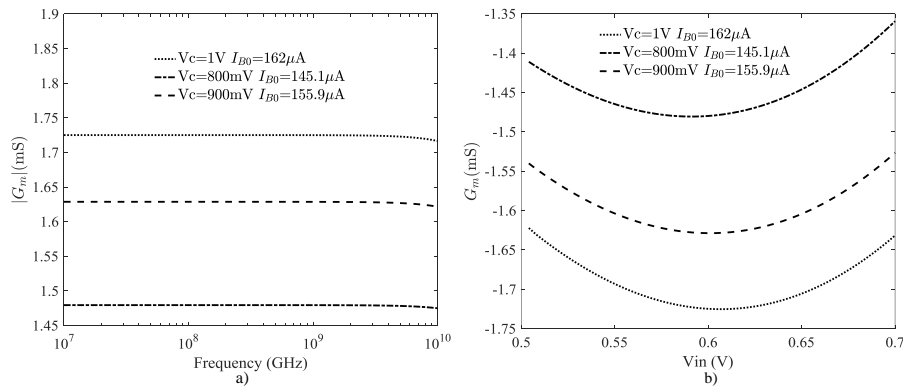


FIGURE 8 a) bandwidth of the negative transconductor with several tuning voltages b) DC characteristics of the transconductors with several tuning voltages.

variation are presented in figure 9 b). At the lowest temperature (0°C), the transconductance has the highest value and the lowest value at 85°C . The bias is unchanged and the value of G_m can be tuned by V_C . With V_{DD} variation, bias point and values are changing. We assume in what follows that the values can be tuned and that the transconductance is quasi-constant between 0.5V and 0.7V at the input.

3.2 | Tunable positive transconductors

One transistor stage does not allow to create a positive transconductance. To obtain a positive transconductance at least two stages are necessary. In that case there is a risk to reduce the bandwidth at intermediary nodes. To keep the bandwidth as high as possible for a wanted value of gain the output impedance of the first stage should be reduced. It is here proposed to manage the transconductance value, the bandwidth as well as the bias point with the schematic proposed in Fig. 10. Transistors sizes for G_{m1} and G_{m3} are provided on the schematic. For G_{mA} , transistors sizes (W/L) in μm are: 1.2/0.06 for M1p, M3p, M5p and 0.58/0.06 for M2p, M4p, M6p. In this schematic the output impedance of the first inverter based OTA will be limited to the half value of the transistors M3p and M4p biased in the triode region. When increasing V, the equivalent resistors of M3p and M4p decreases and then decreases the output impedance of the first stage and consequently the gain. On the contrary of the gain, the bandwidth is increased. To maintain the bias point, it would be necessary in certain situation to impose a bias V_2 larger than $V_{DD} - V$ (typically in SF corner) or smaller than $V_{DD} - V$ (in FS corner). This aspect is illustrated later in this paragraph.

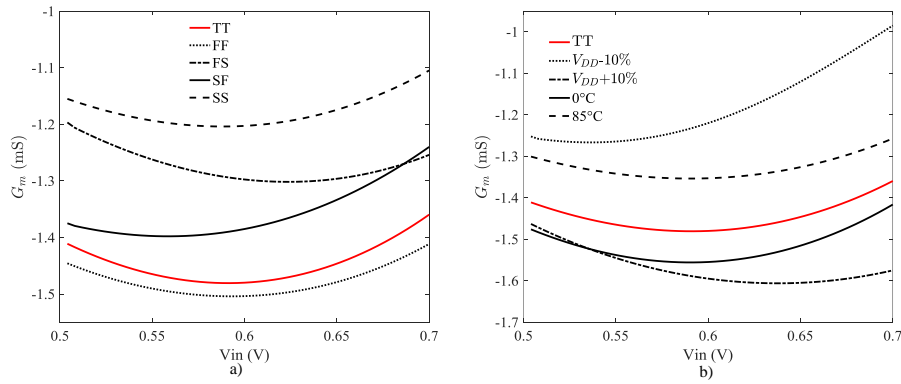


FIGURE 9 PVT variation of tunable negative transconductor a) process corner variation b) Temperature and supply variation.

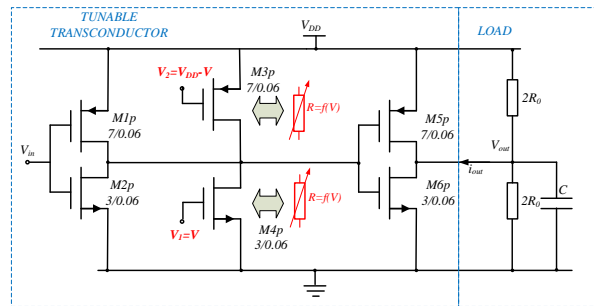


FIGURE 10 Circuit of the tunable positive transconductor. Transistors sizes are provided on the schematic with (W/L) in μm .

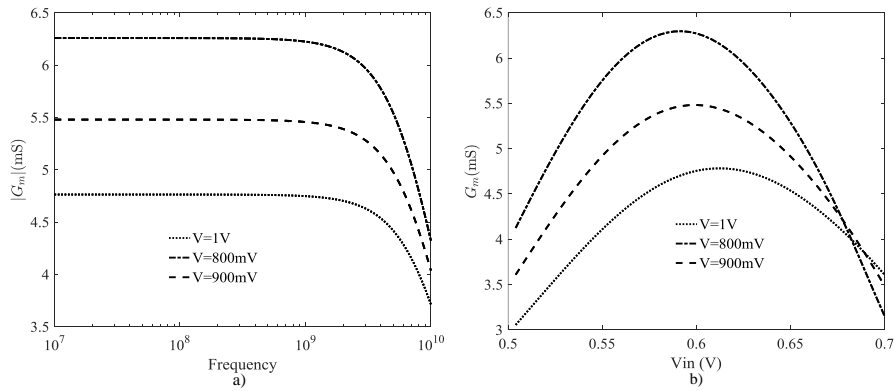


FIGURE 11 Tunable positive transconductor a) bandwidth of the transconductor b) DC characteristics of the transconductors

Figure 11 presents the performances of the positive tunable transconductor. The bandwidth of the positive tunable transconductor is evaluated (without the load) with several control voltage in Fig. 11 a). The bandwidth is reduced compared to the obtained for the negative transconductor. This is due to the necessity of two stages. Nevertheless, the value of the transconductance remains quite constant up to 3 GHz, it will consists in the limit for our design. With the tuning voltage V varying from 800 mV up to 1 V, the values of transconductances are comprised in the range from 4.8 mS up to 6.2 mS.

The process corner simulation in DC of the positive tunable transconductor is presented in Fig. 12 a). The FF corner leads to a greater of transconductance value than typical, when SS corner leads to a lowest value of transconductance than typical but the bias point is maintained ($600mV$ as in the typical case). In these cases $V_1 = V$ and $V_2 = V_{DD} - V$. In the FS and SF corner,

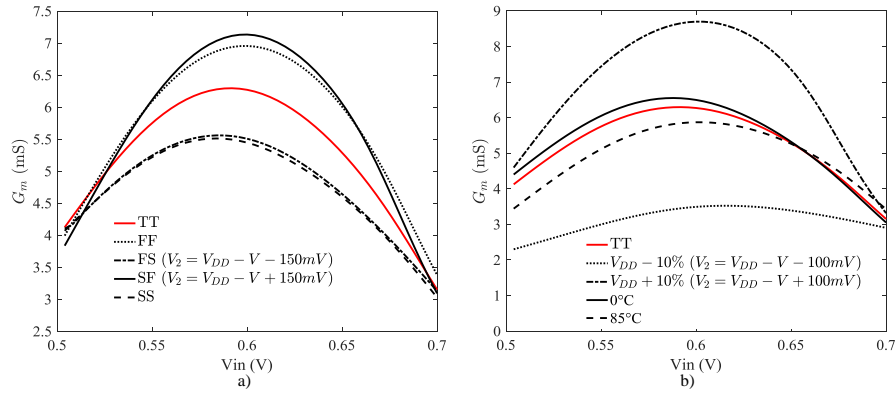


FIGURE 12 PVT variation of tunable positive transconductor a) process corner variation b) Temperature and supply variation

it has been necessary to select V_2 different of $V_{DD} - V$ to mitigate the bias point deviation as indicated in the figure. The DC simulations of the positive transconductor with V_{DD} variation and temperature variation are presented in figure 12 b). At the lowest temperature (0°C), the transconductance has the highest value and the lowest value at 85°C . With V_{DD} variation, bias point and values are changing and it could be mitigated the same way as for SF and FS corner bias point mitigation, with the value of V_2 .

3.3 | Complete second-order cell

The complete second order all pass cell is composed of the positive and negative transconductors described in the previous sections. For all the cells, the same transconductor blocks will be used, only the values of R_0 and C and tuning voltages will change. All cell's parameters are summarized in Table 5. The group delay characteristics obtained with this circuit for all the cells are presented in Fig. 13. All cell's characteristics obtained in nominal case at transistor level (TT) are very close to the ideal optimized group delay characteristics. Furthermore with an appropriate tuning of the voltages summarized in Table 4 the deviation from the nominal case is very small as presented in the inset in Fig. 13 for the first cell. For the FF corner, all the values of transconductances are greater than expected, resulting in a higher frequency of the group delay and a decreased pole-Q (see section 2). So the applied tuning voltages decrease all the values of the transconductances. For a SS corner, transconductances values are smaller than expected and the tuning voltages make them increase. For FS and SF corners the applied tuning voltages are not symmetrical (a 150 mV difference is applied) to set back the bias point and the values of transconductances. The magnitudes of all cells are presented in Fig. 14. The magnitude is not perfectly flat, due to the very high sensitivity to G_{mA} , G_{mB} , G_{m1} variation. A very small deviation of transconductance value (0.2mS) results in a significantly changed magnitude (see section 2). The impact of the deviation due to corner for cell 1 on the magnitude (with appropriate provided in Table 4) is presented in the inset of Fig. 14.

4 | SIMULATION RESULTS

The optimization process considers that the global group delay of the dispersive filter is the sum of all group delays of each all-pass cell. This is true only under matching conditions. For example, with passive networks input and output impedances are the same, most of the time $50\ \Omega$. If these passive networks are cascaded, the resulting group delay will be the sum of group delays of each passive network. In the general case of $Gm-C$ filters, the input impedance tends to infinity and the output impedance on transistors drain would be very large, so matching conditions would be fulfilled. To cascade the eight cells previously discussed, a buffer is needed because we have a large output impedance due to R_{out} which must be connected to the high-pass filter composed

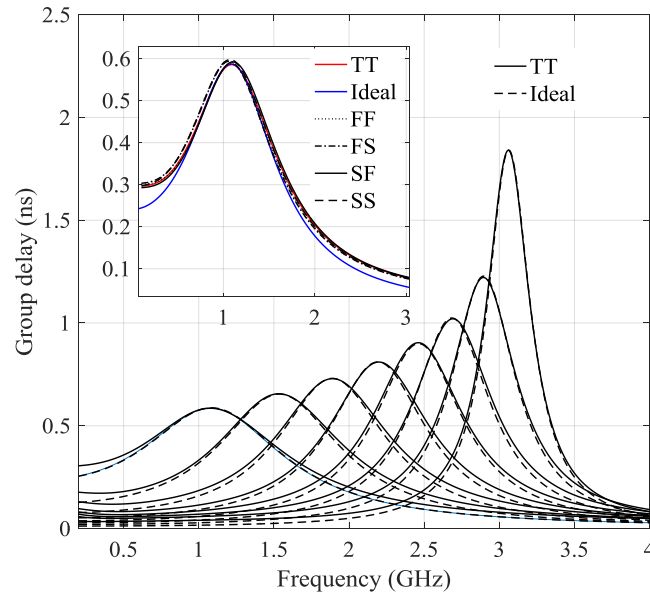


FIGURE 13 Group delay of all the cells in nominal case (TT) compared to wanted group delay (ideal). In the inset: group delay of cell 1 with process corner

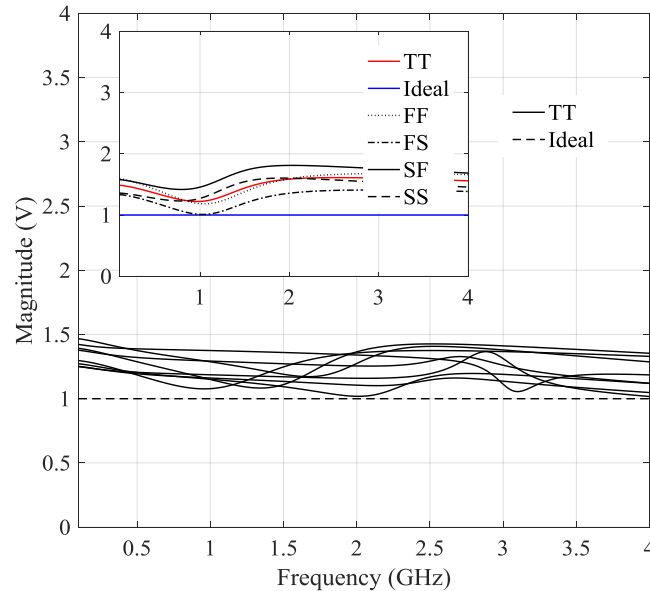


FIGURE 14 Magnitude of all the cells in nominal case (TT) compared to wanted group delay (ideal). In the inset: magnitude of cell 1 with process corner

of C and R_0 . If the buffer is not introduced the signal will be attenuated by the low-pass resulting filter $R_{out}C$. This is why a buffer composed of a circuit identical to G_{m1} with two resistors of 150Ω connected at the output between ground and V_{DD} is introduced between each cell. With an output impedance of 75Ω it is compatible with the high-pass filter $C - R_0$. Also the buffers have been dimensioned to have a gain greater than one. For biasing concern, a high-pass is introduced between each cell. It is composed of a 2pF capacitor and two diode connected PMOS transistors to create two active load connected between V_{DD} and the ground. Sizes of these PMOS transistors are $W = L = 0.135 \mu\text{m}$. In terms of power consumption, each cell consumes

TABLE 4 Cell1: Tuning voltages for process corners

Voltages	TT	FF	SS	FS	SF
V_1 (mV)	925	970	800	925	925
V_{1b} (mV)	$V_{DD} - V_1$	$V_{DD} - V_1$	$V_{DD} - V_1$	$V_{DD} - V_1 - 150\text{mV}$	$V_{DD} - V_1 + 150\text{mV}$
V_2 (mV)	750	700	900	750	750
V_3 (mV)	860	1000	750	860	860
V_{3b} (mV)	$V_{DD} - V_3$	$V_{DD} - V_3$	$V_{DD} - V_3$	$V_{DD} - V_3 - 150\text{mV}$	$V_{DD} - V_3 + 150\text{mV}$
V_A (mV)	1200	1200	1200	1200	1200
V_{Ab} (mV)	$V_{DD} - V_A$	$V_{DD} - V_A$	$V_{DD} - V_A$	$V_{DD} - V_A - 150\text{mV}$	$V_{DD} - V_A + 150\text{mV}$
V_B (mV)	980	800	980	980	980

TABLE 5 All cell's parameters

Cell number	V_A (mV)	V_B (mV)	V_1 (mV)	V_2 (mV)	V_3 (mV)	$2R_0$ (k Ω)	C (fF)
1	1200	980	925	750	860	1.2	435
2	980	850	950	750	860	2	305
3	800	780	950	750	860	2.8	245
4	740	640	950	750	860	3.6	205
5	740	640	1100	750	860	4.6	180
6	700	585	1100	750	870	5.73	160
7	700	535	1100	750	875	7.43	145
8	700	515	1200	750	920	11.7	130

TABLE 6 Comparison of state of the art integrated linear group delay filters.

	Xiang et al. ^{7*}	Xiang et al. ^{5*}	Xiang et al. ^{13*}	Avignon et al. ¹¹	Ferreira et al. ¹² (Lattice)	Ferreira et al. ¹² (Bridge-T)	This work
Technology	CMOS 0.13 μm	CMOS 0.13 μm	CMOS 0.13 μm	BiCMOS 0.13 μm	BiCMOS 0.13 μm	BiCMOS 0.13 μm	CMOS 55nm
Frequency range	12-16 GHz	0.4-4GHz	11-15 GHz	0.8-2.5 GHz	0-3.5 GHz	0-3.5 GHz	0.5-3 GHz
Power consumption	Active, N.A.	750 mW	Active, N.A.	7.2 mW	Passive	Passive	107 mW
Group delay swing	1 ns	1.2 ns	0.8 ns	3 ns	0.33 ns	60 ps	3 ns
Slope's tunability	No	No	No	No	No	No	Yes
Group delay slope	+0.375 ns/GHz	-0.3 ns/GHz	+0.2 ns/GHz	-1 ns/GHz	-0.11 ns/GHz	+20 ps/GHz	+1.2 ns/GHz upto + 1.4 ns/GHz

* Measured results.

about 9 mW and each buffer 5 mW. A large part of the buffer power consumption originates from two resistors of 150 Ω between ground and V_{DD} . It consumes 4 mW. The complete power consumption of the circuit is then 107 mW.

4.1 | AC simulation results

The first objective of this design is to obtain a linear group delay characteristic for ASP applications. As a second objective, it has been seen in section 2 in high level sensitivity analysis, that it is possible to tune the slope of this group delay characteristic by changing only G_{m2} , G_{m3} or the product $G_{m2}G_{m3}$. In what follows, all voltages presented in Table 5 will remain fixed, when V_2 will change to make G_{m2} vary. The result is presented in Fig. 15. For $V_2 = 660\text{mV}$, the obtained slope is 1.4 ns/GHz, for $V_2 = 720\text{mV}$, it is 1.3 ns/GHz and for $V_2 = 780\text{mV}$, it is 1.2 ns/GHz. To define the useful bandwidth of the linear group delay filter, we will tolerate a linearity error up to 60 ps between the group delay characteristic and a linear characteristic obtained by

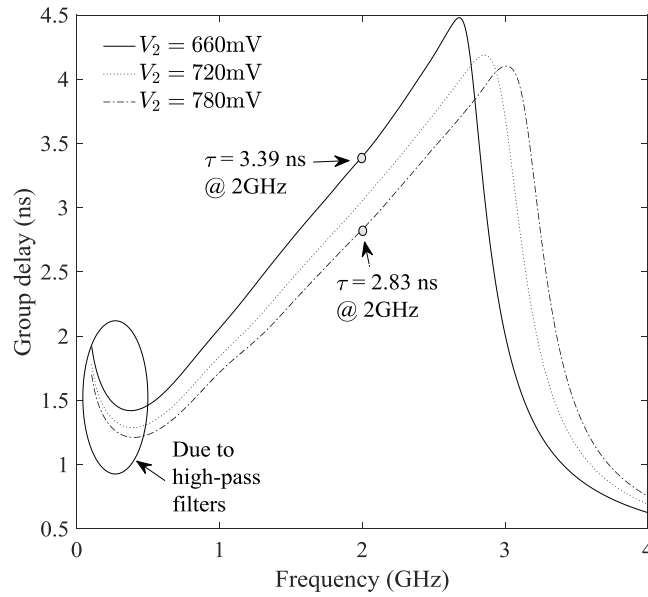


FIGURE 15 Group delay characteristic for several tuning voltages V_2

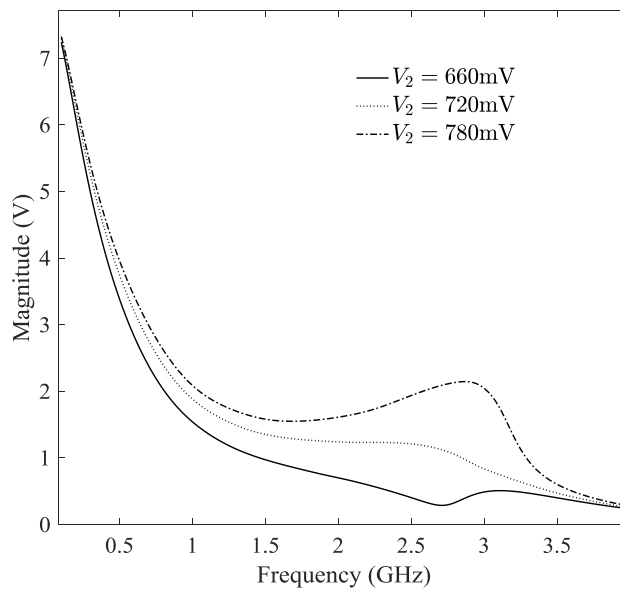


FIGURE 16 Magnitude response for several tuning voltages V_2

fitting the data. With this linearity error the bandwidth is [0.5 -2.6] GHz for $V_2 = 660\text{mV}$, [0.5 -2.85] GHz for $V_2 = 720\text{mV}$, and [0.5 -3] GHz for $V_2 = 780\text{mV}$.

When changing V_2 , the magnitude changes, contrary to what is predicted in section 2 (see Fig. 16). It is justify by the fact that for a change in V_2 all biasing points slightly changes leading in a change of transconductances values of G_{mA} , G_{mB} and G_{m1} leading to a change in the magnitude. Consequently, an improvement of this work could be to control thoroughly the bias point to obtain better tuning possibility.

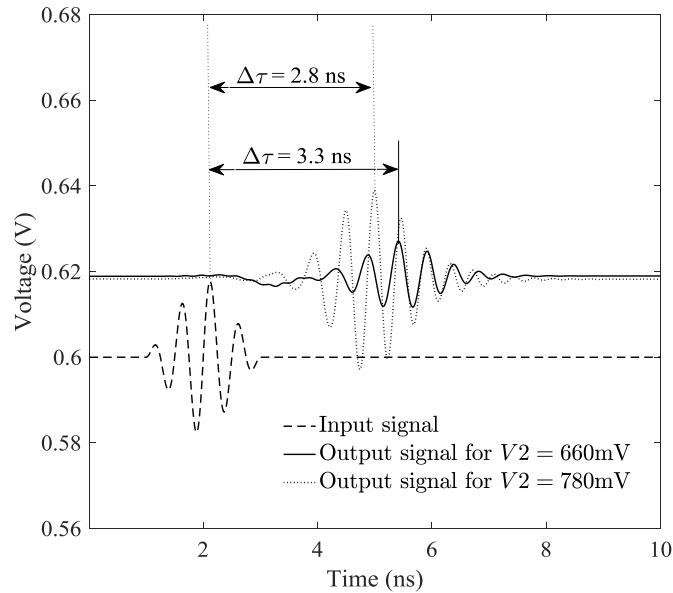


FIGURE 17 Time domain simulation results of the dispersive filter for an input sine wave of 2GHz and two tuning voltages: $V_2 = 660\text{mV}$ and $V_2 = 780\text{mV}$

4.2 | Time domain simulation results

To verify the group delay characteristic in the time domain it is not possible to simply apply a sinusoidal signal to observe the delay at the output. This is because the period of the signal (for instance 0.5 ns for 2 GHz) is smaller than the corresponding group delay (for instance $\tau = 2.8\text{ns}$ at 2 GHz). So to clearly identify the group delay for each frequency, we apply a sinusoidal signal multiplied by a triangular waveform. Here we choose to multiply a 10 mV amplitude sinusoidal signal at 2GHz with a triangular wave starting at 1ns with 1ns rise time and 1ns fall time. To define the group delay corresponding to the frequency of the sinusoidal signal, we calculate the time difference between the two peaks of the triangular envelope at the input and at the output. The results of time-domain simulation are presented in Fig. 17 with both tuning voltages $V_2 = 660\text{mV}$ and $V_2 = 780\text{mV}$. As it could be predicted by figure 15, for a 2GHz sinusoidal signal the delay is 2.8 ns when $V_2 = 780\text{mV}$ and 3.3ns when $V_2 = 660\text{mV}$. Also the amplitude of the output signal is decreased for $V_2 = 660\text{mV}$ as predicted by Fig. 16.

4.3 | Comparison with the state-of-the-art

The previously presented simulation results are compared with the state-of-the-art designs of integrated linear group delay filter and comparison is given in Table 6. In this paper, for the first time the possibility to tune the group delay slope of the filter is offered. This is very important as illustrated in the high-level Analog Chirp Fourier Transformer (ACFT) for cognitive radio presented in⁴. Indeed it is explained that, for the same time frame, when the slope of the group delay is decreased, the resolution of the spectrum is increased. A tunable slope would then allow to zoom a certain part of the spectrum. It should be noticed that in⁴ the results are obtained with an ideal complex model of the dispersive filter having a group delay slope of 170 ns/GHz for a bandwidth of 6 GHz and a maximum time frame (i.e. group delay swing) of 1 μs . Consequently this inspiring ACFT cannot be implemented for the moment with only one technology. Indeed, with SAW filter technology a group delay swing of several μs could be obtained but not a bandwidth of several GHz. With integrated filters at the contrary, the bandwidth of several GHz could be reached but not a group delay swing of several μs . A more realistic application is proposed in⁵ with a Real-Time Spectrum Analyzer (RTSA) for a bandwidth of 0.4-4 GHz and a group delay swing of 1.2 ns. With a bandwidth of 0.5-3 GHz and a group delay swing of 3 ns, our work would allow the design of an ACFT or a RTSA for spectrum analysis for the bandwidth in the range from 1 GHz to 3 GHz.

5 | CONCLUSION

This paper has presented the design of a filter with a linear group delay characteristic. This kind of filter is a key block for many analog signal processing (ASP) applications, especially for spectrum analysis. The design is based on eight second order all-pass cells with optimized values of pole frequency and pole- Q . To fit as good as possible the optimized characteristic of the group delay, a dedicated $Gm - C$ topology has been proposed, which takes into account parasitics since the earlier stage of design. A high-level sensitivity analysis of the filter composed of the eight dedicated $Gm - C$ topology highlights the possibility of tuning the slope of the group delay characteristic. The design has been achieved with a ST CMOS 55nm technology and transistor level simulation results shows a group delay characteristic with tunable slope between 1.2 ns/GHz up to 1.4 ns/GHz in a bandwidth comprised in [0.5 - 3] GHz.

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