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Assessment of 10 nm Tunnel-FETs and FinFETs transistors for ultra-low voltage and high-speed digital circuits

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Abstract—The trade-offs of the Tunnel-FETs (TFETs) in terms of delay, energy per cycle, and noise margin are compared with 10 nm FinFETs for a wide voltage supply ranging from 200 to 600 mV with a specific focus on the ultra-low voltage domain. A calibration process is carried out to ensure the same off-current and extrinsic capacitance in both devices. The TFETs presented a high advantage in terms of delay as well as a penalty in energy consumed. As a result, the TFET circuits show a better Energy-Delay trade-off in voltages as low as 350 mV. This is explained by a larger capacitance caused by the nature of the intrinsic materials chosen of the device modelling.

Keywords—Digital circuits, FinFET, Energy-delay trade-off, Tunnel-FET (TFET), Ultra-low voltage

I. INTRODUCTION

Ultra-low-power circuit design enabled a vision of highly integrated mobile computing systems with lifetimes in the order of years. Such computing systems are attractive for biomedical applications, battery-less operated devices and environmental monitoring for IoT. The energy consumption of these systems ultimately limits form factor, battery life, and complexity. It is therefore critical to develop circuits capable of performing complex tasks under stringent energy constraints. Various low-power digital design techniques have been explored over the past several decades, but supply voltage scaling is generally shown to be the most effective technique due to the quadratic dependence of dynamic energy on the supply voltage [1]. References [2] and [3] have shown that minimum energy is typically achieved when transistors operate in the subthreshold region by working with a V_{DD} scaled below V_{th} . Subthreshold circuits have been shown to be functional below 200 mV [4]. However, an exponential delay increase, high sensitivity to process variations, and temperature fluctuations [5], [6] have limited the adoption of ultra-low-voltage (ULV) circuits from low to mid performance applications.

The FinFET has replaced planar MOSFET in digital circuits since the 22nm technological node, as it shows a superior subthreshold slope (SS) making it a good choice for ultra-low voltage applications. Per contra, the swing of both the FinFET and the planar MOSFET is limited to 70–60mV/dec. The Tunnel-FET (TFET) is a novel device that has shown a subthreshold slope even lower than 60mV/dec making it the ultimate choice for ultra-low Voltage/Power (ULV/P) electronic circuits targeting a voltage supply V_{DD} below 500 mV [7], [8]. Thanks to the different subthreshold conduction behavior of TFET and FinFET, several research groups have proposed comparative benchmarks based on applications ranging from analog [9] to digital [10]–[12], where results have demonstrated that TFETs have the potential to outperform FinFETs at an operating voltage V_{DD} below 400 mV [13]–[16]. Compared to the FinFET, the TFET presents a larger on-current and a smaller propagation delay at ultra-low-voltages (close to 200 mV) [11]–[17]. Nevertheless, the TFET is known to have a higher gate-drain capacitance that can produce significant dynamic energy consumption and has a unidirectional drain current due to the asymmetry of its drain and source regions [13]–[17]. The physic model of the TFET being a geometric structure made out of AlGaSb/InAs nanowires is the reason for the asymmetry of the device. Even if the TFET enables lower power consumption in a circuit when compared to the FinFET it is not clear if under the energy budget perspective the FinFET remains an interesting choice.

This paper assesses Energy - Delay (ED) trade-offs of TFET based digital gates optimized for large Static Noise Margins (SNM). A comparison with 10 nm FinFET with a similar optimization methodology has been performed for several basic digital gates using a wide voltage V_{DD} range. The present article is organized as follows: the methodology

and calibration of the devices to achieve a fair comparison are presented in Section II. The simulation results and measurements are shown and discussed in Section III. Section IV concludes the comparison between the FinFET and the TFET.

II. METHODOLOGY AND CHARACTERIZATION

TFETs and 10nm PTM-FinFETs are compared in this work. The TFETs are described through the Look-Up Tables (LUTs) provided by the authors in [8] which contain the drain current, gate-drain and gate-source capacitances of the TFETs and were simulated through a Verilog-A file. The FinFETs are based on predictive-technology-models (PTM) - available at [18] - that were simulated with the corresponding parameters for the 10 nm low-standby-power (lstp) versions - that is fin height of 21 nm, fin width of 9 nm, and l_g of 14 nm [19]. The lstp version of the PTM-FinFETs was used since a study in a wide supply voltage range (from 200 to 600 mV) is produced with a special focus on the ultra-low voltage domain (ULV) $V_{DD} < 400$ mV. All of the simulations presented were executed in Synopsys Custom Compiler.

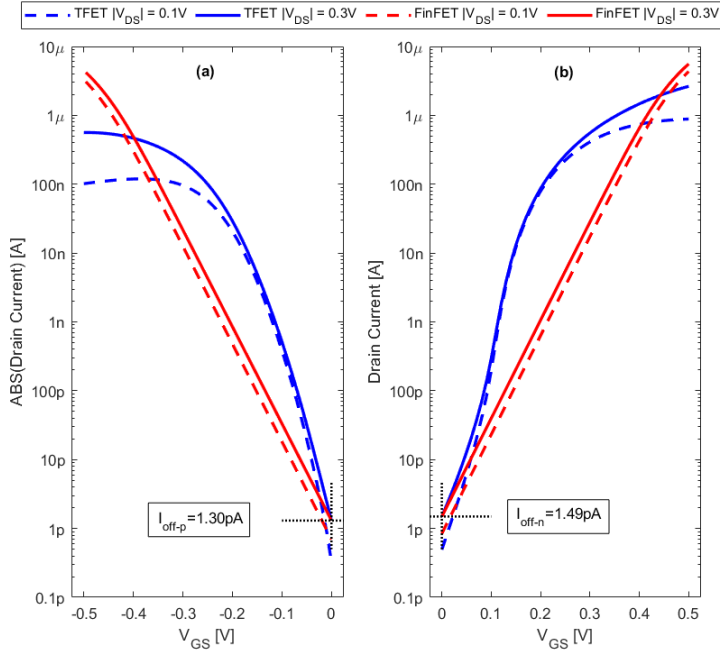


Fig. 1. (a) p-type and (b) n-type drain current (I_{DD}) at $|V_{DS}| = 100$ and 300 mV of a single TFET and FinFET calibrated for an equal off-current of $I_{off-p} = 1.30$ and $I_{off-n} = 1.49$ pA at $V_{DD} = 300$ mV.

The TFETs LUTs must be calibrated to ensure a fair comparison with the FinFETs, which requires the alignment of the transfer characteristics of both n- and p-type TFETs [8], [17]. First, the drain current (I_{DD}) of both the n- and p-type TFETs are calibrated for an off-current of 1.30 and 1.49 pA respectively at $|V_{DS}| = 0.3$ which correspond to the off-currents of the n- and p-type FinFETs. Fig. 1 shows the I_{DD} vs V_{GS} graph for $|V_{DS}|$ voltages of 300 mV and 100 mV where the calibration is evident. Note that the slope of the TFET is able to provide a bigger on-current than

the FinFETs at the same voltage showing the improvement in SS; nevertheless, this tendency reverses at approximately $|V_{GS}|=0.4$ V as explained in [8] since the TFETs are mainly intended for low supply voltages. The slope of the TFETs is much steeper due to the better SS but there is asymmetry between the n- and p-type TFET devices which is not present in the FinFETs.

The last parameter to be calibrated is the gate capacitance (C_{GG}) which is the sum of the gate-source and gate-drain capacitances stored in the TFETs LUTs, where the same extrinsic capacitance as the FinFET models is desired. Fig. 2 presents the C_{GG} vs V_{GS} graph for $|V_{DS}| = 300$ and 0 mV in which it is shown that both devices have been calibrated to a 30 aF extrinsic capacitance. Note that while both FinFET models are symmetric, the p-type TFET has a much higher C_{GG} than its n-type counterpart.

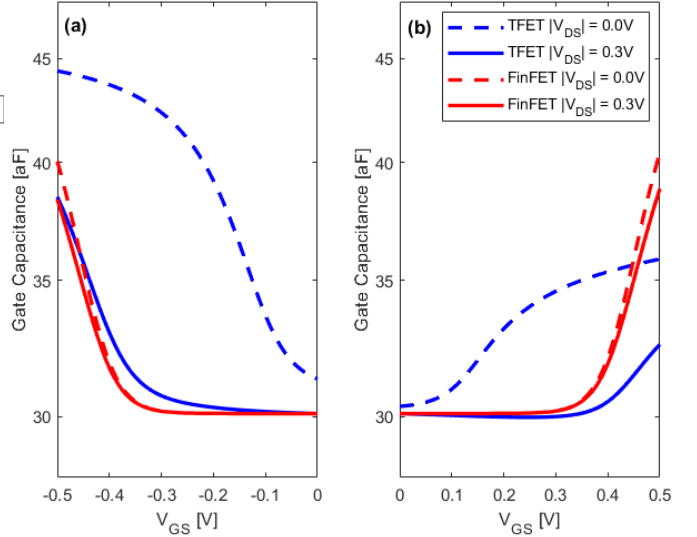


Fig. 2. (a) p-type and (b) n-type total gate capacitance (C_{GG}) at $|V_{DS}| = 0$ and 300 mV for a single TFET and FinFET calibrated for an equal extrinsic capacitance of 30 aF at $V_{DD} = 300$ mV.

The drain current and the gate capacitance of the TFET demonstrated the asymmetry of the device and the necessity of a sizing process to compensate for it. The optimization of the static noise margin (SNM) was considered to reduce this asymmetry as seen in Fig. 3 where the butterfly plot of the voltage transfer curve (VTC) for a TFET and FinFET inverter after the sizing process is presented at a supply voltage of 300 mV. The size of the transistors in the pull-down network (PDN) of the inverter was fixed to the minimum allowed dimension (referred from this point onward as X1) since the n-type TFET has better drive characteristics. Then, the multiplier of the transistors in the pull-up network (PUN) that optimized the VTC by centering it at half of the supply voltage was selected. A factor of 3 was needed at the PUN to center the VTC of the TFET inverter while the FinFET gate required a factor of 1.

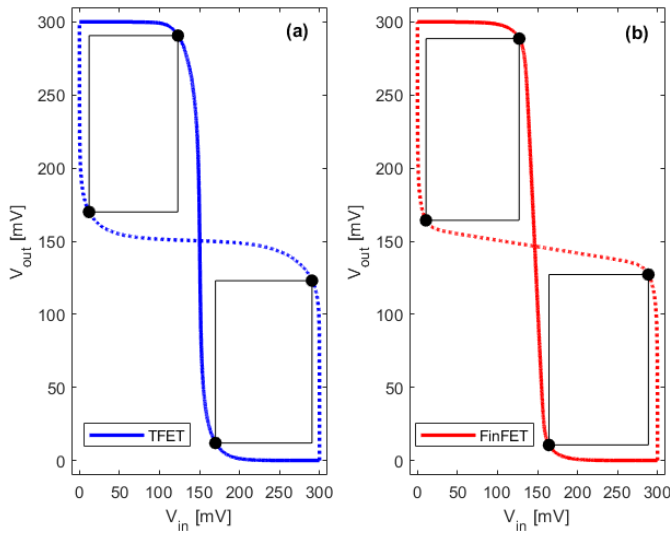


Fig. 3. Butterfly plot of the Voltage Transfer Characteristics of a (a) TFET and (b) FinFET inverter at $V_{DD} = 300\text{mV}$ after the sizing process.

III. RESULTS

The TFET and FinFET devices will be compared in terms of performance and energy efficiency. First, a chain of 20 inverters was tested to compare delay and energy per operation as well as the effects of sizing with an initial multiplier factor of 1 (X1), twice the initial multiplier factor (X2), fan-out of 1 (FO1), and fan-out of 4 (FO4). Then, 2-NAND 2-NOR chain of 20 gates will be used to compare delay, energy, noise margin, and logic depth similar to [20]. These analyses are carried out over a supply voltage range from 200 to 600 mV with a step size of 25 mV. Special comments will be made regarding ultra-low voltages (ULV) at a V_{DD} lower than 400mV where the TFET vastly outperforms the FinFET in terms of delay.

The energy vs. delay plot for a chain of 20 inverters is presented in Fig. 4 where 8 different chains were tested and composed entirely out of TFETs or FinFETs with FO1 or FO4 loads, and with sizing schemes X1 and X2. The points with the smaller delay and higher energy per operation (upper-left corner) correspond to the higher end of the supply voltage range ($V_{DD} = 600$ mV) while the opposite ones (lower-right corner) correspond to $V_{DD} = 200$ mV. There is a trend where the TFETs have more energy consumption while having a much lesser delay than the FinFETs at low voltages. For example, The TFET chain with a FO1 load and sizing scheme X1 consumes 177.4 aJ while presenting 74.65 ns at $V_{DD} = 200$ mV. It is also seen that increasing the minimum allowable dimensions do not distinctly improve the delay while doubling the energy per cycle.

On average, the FinFET is 11.1 times slower than the TFET on the ULV domain while being 4.4 times faster for the rest of the voltage range regardless of the sizing or the load. At $V_{DD} = 200$ mV the TFET exhibits a maximum advantage being 31.7 times faster than the FinFET with the FO4 and X1

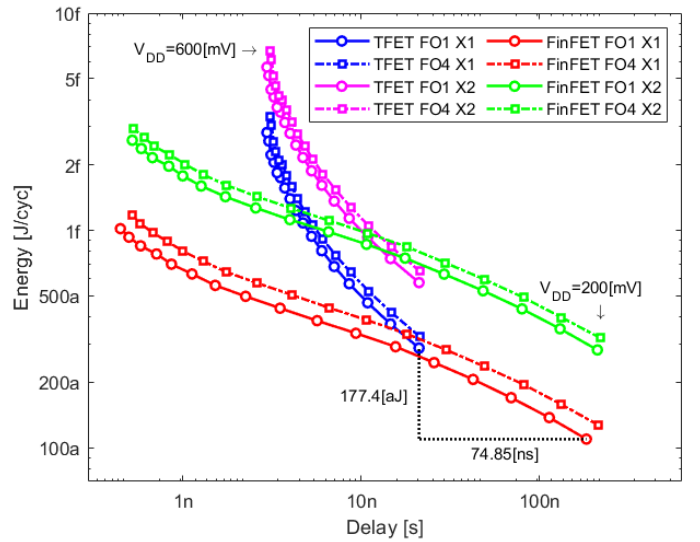


Fig. 4. Energy per cycle vs Delay for a supply range of 200 mV to 600 mV in a chain on 20 inverters using FO1, and FO4 loads as well as a PDN minimum sizing factor of 1 (X1) and 2 (X2).

configuration. The FO4 load adds a 2.53% penalty in delay for the TFET at X1 while it affects the FinFET much more with a 24.92% of speed decrease. The TFET consumes in average 2.74 times more energy per cycle than the FinFET for the whole voltage range. This increase is due to the higher on-current being delivered by the TFET as well as the high activity factor of $\alpha = 0.5$ used as a worst case metric considering an input signal constantly changing; therefore, the energy consumed will be the highest. The voltage overshoots produced by the bigger capacitance of the TFET contribute to a higher energy consumption and have a significant impact in this worst-case scenario. Dimensioning the gates at X2 doubles the energy consumed for the TFET while affecting the FinFET with a 2.56 increase factor.

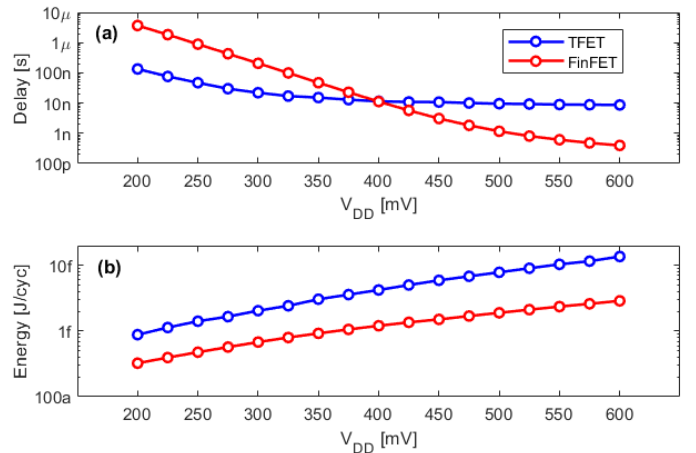


Fig. 5. Propagation delay (a) and energy per cycle (b) comparison in a chain of 20 interleaved 2-NAND 2-NOR gates for a supply voltage range of 200 mV to 600 mV.

A testchain of 20 interleaved 2-NAND and 2-NOR gates sized with the minimum inverter multiplier factor (X1), a FO4 load, and 2 input buffers was used to further explore the energy and delay comparisons of both devices in terms of the supply voltage as can be seen in Fig. 5. The delay in Fig. 5(a) shows the clear advantage of the TFET when the supply voltage is lower than 350 mV being on average 13.14 times faster than the FinFET and a maximum performance at 200 mV where this advantage has a factor of 27.45x; likewise, at higher voltages the FinFET has a better performance being on average 6.32 times faster. Fig. 5(b) shows that the TFET is more energy consuming than the FinFET across all the voltage range, mainly due to its high capacitance. The TFET consumes 4.13 times more energy on average for the whole voltage range.

The energy-delay product (EDP) is presented in Fig. 6 to analyse the trade-off between performance and energy consumption. The supply voltage of $V_{DD} = 350$ mV is the decisive point where at higher voltages the EDP of the TFET starts being higher than the FinFET. The TFET has in average an EDP 5.82 times greater than the EDP of the FinFET at voltages below $V_{DD} = 350$ mV while the FinFET presents an average EDP 34.77 greater at the higher-end of the range. It is clear that the TFET should be used in the ULV domain for a better trade-off between performance and energy consumption.

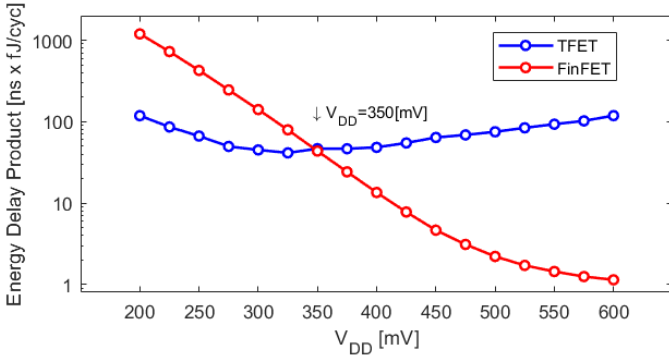


Fig. 6. Energy-Delay Product in a chain of 20 interleaved 2-NAND 2-NOR gates for a supply voltage range of 200 mV to 600 mV.

The robustness of the 2-NAND 2-NOR chain is discussed next with the static noise margin (SNM) presented in Table I. Both the TFET and the FinFET present similar robustness across a voltage supply range of 200 mV to 600 mV with a step size of 100 mV. The sizing process is thus proven correct since the TFET is able to present a similar SNM than the FinFET even though the former has intrinsic asymmetric transfer characteristics. Even though the PUN and PDN of the TFET present a similar drive current which centers the VTC and provides a better SNM, the effect cannot be maintained across all of the voltage range. At 200 mV the difference between the TFET and FinFET SNM is the biggest.

Fig. 7(a) shows the delay and Fig. 7(b) presents the energy per cycle both normalized to the number of gates as a function of the logic depth (LD) of the 2-NAND 2-NOR chain. The

TABLE I
STATIC NOISE MARGIN

V_{DD} mV	SNM mV	
	TFET	FinFET
200	89.00	96.39
300	150.00	146.0
400	199.00	196.00
500	247.00	246.00
600	292.00	295.00

delay per gate remains constant through the whole chain, while the energy per cycle is higher if the path consists of a smaller number of gates for both TFET and FinFET. Two supply voltages were considered: 300 mV and 500 mV to sample the ULV domain and a higher supply. Once again, the TFET presents a smaller delay in the ULV range while a slower performance at 500 mV. The degradation in delay when comparing the 500 mV supply to the 300 mV one has a factor of 2.19x for the TFET and a factor of 180.02x for the FinFET. Therefore, the FinFET exhibits a higher delay degradation that ends up severely affecting the delay at lower voltages in all of the LD range. The TFET chain has a higher energy consumption for both supply voltages throughout the whole LD. Decreasing the supply voltage amplifies the energy consumption 4.11 times for the TFET and 2.70 times for the FinFET across the LD of the chain.

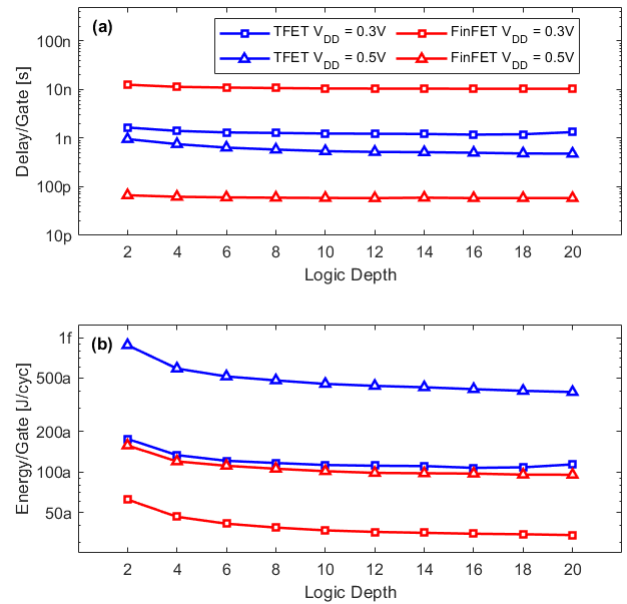


Fig. 7. Logic depth in terms of (a) delay and (b) energy per cycle both normalized to the number of gates in a 2-NAND 2-NOR chain for a supply voltage of 300mV and 500mV.

The performance was further evaluated with a two-dimensional table that involves the measurement of the propagation delay for different values of transition slopes ($Slope_{in}$) and capacitance loads (C_{load}). Supply voltages of 300 (Fig. 8(a) through (c)), and 500 mV (Fig. 8(d) through (f)) were

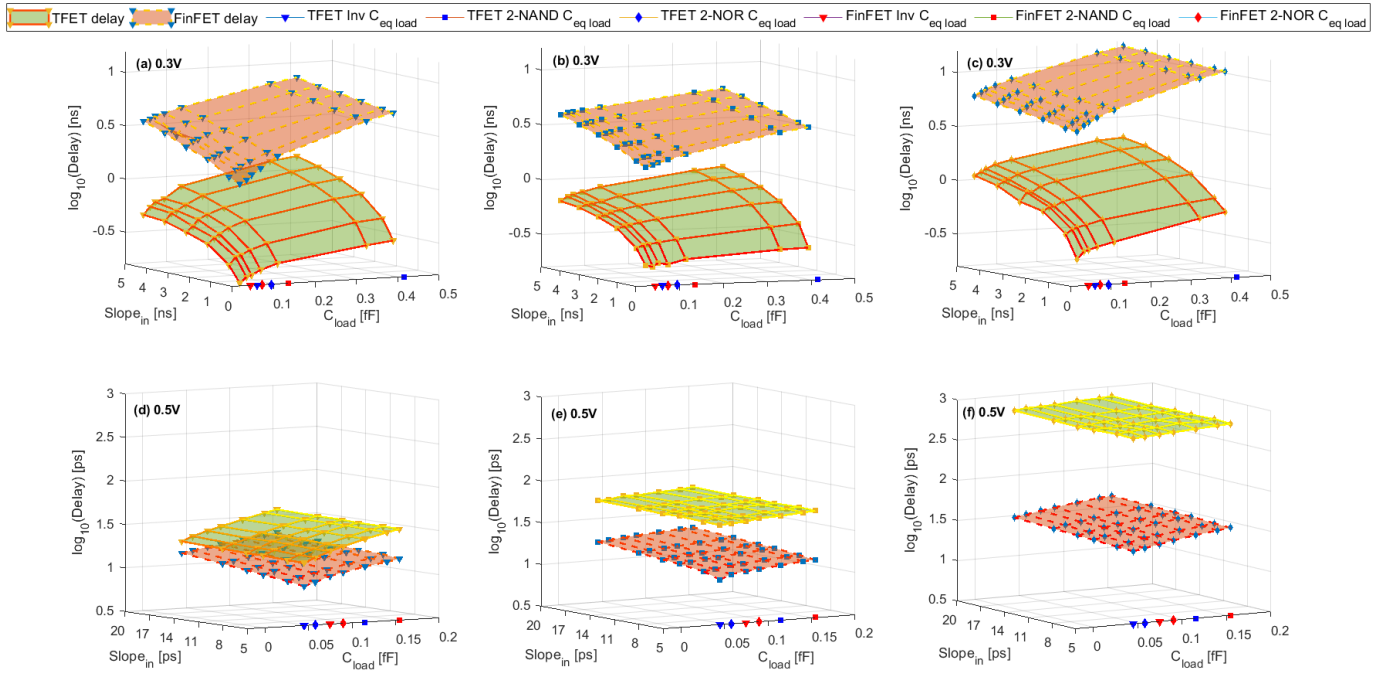


Fig. 8. Propagation delay in terms of input slope $Slope_{in}$ and load capacitance C_{load} at a voltage supply of 0.3V ((a) through (c)) and 0.5V ((d) through (f)) for an (left) inverter, (middle) 2-NAND, and (right) 2-NOR.

used to measure the delay corresponding to minimum sized inverter (left), 2-NAND (middle), and 2-NOR gates (right).

The limits in the chosen load capacitance vector are the highest and lowest equivalent capacitance that each of the tested gates generate as a load. Three input inverters were connected to an inverter, 2-NAND, and 2-NOR gates acting as a load and the capacitance that generates the same propagation delay as these gates is selected as the equivalent load capacitances presented in Table II and marked on the capacitance axis of Fig 8.

TABLE II
EQUIVALENT LOAD CAPACITANCE fF

Gate	$V_{DD} = 300$ mV		$V_{DD} = 500$ mV	
	TFET	FinFET	TFET	FinFET
Inverter	0.0603	0.0411	0.0449	0.0746
2-NAND	0.4147	0.1354	0.1149	0.1543
2-NOR	0.0947	0.0727	0.0576	0.0898

All of the benchmarks in Fig. 8 show that the TFET is superior in terms of delay at a supply voltage of 300 mV, while the FinFET is faster at a supply voltage of 500 mV across the slope and load capacitance test vectors defined by the equivalent load capacitances from each gate. At 300 mV the TFET is faster, on average, by a factor of 7.13x for the inverter, 6.47x for the 2-NAND, and 9.36x for the 2-NOR. Even at the worst-performing condition (inverter with a slope of 3 ns and a load capacitance of 0.073 fF) the TFET is 5.1 times faster. For a supply voltage of 500 mV the FinFET is faster, on average, by a factor of 1.83x, 3.54x, and 20.63x for the inverter, 2-NAND, and 2-NOR respectively. The lowest

ratio (inverter with a slope of 20 ps and a load capacitance of 0.045 fF) shows that the FinFET is barely 1.36 times faster than the TFET. This indicates the dominance of the TFET at low voltages and demonstrates how at the range superior to the ULV domain the performance of the FinFET is not severely superior than that of the TFET for simpler gates like the inverter. The difference in performance degrades once the gates consist of more transistors (like the 2-NAND and 2-NOR) due to the asymmetry of the device causing the sizing to increment the capacitance of the gate.

IV. CONCLUSIONS

The current work compared the TFET and the 10 nm PTM-FinFET devices after calibration in terms of energy, delay, and robustness. Sizing of basic digital gates was carried out to account for the inherent asymmetry of the TFET. The superiority in terms of speed performance of the TFET at ultra-low voltages ($V_{DD} < 400$ mV) was demonstrated in different benchmarks including an inverter chain, a 2-NAND 2-NOR chain, and a two-dimensional mesh of transition slopes and capacitance loads vectors for single digital gates. The energy per cycle was also analysed with an activity factor of $\alpha = 0.5$ as a worst-case condition. In all of the various benchmarks the TFET always consumed more energy than the FinFET, due to it driving more current at the same supply voltage. Nevertheless, the TFET showed a bigger improvement in terms of delay than the penalty paid in energy consumption and, the Energy-Delay Product showed that this tendency is specially strong at supply voltages lower than 300mV. The use of TFETs at ultra-low voltages is encouraged due to their

capability of delivering a bigger on-current and lessening their delay when consuming an equal amount of energy as the FinFETs.

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