A 180 nm Low-Cost Operational Amplifier for IoT Applications

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***Abstract*—This paper presents the design and post-layout simulation of a two-stage operational amplifier (opamp) with Miller compensation. The TSMC 0.18µm PDK was used for the design, simulation and implementation in Cadence Virtuoso. The opamp exhibits 20µW power consumption with a 1-V rail-to-rail supply. Post layout simulation shows a unity gain bandwidth (UGBW) of 69.18 MHz (A_v = 49.63dB) with a phase margin (PM) larger than 86° and a Slew rate of 19.87µV/s making our design suitable for small and large signal applications.**

***Keywords*—component, formatting, style, styling, insert**

I. Introduction

Operational amplifiers are fundamental building blocks for almost all analog applications, such as current-to-voltage converters, rectifiers, integrators, filters or voltage comparators. The semiconductor industry led by the CMOS scaling have resulted lately of portability and low-power electronic system. Integrating sensors among other and proposing new applications for the field of environmental monitoring and biomedecine [1]–[3]. However, analog designers had to face several challenges related to CMOS scaling and power consumption to maintain a stable and high enough Gain Band Width (GBW). This has conducted to the emergence of new topologies such as the bulk-driven (BD) [13], subthreshold (SUB) [12] or Body Biased (BB) [11], among others. In parallel, scaling is involving an important increase of the fabrication cost which have demanded the designers to maximize the technology resources for each technology node.

Taking these trade-offs into account, our design is based on a simple two-stage based opamp topology, with only 12 transistors. As a consequence, the proposed opamp can be integrated on a small area, as low as $0.0015mm^2$ for the 180nm technology node. By reducing the complexity of the design we aim for versatile small and large signal applications. Therefore, our design satisfies stability and supply voltage requirements for Internet of Things (IoT) applications [23], [24], which usually integrate opamps with sensors and communication ports.

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In the following the original topology is presented and properly explained. Layout was defined using the 180nm PDK provided by TSMC. We show the results of the post-simulation using Virtuoso tool from Cadence. Finally, we discuss the results and compare them with designs using different topologies. The comparison is performed using a specific figure of merit (FoM) for large and small signal applications and concludes with the yield obtained signals.

II. Operational Amplifier Topology

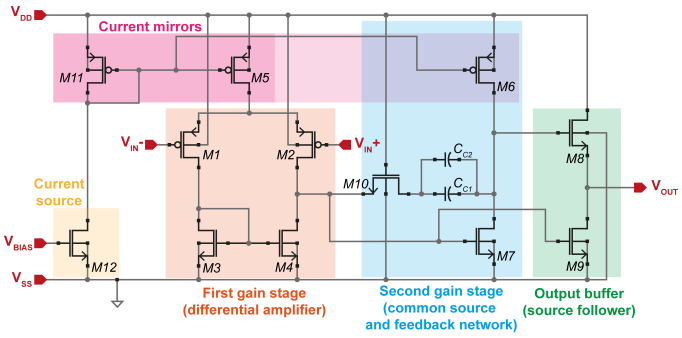

Fig. 1. Schematic of the Two-Stage Operational Amplifier with Miller Compensation

The two-stage opamp topology proposed in this work is shown in Fig. 1. The first gain stage (M1, M2, M3, M4) is a single-ended Operational Transconductance Amplifier (OTA), while the second gain stage (M6, M7) is a common source with an active load. The Miller capacitance feedback network (M10, C_{c1}, and C_{c2}) was used to improve the stability of the circuit [6] by zero-pole cancellation frequency and pole division compensation network [7]. The third stage includes a source follower (M8, M9) to increase the drive capability of a sensor based circuit that is represented by an impedance load (RL//CL). Fig. 1 also shows a current mirror (M5-M11) as well as the V_{bias} controlled current source (M12). The set up choice of pMOS as an input transistors (M1,M2) was made to reduce the low frequency and flickering noise.

The gain of the first stage results are due to a larger aspect ratio for its relation with pMOS as differential input (M1, M2) and nMOS as active loads and current mirrors (M3,M4). These transistors are working together to achieve a single end OTA. The second stage uses a CS amplifier with nMOS input (M7) which enables a larger output voltage. To increase the stage gain it utilizes a larger pMOS transistor as active load and current mirror (M6).

In our topology, the capacitance C_{c1},C_{c2} and the nMOS transistor (M10) have very important functions: Miller Compensation, feedback loop network and matching between first and second stage. The frequency response is going to be dominated by the Miller compensation, which enables the trade-off between stability and a UGBW [8]. As seen in Fig.2, when there is no such compensation, the design is unstable.

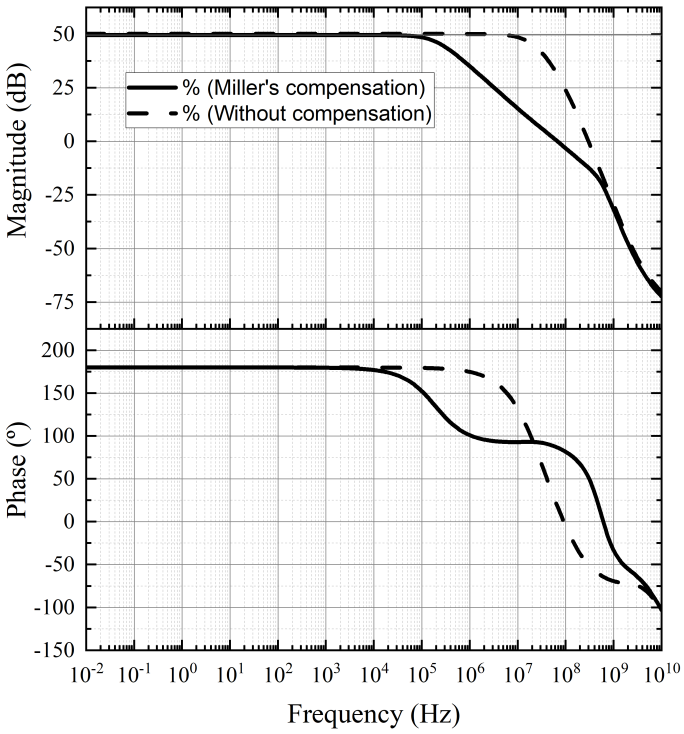

Fig. 2. Bode Diagram with V_{CM} = 345 mV, T = 27 ºC and V_{DD} =1 V with and without Miller compensation

Therefore, the pole splitting technique is used to increase the PM without affecting the UGBW too much by correctly sizing the capacitance and nMOS transistor (M10), which operates in a triode regime. The two capacitors are implemented in parallel C_{c1} and C_{c2} because the 180nm TSMC library did not have the capacitance of 1.734pf.

Finally, the last stage is a source follower nMOS (M8, M9) which would be implemented to increase the capacity of the output drivers for subsequent connection to a following circuit, because the buffer allows matching any stage achieving a low impedance at the output.

Table I presents a summary of the aspect ratio for transistors. Devices in the gain stages were sized to drive enough current

TABLE I
TRANSISTOR SIZING

Stage	Transistor	W/L
First gain stage	M1	114
	M2	114
	M3	16
	M4	16
Second gain stage	M6	300
	M7	34
Output buffer	M8	50
	M9	8
Current mirror	M5	252
	M11	42
Current source	M12	0.85
Miller's compensation	M10	6.8
	C_{c1}	0.867 pF
	C_{c2}	0.867 pF

to exhibit high transconductance for optimization of amplification. Since we are limited by a 1V rail-to-rail supply, the size was carefully selected to ensure saturation of all transistors on each branch. For miller compensation, M10 was set to triode operation region to produce the R_c setting for the stability planned for the amplifier. Since M5 and M6 with M11 will bias the different stages then they require a large aspect ratio to amplify the M12 generated current reference. The output buffer is sized for a gain close to unity.

III. LAYOUT

Fig 3. shows the layout of the opamp based on the schematic in Fig. 1. We ensure that the inputs and outputs were available for connection on the left and the right sides of the design, respectively, hence and the metal overlap was avoided. The parts of the circuit that are activated by voltage were placed closer to the power supplies to avoid voltage drops between the interconnected metals and the contacts. To avoid shunt capacitive discharge and addressing requirements to 180nm TSMC the library design rule check was used. Due to design rule, the operational amplifier area was optimized and avoids etching. The pMOS and nMOS transistors were positioned to share the same n-well and p-well respectively, and the voltage rail with the source electrode, namely AVDD for pMOS and AVSS for nMOS.

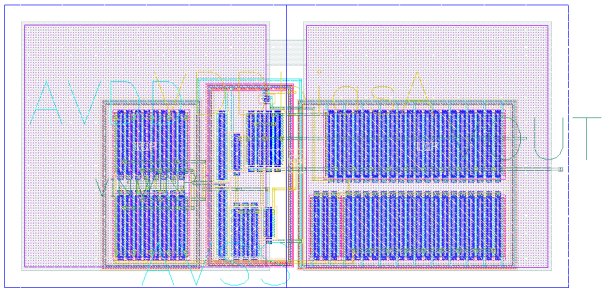

Fig. 3. Layout of the Operational Amplifier with the Compensation Capacitors on the Upper Layer

Transistors input unit placed with matching techniques, each transistor is divided into four parts and connected and interlocked to share the same source [9]. This allows better symmetry in the circuit, as well as greater robustness against etching errors due to variation in fabrication process. The compensation capacitances are the largest cells in the design. Since the outermost metallic layers are used for these capacitors (metals 5 and 6), they are placed on top of the amplifier optimizing the overall area. Fig. 4 shows the final layout without these upper layers.

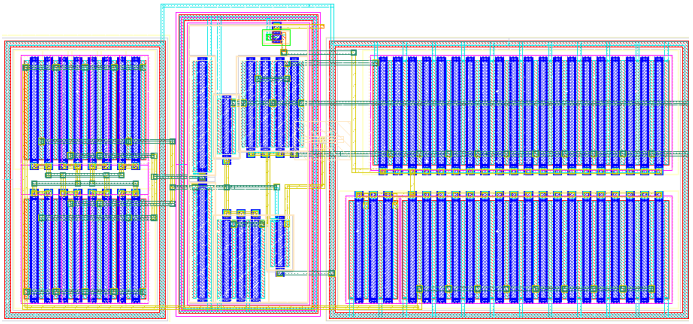

Fig. 4. Layout of the Operational Amplifier without the Compensation Capacitors on the Upper Layer

IV. Post-Layout Results

The post-layout simulation is carried out by using (AXL) . Fig. 5 shows the Bode diagram where we confirm an open-loop voltage gain of about $A_v = 49.63$ dB and with a cut-off frequency of $f_c = 190.55$ KHz. From Fig. 5 we can also extract an $UGBW = 69.18$ MHz. A second pole at 300MHz with a -15db attenuation along with a phase margin of 86.32° demostrates high stability of the UGBW of the proposed topology. It is consistent with the proper RC compensation network from the C_{c1},C_{c2} and M10 sizing design method. The common mode post-layout simulation allows a Common Mode Rejection Ratio (CMRR) of 69.49 dB while noise supply simulation lead to a Power Supply Rejection Ratio (PSRR) of 79.19 dB.

Next, we evaluate the effect of temperature and process variation for a small signal applications. The Bode diagram of a temperature variation in the range of -10°C to 100°C show that the gain and unity-gain bandwidth are relatively constant throughout the whole temperature range while the phase margin show some reduction for the highest temperatures ($T > 70C$) indicating a 4.41 % degradation of the stability. This results demonstrates that the opamp can be implemented in integrated circuit with a temperature sensor and operating reliably between T= -10°C and 100°C. Fig. 7 shows the process corner analysis in AC. We observe a 6.04 % degradation of the unity-gain bandwidth frequency and phase margin in the slower corners with a relatively stable gain.

The process variation measurements were considered through out 1000 Monte Carlo simulations for the gain, UGBW and phase margin (Fig. 8). These simulations produce voltage gain variation from 49 to 52.5 dB. The UGBW varies

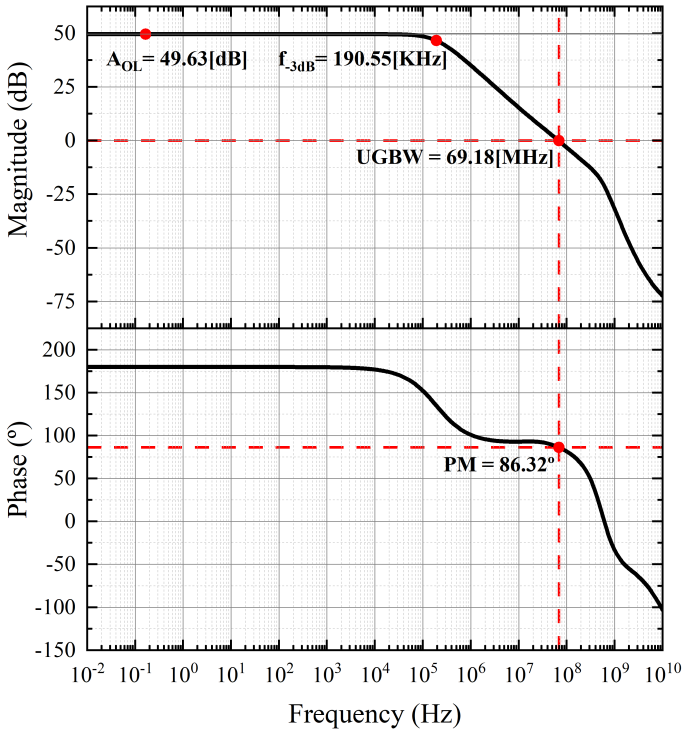

Fig. 5. Bode Diagram with $V_{CM} = 345$ mV, $T = 27$ ºC and V_{DD} =1 V

from 65 to 85 MHz while the phase margin alters from 84° to 91°. As a result the voltage gain is steady while the UGBW is suffering from larger variations, but still remain over 65MHz. On the other hand the PM greater than 84° is consider high enough stability. Therefore the Monte Carlo simulation confirm the robustness of the proposed design for the voltage gain with enough stability.

Another important metric in operational amplifiers design is the slew rate which indicates the speed of the circuit. Fig. 10 shows the post-layout transient analysis executed which showed an average slew rate of 19.875 $V/\mu s$. The slew rate analysis was subjected to a temperature variation from -10 to 100°C as seen in Fig. 10. In which the slope remains the same and the only thing that varies is the settling time up to 2274%.

We conclude from these analysis that the proposed design shows a strong robustness in terms of process and temperature variation. This is explained by our choice to use a simple topology with few transistors. This opamp can perfectly suit for an integration with sensor and communication port for SiP or System on Chip (SoC).

The electrical characteristics and performance of the proposed design is show in Table II where it is compared with design from the recent literature using technological node ranging from 350-65nm and different topology strategy. This comparison demonstrate that the main advantages of our design rely on the low area, high-performance in terms of UGBW, phase margin, and slew rate. Comparable results to other publications were achieved regarding open loop gain, CMRR, and PSRR, while we have some room to reduce

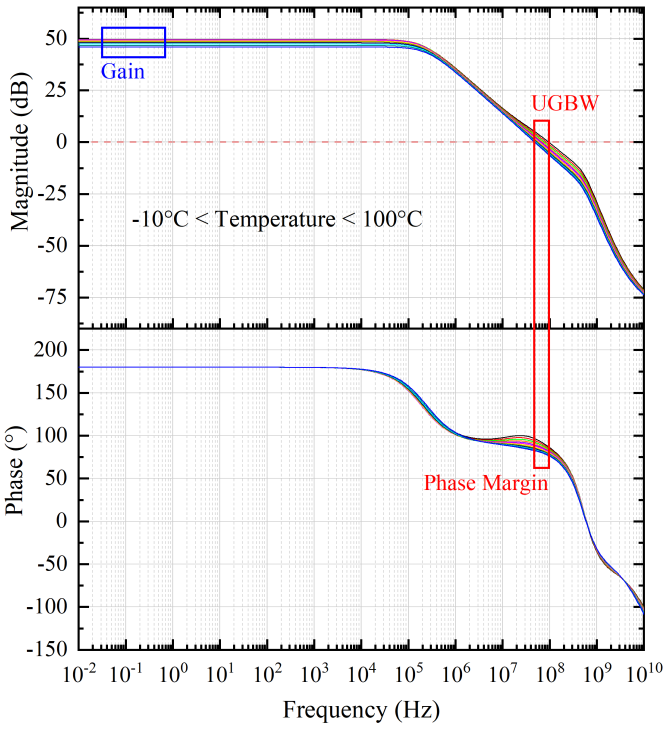

Fig. 6. Bode Diagram with V_{CM} = 345 mV and V_{DD} = 1 V with Temperature Variation from - 10 ℃ to 100 ℃

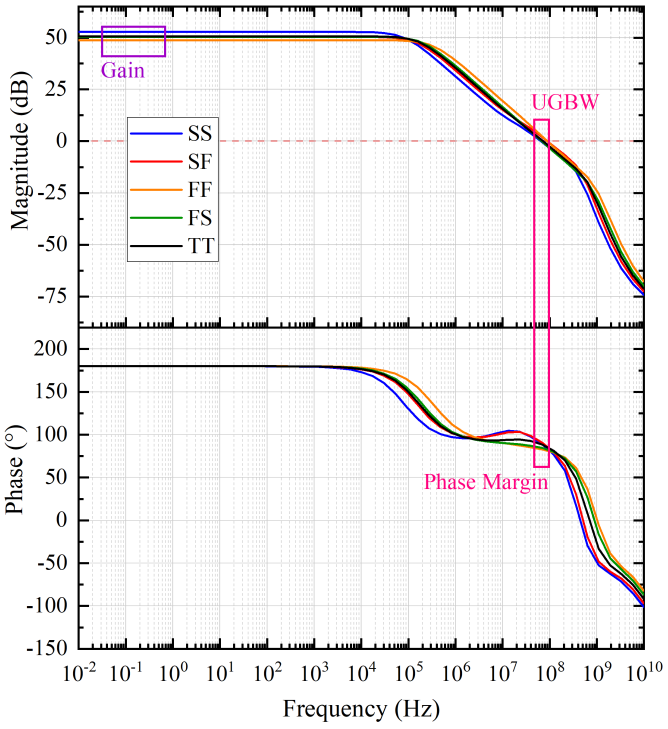

Fig. 7. Bode Diagram with V_{CM} = 345 mV, T = 27 ℃ and VDD = 1 V, with Process Corner Variation

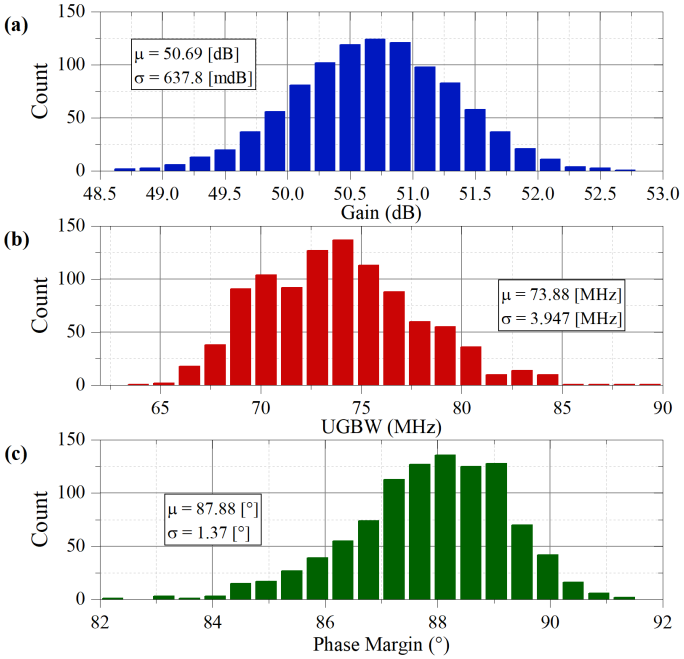

Fig. 8. Monte Carlo simulation with V_{CM} = 345 mV, T = 27 ℃ and VDD = 1 V, where: (a) Gain Distribution, (b) Unity-Gain Bandwidth Distribution, and (c) Phase Margin

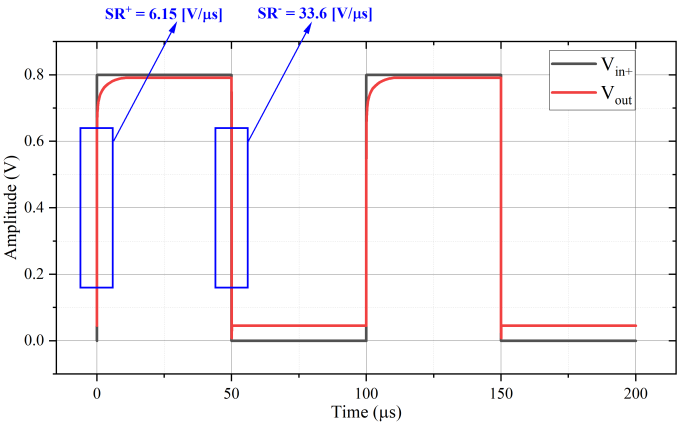

Fig. 9. Transient Simulation for Slew Rate Calculation with V_{CM} = 345 mV, T = 27℃ and VDD = 1 V

voltage supply, power. The chosen load capacitance is lower than other design in 180nm but remains in the range for the expected applications. Also in order to have a fair comparison for the small and large signal performance we decided to use the next FoM

$$FOM_{AS} = \frac{\omega_{GWB}}{AreaI_T} C_L \tag{1}$$

$$FOM_{AL} = \frac{SR}{AreaI_T} C_L \tag{2}$$

where C_L is the capacitance load, I_T the total current and normalized to the area

The values of the FoM for our design and the ones from Table II is given in Fig. 11. For the small signal (FOM_{AL})

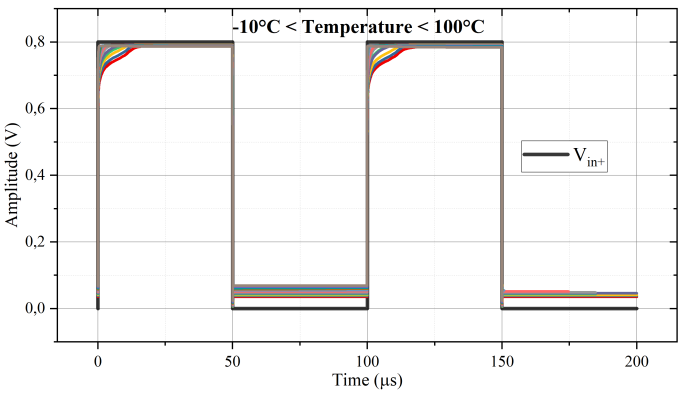

Fig. 10. Transient Simulation for Slew Rate Calculation with V_{CM} = 345 mV and V_{DD} = 1 V with Temperature Variation from - 10 ºC to 100 ºC

as for the large (FOM_{AS}) performance, the opamp design porposed in this work is shown to be on top of the trend line. We can conclude that this opamp is a low cost and simple solution for general purposes involving easy implementation in addition to have a good robustness for temperature variation for various environmental applications.

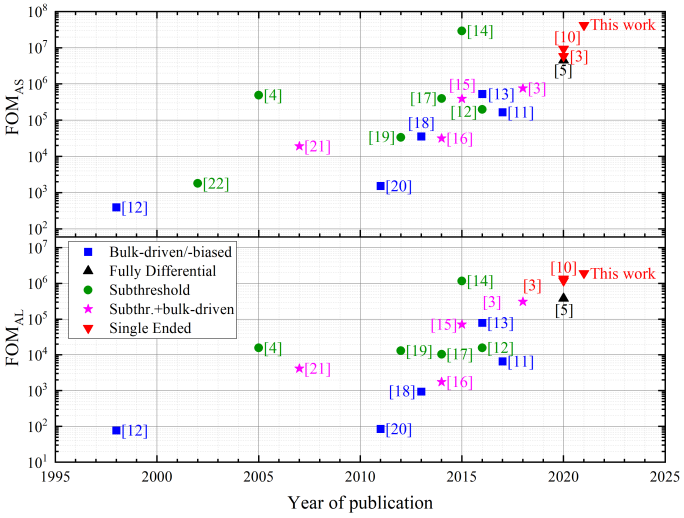

Fig. 11. Small and Large Signal Figures of Merit Normalized to the Area

V. Conclusions

The post-layout results for a two-stage operation amplifier with Miller frequency compensation were presented in this paper. The topology selected was chosen among other more complex and novel architectures due to its high-performance and simplicity in terms of area and stability. This last parameter was of substantial importance since the opamp will be physically implemented in the first integrated circuit of Ecuador so robustness is key. The main objectives of this project were achieved obtaining a DC gain of 49.63 dB, unity-gain bandwidth of 69.18 MHz, phase margin of 86.32°, and slew rate of 19.875 $V/\mu s$ on a total area of 0.0015 mm^2. Temperature, mismatch, and process variations were analyzed to further verify the robustness of the design. Two figures of merit were present in which the competitiveness of this work was demonstrated. Future work includes SoC measurements and exploration of other operational amplifier topologies.

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TABLE II
ELECTRICAL CHARACTERISTICS OF THIS WORK AND OTHER RELEVANT PUBLICATIONS USED FOR FIGURES OF MERIT CALCULATION

	This work	**[5]**	**[10]**	**[3]**		**[11]**	**[12]**	**[13]**	**[14]**	**[15]**	**[16]**	**[17]**
Tech [μm]	0.18	0.18	0.18	0.18	0.18	0.35	0.18	0.18	0.35	0.065	0.13	0.18
Year	2021	2020	2020	2018	2018	2017	2016	2016	2015	2015	2014	2014
Area [mm^2]	**0.0015**	0.0443	0.0085	0.0100	0.0082	0.0140	0.0360	0.0198	0.0044	0.0050	0.0830	0.0570
Supply [V]	1	0.6	0.6	0.6	0.3	0.7	0.5	0.7	1	0.5	0.25	0.5
C_L [pF]	3	10	30	20	20	10	40	20	200	3	15	30
Gain [dB]	49.63	42.2	57.9	2.334	63	65	77	57	129	46	60	70
Power [μW]	20	3	3	3	0.0168	18.9	0.07	25.2	0.195	183	0.018	0.075
UGBW [MHz]	**69.18**	16.1	2.1	2.34	0.0028	1	0.004	3	0.02	38	0.002	0.018
PM [°]	**86.32**	54	59	85	61	60	56	60	52	57	53	55
SR^a [$V/\mu s$]	**19.875**	8.4	1.91	2.97	0.0071	0.25	0.002	2.8	0.005	43	0.0007	0.003
CMRR [dB]	69.49	85.12	75	60	72	45	55	19	70	35	-	-
PSRR [dB]	79.19	55.07	69.2	24	62	50	52	52	184	37	-	-
Op. Mode	SE	FD	SE	SE	SUB,BD	BB	SUB	BD	SUB	SUB,BD	SUB,BD	SUB
Stages	2	2	2	3	2	2	2	3	3	3	2	2

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