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SiN half-etch horizontal slot waveguides for integrated photonics: numerical modeling, fabrication, and characterization of passive components

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Abstract: This work presents a “half-etch” horizontal slot waveguide design based on SiN, where only the upper SiN layer is etched to form a strip that confines the mode laterally. The numerical modeling, fabrication, and characterization of passive waveguiding components are described. This novel slot waveguide structure was designed with on-chip light amplification in mind, for example with an Er-doped oxide spacer layer. Proof-of-concept racetrack resonators were fabricated and characterized, showing quality factors up to 50,000 at critical coupling and residual losses of 4 dB/cm at wavelengths away from the N-H bond absorption peak in SiN, demonstrating the high potential of these horizontal slot waveguides for use in active integrated photonics.

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1. Introduction

Silicon integrated photonics is one of the most studied and developed fields in micro-photonics. Like wires in electronics, the basic structure in integrated photonics is the waveguide, fabricated for example with Si/SiO₂ core/cladding thin films for telecom applications [1] or SiN/SiO₂ for other applications like sensing [2,3]. In both cases, many component building blocks are currently available, both passive (filters, couplers, splitters, polarization management . . .) [4] and active (sources, modulators, detectors. . .) [5,6]. SiN-core waveguides offer several advantages over their Si counterparts such as lower propagation losses, lower sensitivity to temperature variations, and greater tolerance to high optical power. For light amplification, SiN waveguides can be encapsulated with rare-earth doped materials [7,8]. Passive SiN-based integrated photonics components such as gratings, multi-mode interferometers (MMI), and Si/SiN tapers have been fabricated commercially, such as on the STMicroelectronics 300 mm DAPHNE industrial platform [9]. The integration of active components has therefore become a topic of great interest [10].

In *slot* waveguides, the “core” is in fact a narrow low-index region sandwiched between two high-index regions. This structure was studied for the first time in silicon in [11]. Slot waveguides are well-suited for active functions in integrated photonics such as electro-optic modulation, amplification, and light sources as the overlap between the mode energy and the active material is high [12]. In *vertical* slot waveguides, control of mode confinement along the (horizontal) axis of slot width is determined by the photolithography resolution [7]. In *horizontal* slot waveguides, the level of mode confinement along the (vertical) axis of slot height is set by the active material

film thickness, which can be controlled with much greater accuracy and at much lower cost in the fabrication process. In addition, since the active layer in horizontal waveguides does not need to be etched, many more materials can be considered.

Vertical Si-based slot waveguides either show high propagation losses (9 dB/cm [13]) or required isotropic fabrication processes such as wet etching to reduce losses (4 dB/cm [12,14]). Recently, on-chip amplification at 1.54 μm with an $\text{Al}_2\text{O}_3:\text{Er}^{3+}$ film integrated into a SiN-based vertical slot waveguide was demonstrated [7]. However, the SiN was deposited using low-pressure chemical vapor deposition (LPCVD) which is not compatible with middle-of-line (MOL) or back-end-of-line (BEOL) integration in a CMOS process due to the high deposition temperature ($>700^\circ\text{C}$). In addition, high resolution patterning by electron beam lithography was needed for the vertical slot design.

Active Si-based horizontal slot waveguides were first used for the realization of high-speed modulators by integrating into the slot a BaTiO_3 ferroelectric film chosen for its high Pockels coefficient [15]. The authors refer to their configuration as a “partially-etched” horizontal slot waveguide as only the upper high-index (Si) layer is etched to form a strip while the low-index active layer (BaTiO_3) and lower Si layer do not require etching. However, this design suffers from high propagation losses of 20-600 dB/cm due to the metallic SrTiO_3 buffer layer needed for epitaxy. This problem was overcome in [16] where absorption by hydrogen defects was identified as the source of optical losses, which could be reduced to 6 dB/cm at 1.54 μm by thermal annealing at 350°C . Low propagation losses of 6-10 dB/cm have also been obtained for slot waveguides on SOI substrates with integration of thin or thick high bandgap layers of HfO_2 , SiC or AlN, a potentially interesting solution for non-linear optical properties [17]. In this case, losses are caused mainly by strain in the a-Si:H layer and ebeam lithography waveguide stitching errors. Furthermore, such kind of waveguides were also shown in [18], but with relatively low Q-factors. In [19], horizontal slot waveguides with an epitaxial layer of Gd_2O_3 crystal sandwiched between two Si layers were developed for erbium amplification purposes. A high TM mode overlap of 50% within the oxide layer was demonstrated. However, these waveguides showed high propagation losses (284 dB/cm) due to material absorption. This problem was solved in [20] by replacing the upper a-Si layer with SiN, and a signal enhancement of 16 dB/cm was demonstrated at 1.536 μm .

A horizontal slot waveguide based on SiN, therefore, integrating an Er-doped SiO_2 or Al_2O_3 active layer, is a prime candidate for light amplification in integrated photonics with low losses, high mode overlap, and fabrication with low-resolution lithography. In this report on the first part of our work on these devices, we present the design, fabrication, and characterization of passive waveguides integrating the oxide slot layers without Er doping. Racetrack ring resonators were fabricated and characterized as a proof-of-concept devices, demonstrating the potential of the proposed waveguide design for integrated devices incorporating optical amplification that can be fabricated on an industrial platform.

2. Waveguide design

2.1. Principle of operation

In the proposed horizontal slot waveguide design, where the thin lower refractive index oxide layer is sandwiched vertically between the two SiN layers, the upper SiN layer is etched to form a strip that confines the mode laterally. Since only the upper SiN layer is etched, propagation losses from sidewall roughness are greatly reduced compared to the more common horizontal slot waveguide designs where all three layers are etched. Though the authors of [15] refer their Si-based slot waveguide of similar design as “partially-etched”, the expression “half-etch” is preferred here to avoid confusion with true non-fully etched structures such as “partially etched gratings” and to emphasize that one half of the high index layer pair is etched.

2.2. Numerical modeling

In a horizontal slot waveguide, a significant proportion of the transverse magnetic mode (TM) power is confined to the thin film in the slot due to the electric field discontinuities at the top/bottom interfaces. For amplification, erbium doping is commonly used in integrated devices, either in SiO₂ [21] or Al₂O₃ films [7,10,22–24]. Amplification by Er doping requires optical pumping at 1.48 μm or 0.98 μm to amplify a signal at 1.54 μm.

Figure 1(a) shows a cross-section of the proposed half etch horizontal slot waveguide structure used in the numerical modeling. The stack consists of a “spacer” (either SiO₂ or Al₂O₃) sandwiched between symmetric SiN layers deposited on top of a 2 μm SiO₂ buffer layer on an Si substrate. The thickness of the upper and lower SiN layers was set at 350 nm to maximize mode overlap in the spacer layer via symmetry and to facilitate etching of the upper SiN strip (a thicker layer would require a hard mask). Though simulations were run for both SiO₂ and Al₂O₃ spacers, Al₂O₃ is the preferred of the two in practice for active optical properties via Er doping (more efficient amplification due to higher erbium solubility, in particular [25]). Importantly, the effective index of the quasi-TM_{0,0} mode in the slot waveguide must be higher than that of the TE_{0,0} mode in the planar waveguide below formed by the SiN slab (spacer/SiN slab/SiO₂ buffer) to avoid lateral leakage of the minor TE component from the quasi-TM_{0,0} slot mode into the TE slab mode. Lateral leakage is represented by the red arrows in Fig. 1(a). A detailed explanation of this phenomenon is given in [26]. For a spacer thickness of 25 nm, this condition is fulfilled with a SiN strip width of 2 μm. For an Al₂O₃ spacer, a 25 nm thickness was chosen to maximize optical power in the slot (high mode confinement in the active material), upper SiN strip ease of fabrication (relatively thin strip layer adequate for providing lateral mode confinement) and minimal footprint (width), and sufficient difference between the effective indices of the slot and slab modes.

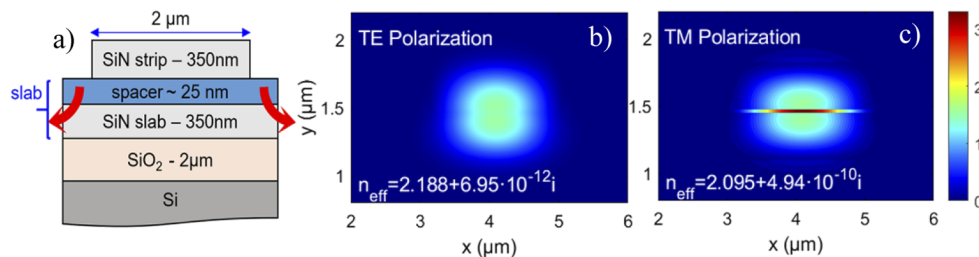


Fig. 1. Cross section of the proposed half-etch horizontal slot waveguide; Mode profiles (power) of the b) quasi-TE and c) quasi-TM modes in a straight waveguide section computed using a finite differences mode solver at 1.54 μm showing the strong confinement of the quasi-TM mode in the spacer layer. Simulation parameters: 350 nm thickness SiN layers, 2 μm width upper SiN strip layer, 25 nm thickness Al₂O₃ spacer, refractive indices of 2.38, 1.44 and 1.6 for SiN, SiO₂ and Al₂O₃, respectively.

Figures 1(b) and 1(c) show numerical modeling results for the quasi-TE_{0,0} and quasi-TM_{0,0} mode profiles for a slot waveguide with a 25 nm Al₂O₃ spacer. The modeling was done using a custom full vectorial finite difference mode solver implemented in Matlab. The solver uses a 9-point discretization scheme to avoid index averaging at waveguide interfaces in cartesian [27] and cylindrical coordinates [26] for straight and curved sections, respectively. Figure 1(c) clearly shows that a significant proportion of the quasi-TM_{0,0} mode power is confined in the spacer layer, as expected (10% mode confinement for the quasi-TM_{0,0} mode versus 4.5% for the quasi-TE_{0,0} mode with 25 nm spacer). Radiative bending losses of the quasi-TM_{0,0} mode are below 0.05 dB/90° for radii greater than 75 μm and below 0.01 dB/90° for radii greater than 150 μm. As an example, at a radius of 20 μm, bending losses reach 0.1 dB/90°, which gives an idea of the lower

limit for an actual device footprint. The same value is obtained for conventional DAPHNE strip SiN waveguides ($n = 1.91$, $0.6 \times 0.6 \mu\text{m}^2$ core).

Numerical simulations of a ring resonator built with the half-etch horizontal slot waveguides were also run. For a racetrack resonator with a 1.34 mm perimeter, 4 dB/cm linear propagation losses, and a $0.7 \mu\text{m}$ spacing between the ring and bus waveguides, a coupling length of $200 \mu\text{m}$ is required for critical coupling of the quasi-TM_{0,0} mode. [28]

3. Fabrication

3.1. Thin film material properties

Device fabrication was conducted sequentially on two sites: first on the DAPHNE photonics platform at STMicroelectronics in Grenoble, followed by the NanoLyon platform at the *Institut des Nanotechnologies de Lyon* (INL). The upper and lower SiN layer pairs were deposited in two distinct material property configurations, termed “standard” and “high index” (described below), to study the effects on propagation losses. First, the lower SiN layers were deposited at STMicroelectronics on 300 mm Si wafers by plasma-enhanced chemical vapor deposition (PECVD) on top of $2 \mu\text{m}$ SiO₂ buffer layers. Two types of SiN films were deposited: a “standard” film with a refractive index of 1.91 at $1.54 \mu\text{m}$ and a “high-index” Si-enriched film with a refractive index of 2.38 at $1.54 \mu\text{m}$ having lower N-H bond absorption losses [29]. Strip waveguide test structures were patterned in the SiN layers at INL to confirm the expected reduction in losses of the “high-index” film (see [Appendix](#)).

The subsequent fabrication steps were carried out on the NanoLyon platform to demonstrate a proof-of-concept device. A layer of oxide (Al₂O₃ or SiO₂) was first deposited by RF sputtering (Alliance Concept AC 450) on the 300 mm wafers received from STMicroelectronics, a well-known CMOS-compatible industrial process. During this process, the cathode was not heated so the only source of heat was the plasma itself ($45 \text{ }^\circ\text{C}$). The deposited film thicknesses were measured by reflectometry: $40 \pm 5 \text{ nm}$ for SiO₂, $15 \pm 5 \text{ nm}$ and $25 \pm 5 \text{ nm}$ for Al₂O₃. The upper SiN layer was then deposited by PECVD at $300 \text{ }^\circ\text{C}$ using a plasma of SiH₄, NH₃ and N₂. The ratio of SiH₄/NH₃ and N₂ flow were varied to obtain upper SiN films with refractive indices close to that of the two types of SiN films deposited on the DAPHNE platform. PECVD SiN shows high propagation losses around $1.525 \mu\text{m}$ due to its high hydrogen content creating absorbing –NH bonds, which are significantly reduced in LPCVD SiN. However, LPCVD is a high-temperature process, whereas PECVD deposition is performed at temperatures around 400°C , which are compatible with the standard CMOS process [30]. The resulting upper SiN film characteristics were determined by ellipsometry: 2.52 ± 0.05 and 2.10 ± 0.05 at $1.54 \mu\text{m}$, with a thickness of $325 \pm 25 \text{ nm}$. Hence, two SiN layer pair configurations with distinct lower/upper refractive index combinations were fabricated: “high index” with 2.38/2.52 and “standard” with 1.91/2.1. The SiO₂ spacer thickness was $40 \pm 5 \text{ nm}$ for both SiN configurations while the Al₂O₃ spacer thicknesses were $15 \pm 5 \text{ nm}$ for the “high index” and $25 \pm 5 \text{ nm}$ for the “standard” configurations, respectively.

3.2. Waveguide patterning and fabrication

Figure 2(a) shows the waveguide fabrication process flow. Wafers received from STMicroelectronics were cleaned using acetone, and ethanol ultrasound bath. An anti-reflective layer coating (Barli) was first deposited to avoid sidewall roughness caused by standing waves in the photoresist profiles. Waveguides were then patterned in MAN2403 photoresist using laser lithography (Heidelberg μPG101) working at a wavelength of 375 nm in vector mode. Compared to the more common raster mode, vector mode is advantageous for writing long straight or curved lines at higher speed without stitching errors and results in reduced sidewall roughness. Waveguides were then etched using inductively coupled plasma (ICP) in two steps: first with an Ar/O₂ plasma

to etch the anti-reflective layer followed by a $\text{Ar}/\text{N}_2/\text{CHF}_3/\text{O}_2$ plasma to etch the upper SiN layer. Any remaining photoresist was removed with an O_2 plasma before encapsulating the waveguides in a $1.2\ \mu\text{m}$ thickness PECVD SiO_2 layer. Figure 2 shows SEM images of a top SiN strip before encapsulation (2-b) and a complete slot waveguide after encapsulation (2-c). The waveguide widths were measured at $1.95 \pm 0.15\ \mu\text{m}$. The SEM images show low sidewall roughness with relatively straight profiles.

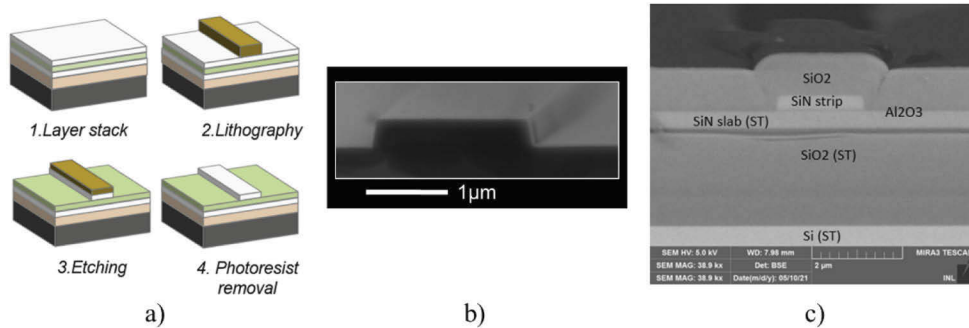


Fig. 2. a) Waveguide fabrication process flow; b) SEM image of a top SiN strip before encapsulation; c) SEM image of a complete slot waveguide after SiO_2 encapsulation.

4. Estimation of propagation losses and spacer layer confinement

4.1. Propagation loss estimation methodology

Figure 3(a) shows the test structure used for propagation loss estimations in both “standard” and “high index” configurations, incorporating four waveguides of different lengths (curved section bending radii of $75\ \mu\text{m}$). While the exact overall device length may vary from one test structure to another due to the cleaving process, the differences in lengths between the 4 waveguides in all test structures (0.8 cm, 1.2 cm, 1.6 cm and 2 cm) were well controlled by the lithography process. Light from a broadband IR source (SLED) was injected by butt-coupling to the slot waveguides using lensed fibers. A polarization controller and filter were placed between the source and the sample to select either the quasi-TE or the quasi-TM mode. Output light power levels were measured separately for each waveguide over the source bandwidth with an optical spectrum analyzer (OSA). The polarization was also verified at the output from the waveguide, showing no parasitic polarization conversion. We measured insertion losses around 15 dB for our setup. Note that bending losses could not be evaluated by top view imaging because the imaged light levels were too low (Fig. 3(b)), which is consistent with the numerical modeling conditions used above.

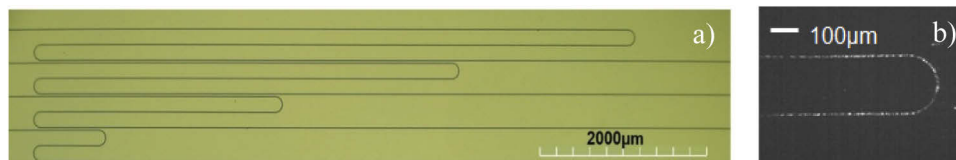


Fig. 3. a) Test structure used for propagation loss estimations incorporating 4 waveguides with differential lengths of 0.8 cm, 1.2 cm, 1.6 cm and 2 cm (bending radius: $75\ \mu\text{m}$); b) top view of a waveguide bend, the waveguide is visible due to radiative losses. This structure was used for all four waveguide configurations.

The slope from a linear regression on the data at a particular wavelength yielded an estimate of the propagation losses at that wavelength. The slope and corresponding uncertainty on the

fit were computed using the York method [31] which allows for errors on both the independent (waveguide length) and dependent (output power) variables. The average error on waveguide length due to lithography tolerances was estimated at $\pm 10 \mu\text{m}$ as the mask alignment precision is on the order of a few μm . The average error on power measurements due to fiber alignment accuracy was estimated at 10%, or $\pm 0.45 \text{ dBm}$ by repeating measurements several times. Figure 4 shows propagation loss estimation by linear regression at $1.434 \mu\text{m}$: $5.26 \pm 0.747 \text{ dB/cm}$. This case was chosen as example where measurement points are not perfectly aligned. Note that we chose to work at low signal power to avoid any unwanted non-linear effects.

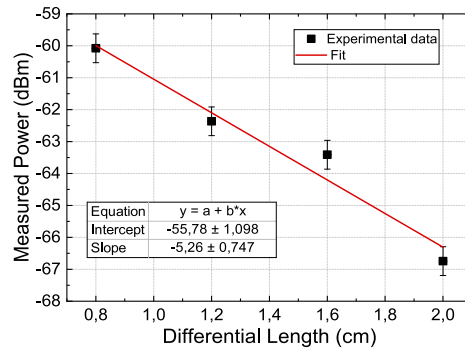


Fig. 4. Example estimate of propagation losses by linear regression at $1.434 \mu\text{m}$: $5.26 \pm 0.747 \text{ dB/cm}$.

4.2. Propagation loss estimation results

Figure 5 shows the frequency-dependent propagation losses estimated from the experimental data using the methodology explained above. Results are shown for waveguides fabricated using the two SiN layer pair configurations (“standard”: $1.91/2.1$ and “high index”: $2.38/2.52$) and the two types of spacer layers (Al_2O_3 and SiO_2), for the fundamental modes in both polarizations.

For Er-doping based optical amplification, the optimal signal wavelength is $1.54 \mu\text{m}$ since it corresponds to the main Er transition used for gain [7]. As expected, as seen in the bottom graphs of Figs. 5(a) and 5(b), the “standard” SiN configuration shows significant losses centered around $1.525 \mu\text{m}$ in both polarizations, which are attributed to absorption by N–H bonds [29]. In contrast, as seen in the top graphs of Figs. 5(a) and 5(b), losses centered around $1.525 \mu\text{m}$ are much less pronounced for the “high index” SiN configuration, including at $1.54 \mu\text{m}$. Oscillations in the curves in the top right graph of Fig. 5(b) are visible, with levels near 0 at higher wavelengths. They can be caused by impurities introduced during fabrication, coupling energy to radiative modes. However, the average value of losses remains correct. AFM measurements were carried out on the 25nm Al_2O_3 layer, showing that the surface is rather smooth, with a RMS value of 0.2nm and a maximum value of 1.7nm .

Table 1 shows the propagation losses estimated from the experimental data both at the N-H bond absorption peak ($\sim 1.525 \mu\text{m}$) and averaged over the $1.58\text{--}1.64 \mu\text{m}$ wavelength range, for both the SiN “standard” and “high-index” layer pair configurations, with either SiO_2 or Al_2O_3 spacer layers. Error bars correspond to the loss standard deviation over this range. These results show that losses are indeed lower in the case of the “high-index” layer pair configurations for the quasi- $\text{TM}_{0,0}$ mode, both at the N-H bond absorption peak and over the wider operating bandwidth (shaded cells in the Table).

These loss values could be further reduced by transferring the technology to an industrial photonics platform: sidewall roughness would be reduced using deep UV photolithography, material quality would be improved, and particle contamination would be extremely low. As

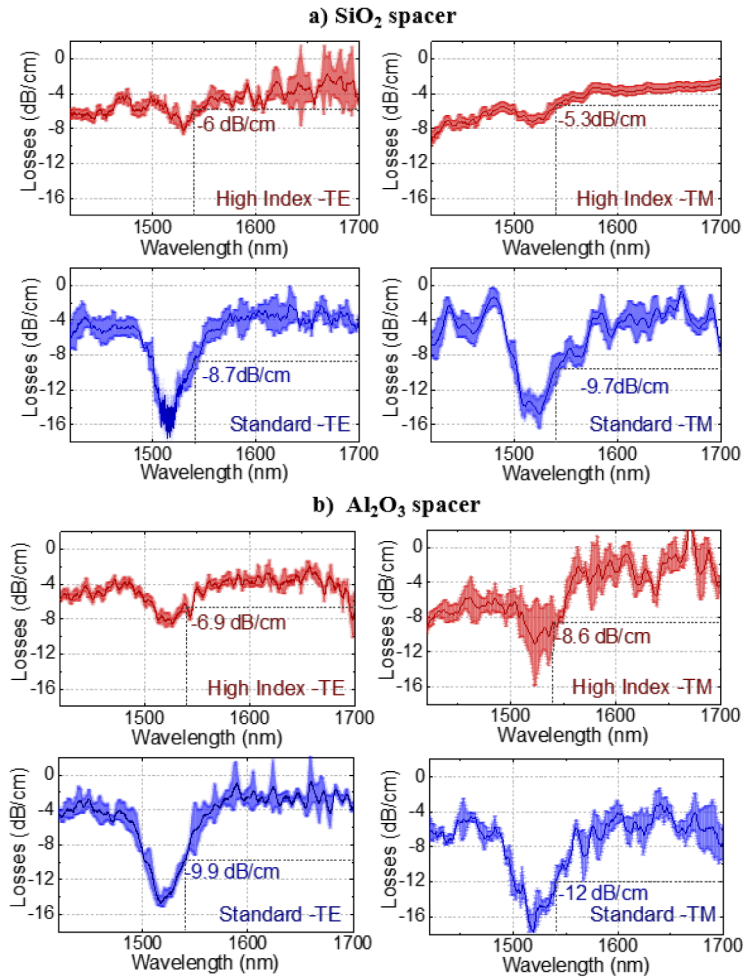


Fig. 5. Estimated frequency-dependent propagation losses for the two SiN layer pair configurations (“standard”: 1.91/2.1 and “high index”: 2.38/2.52) with a) SiO₂ and b) Al₂O₃ spacer layers, for the quasi-TM_{0,0} and quasi-TE_{0,0} modes

Table 1. Losses estimated from the experimental data at the minimum of the N-H absorption peak (~1.525 μm) and averaged over the 1.58-1.64 μm wavelength range for SiN “standard” and “high-index” layer pair configurations with SiO₂ and Al₂O₃ spacer layers

SiO ₂ spacer	quasi-TM _{0,0}		quasi-TE _{0,0}	
	N-H peak	Avg 1.58-1.64μm	N-H peak	Avg 1.58-1.64μm
“High index” SiN	7.2±0.7 dB/cm	3.6±0.2 dB/cm	8.2±0.5 dB/cm	4.2±0.8 dB/cm
“Standard” SiN	14.7±1.7 dB/cm	4.1±0.8 dB/cm	16.8±1.6 dB/cm	3.5±0.4 dB/cm
Al ₂ O ₃ spacer	quasi-TM _{0,0}		quasi-TE _{0,0}	
	N-H peak	Avg 1.58-1.64μm	N-H peak	Avg 1.58-1.64μm
“High index” SiN	11.1±4.9 dB/cm	2.9±1.2 dB/cm	8.6±0.5 dB/cm	3.6±0.4 dB/cm
“Standard” SiN	17.8±2 dB/cm	5.6±1.1 dB/cm	14.7±0.6 dB/cm	2.6±0.6 dB/cm

shown in the appendix, TE propagation losses in a SiN standard strip waveguide ($1 \times 0.35 \mu\text{m}^2$ core) fabricated with our platform were measured at 3dB/cm at $1.31 \mu\text{m}$. In comparison, losses on a $0.9 \times 0.35 \mu\text{m}^2$ strip waveguide patterned at STMicroelectronics showed losses as low as 0.4dB/cm [32], a significant potential for improvement.

If the Al_2O_3 layer is doped with erbium, we can expect losses in the 1.52-1.57 μm wavelength range to increase due to erbium absorption. When the waveguides are pumped with sufficient power, however, this will create signal enhancement [22]. Erbium concentration must be adapted to the waveguides length and losses.

Table 2 shows the fraction of total optical power at 1.54 μm (optimal signal wavelength for Er doping) estimated by numerical modeling in the various layers of the slot waveguide stack, using the actual deposited layer material parameters (optical indices and thicknesses). Note that values were also estimated for the interface volume between the upper SiN strip and the spacer (nominal thickness: 2 nm), as well as for the strip slanted sidewall volumes, since the oxide surface roughness at these interfaces can create additional losses. As seen in Table 2 (shaded cells), even for small Al_2O_3 spacer film thicknesses (< 50 nm), mode confinement in the slot is significant. Note that mode confinement in the thinner Al_2O_3 spacer layer (15 nm, “high-index” SiN) is higher (9% vs 6%) than for the thicker Al_2O_3 spacer layer (25 nm, “standard” SiN) because the SiN/ Al_2O_3 index contrast is higher for the “high-index” SiN layer stack configuration. Interestingly, the fraction of total power in the SiN layers is more important for waveguides with the thinner Al_2O_3 spacers (compared to SiO_2), which may explain the higher absorption for the quasi- $\text{TM}_{0,0}$ mode around the N-H bond peak (Table 1).

Table 2. Fraction of total power at 1.54 μm estimated by numerical modeling in the layers of the waveguide stack SiN “standard” and “high-index” layer pair configurations with either SiO_2 or Al_2O_3 spacer layers^a

“Standard” SiN	SiO_2 spacer (40nm)		Al_2O_3 spacer (25nm)	
	quasi- $\text{TM}_{0,0}$	quasi- $\text{TE}_{0,0}$	quasi- $\text{TM}_{0,0}$	quasi- $\text{TE}_{0,0}$
Upper SiN strip layer	37%	49%	40%	49%
Strip/spacer interface	3%	3%	3%	3%
Spacer	10%	6%	6%	4%
Lower SiN slab layer	33%	28%	36%	30%
Strip slanted sidewall vol.	0.007%	0.003%	0.006%	0.003%
“High-index” SiN	SiO_2 spacer (40nm)		Al_2O_3 spacer (15nm)	
	quasi- $\text{TM}_{0,0}$	quasi- $\text{TE}_{0,0}$	quasi- $\text{TM}_{0,0}$	quasi- $\text{TE}_{0,0}$
Upper SiN strip layer	39%	50%	43%	51%
Strip/spacer interface	3%	3%	3%	3%
Spacer	15%	6%	9%	4%
Lower SiN slab layer	36%	33%	39%	35%
Strip slanted sidewall vol.	0.004%	0.01%	0.004%	0.001%

^aModeling parameters. Lower SiN layer: 350 nm thickness, $n = 1.91$ for “standard”, $n = 2.38$ for “high-index”; upper SiN strip layer: 325 nm thickness, $1.95 \mu\text{m}$ width, $n = 2.1$ for “standard”, $n = 2.52$ for “high-index”; SiO_2 spacer: 40 nm thickness, $n = 1.44$; Al_2O_3 spacer thicknesses: 15 nm (“high-index” SiN) and 25 nm (“standard” SiN), $n = 1.6$.

In both configurations, the mode overlap with the spacer can be improved by increasing the oxide thickness, thus increasing the potential amplification level for rare-earth doped oxide. An optimal thickness value must be chosen to avoid losses from lateral leakage. For “high index” SiN configuration, with a Al_2O_3 spacer thickness of 100 nm, we computed a mode overlap of 24% with losses of 0.2 dB/cm associated to lateral leakage. Above 100 nm, however, the TM

mode is no longer guided [17]. With horizontal slot waveguides, it is also easier to control the thickness of the doped oxide, and to apply a voltage with lateral electrodes to enhance the non-linear properties of the active layer, as was done with a BTO layer in [15]. The half etch slot configuration is therefore a trade-off between a 3D integration of strip waveguide patterned only in the active layer, allowing high confinement factor, and active material cladding on passive strip waveguide, where only the evanescent part of the mode interacts with the active layer, providing less efficiency.

5. Racetrack resonators

Racetrack resonators based on the proposed half-etch horizontal slot waveguides were fabricated using three of the four available permutations of SiN layer pair configurations and spacer materials: “high index” SiN with SiO₂ and Al₂O₃ spacers, and “standard” SiN with SiO₂ spacer. Resonance measurements were carried out by sweeping the wavelength of a tunable laser (Tunics) and integrating the power detected by the spectrometer. Normally, the resonators would be designed for critically coupled resonance at 1.54 μm (optimal signal wavelength for an Er-doped active spacer layer). However, to maximize the quality of the characterization measurements on these first proof-of-concept passive devices, the racetracks were designed for critical coupling at a resonance around 1.6 μm to shift the operating point away from the N-H bond absorption peak (~1.525 μm). Also, resonators were fabricated with a range of different bus/ring waveguide spacings (gap sizes) to study their behavior at different resonances at, as well as away from, critical coupling. In the fabricated devices, the bus/ring spacings measured by optical microscopy ranged from 500 ± 150 nm to 950 ± 150 nm. As shown in Fig. 6, the corner bending radii in the racetracks were 150 μm and the bus/ring waveguide coupling length was 200 μm.

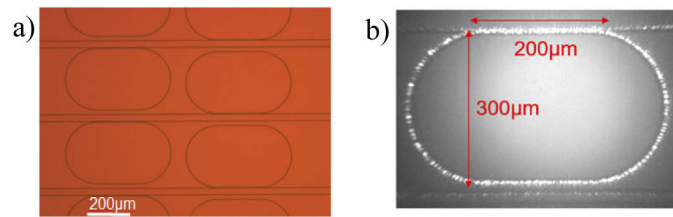


Fig. 6. Top view of fabricated racetrack resonators a) without and b) with light injection

Figure 7 shows examples of experimentally measured I/O transfer functions (normalized transmission through the bus waveguide as a function of frequency) for resonators fabricated with different waveguide structure permutations (SiN layer pairs, spacer materials) and different bus/ring waveguide spacings. The experimental data were fitted with Lorentzian models to estimate metrics such as quality factor and max/min contrast at resonance. The loaded quality factor, Q , is equal to the resonance wavelength divided by the full width at half maximum (FWHM). Extinction ratios were measured in dB from raw measurements.

As seen in the top-right graph of Fig. 7(a), $Q = 54,000$ (17 dB contrast) at critical coupling for the quasi-TE_{0,0} mode in a racetrack having a “high-index” SiN configuration and an Al₂O₃ spacer. The free spectral range (FSR) for this resonator was measured to be 0.7 nm with the same broadband source (SLED) as used for propagation losses measurements. At critical coupling, the loaded quality factor can also be expressed by Eq. (1) [28]:

$$Q = \frac{\lambda_m \pi}{FSR} \times \frac{\exp(-\alpha L/2)}{1 - \exp(-\alpha L)} \quad (1)$$

where λ_m is the resonance wavelength, L is the ring perimeter and α the propagation losses. Assuming $\alpha = 4$ dB/cm, this corresponds to a theoretical Q factor of 59,000, which is very close

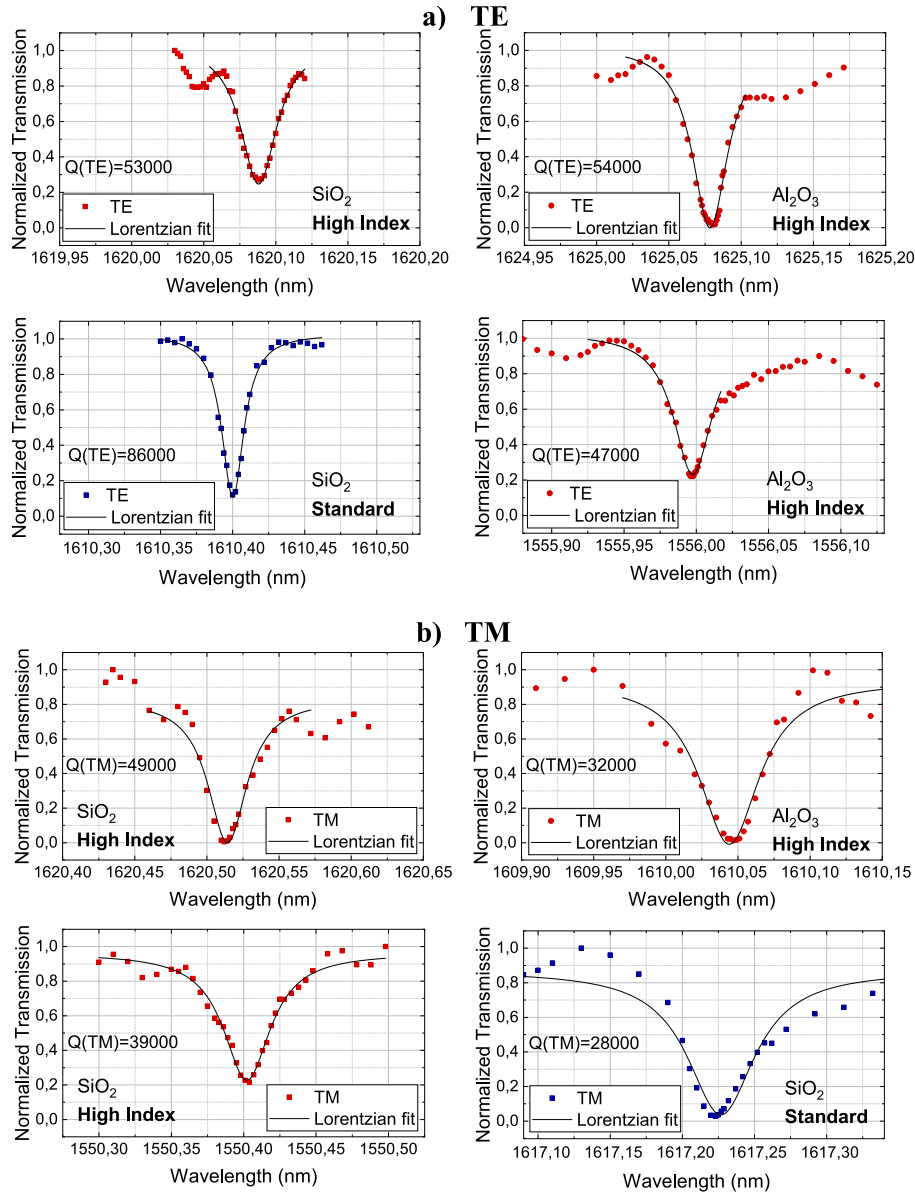


Fig. 7. Experimentally measured ring I/O transfer functions (normalized transmission through the bus waveguide as a function of frequency) for different waveguide structure permutations (markers: experimental data, solid lines: Lorentzian models fitted to the data) for a) TE polarization and b) TM polarization.

to the experimentally observed value. As another example (bottom-left graph of Fig. 7(a)), $Q = 86,000$ (9 dB contrast) for the quasi- $TE_{0,0}$ mode in a racetrack having a “standard” SiN configuration and a SiO_2 spacer (the lower contrast is attributed to a sub-optimal bus/ring spacing at resonance). The bottom-right graph in Fig. 7(a) shows an example of a resonance profile where, even for the resonance around $1.56 \mu m$ that is not at critical coupling, the quality factor is still quite high ($Q = 47,000$).

For quasi- $TM_{0,0}$ modes in racetracks having a “high-index” SiN configuration and a SiO_2 spacer, example resonance profiles were measured at $Q = 49,000$ (22 dB contrast, Fig. 7(b), top-left) and $Q = 39,000$ (6 dB contrast, Fig. 7(b), bottom-left). Similarly, for quasi- $TM_{0,0}$ modes in racetracks with a “high-index” SiN configuration and an Al_2O_3 spacer, a range of resonance profiles were measured, such as $Q = 32,000$ (19 dB contrast, Fig. 7(b), top-right). Here again, the bottom-left graph in Fig. 7(b) shows an example of a secondary resonance away from critical coupling nevertheless having a high quality factor ($Q = 39,000$). Note that the lower Q factors for the TM modes can be attributed to the higher sensitivity to the upper SiN strip width which can cause leakage towards the SiN slab mode below. This problem can be overcome by widening the upper SiN strip, or by increasing its thickness.

6. Conclusion and perspectives

In this work, we presented the numerical modeling, fabrication, and characterization of passive waveguiding components built using SiN half etch horizontal slot waveguides, where only the upper SiN layer is etched to form a strip that confines the mode laterally. Advantages of the SiN half etch horizontal slot waveguides are low losses, high mode overlap, and fabrication with low-resolution lithography. This novel waveguide structure was designed for on-chip light amplification in integrated photonics by Er doping of the oxide spacer layer.

Device fabrication was conducted on two sites: the DAPHNE platform at STMicroelectronics and the NanoLyon platform at Institut des Nanotechnologies de Lyon (INL). Two slot spacer layer materials were compared: SiO_2 and Al_2O_3 . In addition, two SiN layer pairs were compared for the high index materials of the slot waveguide: a “standard” configuration and a “high-index” configuration having lower losses from N-H bond absorption. For the “high-index” SiN configuration, experimental measurements showed residual losses of 4 dB/cm at wavelengths away from the N-H bond absorption peak ($\sim 1.525 \mu m$), where propagation losses induced by sidewall roughness are dominant. Proof-of-concept racetrack resonators were fabricated and characterized, showing quality factors up to 50,000 at critical coupling around a $1.6 \mu m$ resonance wavelength. Propagation losses would be improved by fabricating the entire devices on the DAPHNE platform, resulting in higher quality factors. The -NH bond absorption losses could be greatly reduced by depositing SiN with physical vapor deposition (PVD) (losses of 1.7 dB/cm were obtained at $1.55 \mu m$ on $0.7 \times 0.6 \mu m^2$ strip waveguides fabricated at STMicroelectronics [33], and 0.8 dB/cm for $2 \times 0.4 \mu m^2$ waveguides were demonstrated at $1.55 \mu m$ after annealing at $400^\circ C$ in [34]).

Appendix: propagation loss measurements for the SiN layers deposited at STMicroelectronics

Figure 8 shows the quasi- $TE_{0,0}$ mode propagation losses measured for the “standard” and “high index” SiN layers deposited on 300 mm wafers at STMicroelectronics. Losses were measured using strip waveguides patterned at INL into the same test structures (Fig. 3) as for the slot waveguide loss measurements. The strip waveguide widths were 1000 ± 150 nm for “standard” SiN and 750 ± 150 nm for “high index” SiN. The “high index” SiN waveguides clearly show a reduced N-H absorption peak around $1.525 \mu m$ compared to “standard” SiN.

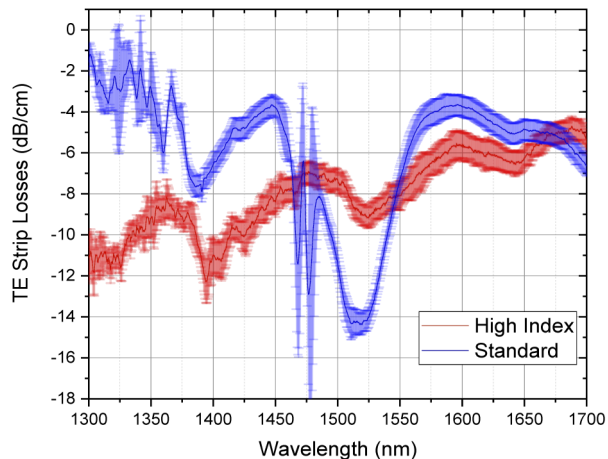


Fig. 8. Quasi- $TE_{0,0}$ mode propagation losses estimated for the “standard” and “high index” SiN layers deposited on 300 mm wafers at STMicroelectronics using strip waveguide test structures patterned at INL.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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