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Vincent Frick, Luc Hebrard, Philippe Poure, Freddy Anstotz, Francis Braun. CMOS Microsystem for AC Current Measurement with Galvanic Isolation. IEEE Sensors Journal, 2003. hal-03570680

**HAL Id: hal-03570680**

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Submitted on 23 Feb 2022

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# CMOS Microsystem for AC Current Measurement with Galvanic Isolation

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*Abstract*—In this paper, we present an integrated AC current sensor based on sensitivity-optimised Horizontal Hall effect Devices (HHDs) and a differential readout chain. This microsystem has been designed for 5A rms nominal AC current measurement with 5kV galvanic isolation and 0.5% accuracy over 1.5kHz bandwidth, which allows up to 30th (25th) harmonic detection in 50Hz (60Hz) applications.

From the sensing element throughout the instrumental chain's output the signal conditioning is exclusively performed by low-noise standard CMOS analog blocks. Moreover the whole microsystem features a mixed signal structure dedicated to auto-balancing.

*Index Terms*—Special Issue Sensors 2002, current sensor, microsystem, Hall effect devices, galvanic isolation, submicron CMOS technology.

## I. INTRODUCTION

CURRENT sensing is a common line in many power control related applications. In an industrial context the sensor's operating conditions are far from the ideal laboratory environment and the designer is confronted to numerous requirements such as galvanic isolation or Electro-Magnetic Compatibility (EMC) in order to make the sensor compliant with norms attached to products it is designed for.

Bulk and expensive current transformers are often used for sensing current with galvanic isolation. Low

cost solutions based on Hall effect devices used to sense the magnetic field produced by the current to be measured are now envisaged [1] [2]. When fabricated in CMOS technologies these Hall devices are associated to complementary embedded electronics for appropriate signal conditioning [3], which allows sensitivity improvement without any post-processing such as flux concentrators affixing. The use of magnetic material induces non-linearity unless it has a good permeability. But this implies higher production costs of the microsystem.

Furthermore, most of magnetic measurement systems based on Hall effect feature spinning-current Hall devices, which are mainly optimised for offset cancellation and  $1/f$  noise reduction but suffer from switching noise [4]. Yet, in AC current-measurement applications, these drawbacks can be passed round with high-pass filtering. Using such an AC coupling, this work concentrates on a solution based on sensitivity-optimised Horizontal Hall effect Devices (HHDs) with dedicated signal conditioning and a special focus on the system's linearity and EMC.

Microsystem design is a discipline where the number of factors one has to take into account can be quite sizeable. Therefore, this paper will start with preliminary considerations on the differential architecture, which is strongly related to the geometry of the conductor strip carrying the current to be measured and to the packaging. The following section will deal with a microtesla range magnetic field sensing front-end. This front-end is connected to an analog differential instrumental chain detailed in the next section. The technique used to balance this chain will then be proposed. Finally, further precision on packaging will be brought and test results will be detailed.

## II. DIFFERENTIAL SENSING ARCHITECTURE

One of the most common means for measuring current with galvanic isolation consists in sensing the magnetic field generated by the current. Yet a single magnetic sensor doesn't discriminate between the useful signal ( $B_C$ ) generated by the current itself and any other parasitic field ( $B_p$ ) from different sources (Earth's magnetic field, radiant voltage transformers, etc.). In the structure proposed by figure 1 the current flows between a pair of identical HHDs embedded on one single silicon die. A general expression

for the Hall voltage at the output of each HHD reads [5]:

$$V_H = K_H B_y = K_H (B_{Cy} + B_{py}) \quad (1)$$

where  $K_H$  is a constant that depends on the material as well as on the HHD's geometry and the biasing conditions [5] [6]. The term  $B_y$  denotes the vertical component of the total magnetic field  $B=B_C+B_p$  applied upon the HHD, composed of both the useful and the external parasitic contributions. As a consequence the output voltages of both HHDs appearing in figure 1 are respectively:

$$\begin{cases} V_{H1} = K_{H1}(B_{Cy1} + B_{py1}) \\ V_{H2} = K_{H2}(B_{Cy2} + B_{py2}) \end{cases} \quad (2)$$

In such a configuration, the useful components of the Hall voltages,  $K_{H1}B_{Cy1}$  and  $K_{H2}B_{Cy2}$  have opposite signs. Therefore, differential signal conditioning might efficiently reject the parasitic components, allowing EMC achievement. However, through this statement we assume that the parasitic magnetic field is a common mode signal, which is proven correct at three conditions. First, the HHDs have to be perfectly identical (i.e.  $K_{H1}=K_{H2}$ ). Besides, they have to be close enough from one another and finally the distance between the silicon die and any parasitic source has to be sufficient so that the field gradient from one sensing element to the other can be considered as negligible. We first will suppose these conditions are true, which is the case in practice as discussed in the section dedicated to the packaging issue.

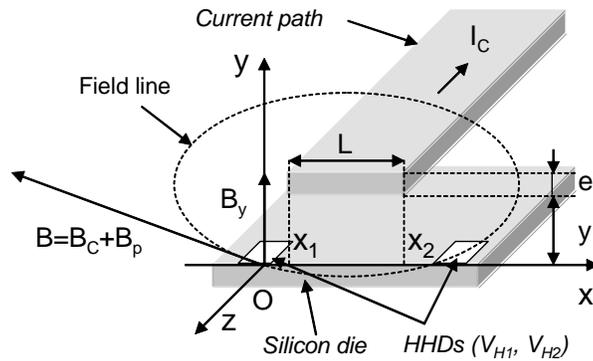


Fig. 1. Differential current sensor topology.

The preliminary phase to the microsystem's design lies in the evaluation of the quantity of magnetic signal that can be expected in the vicinity of the current path. The spatial magnetic field distribution has

been evaluated in order to determine the best tradeoffs between the field's amplitude and the path's position against the HDDs. In open air the magnetic field drops quickly according to the distance from its source. Figure 2 presents a realistic worst case finite-element magnetic simulation carried out with FLUX2D<sup>®</sup>. The current path's section is  $500 \times 35 \mu\text{m}^2$  and the distance to the silicon die is  $y=75 \mu\text{m}$ .

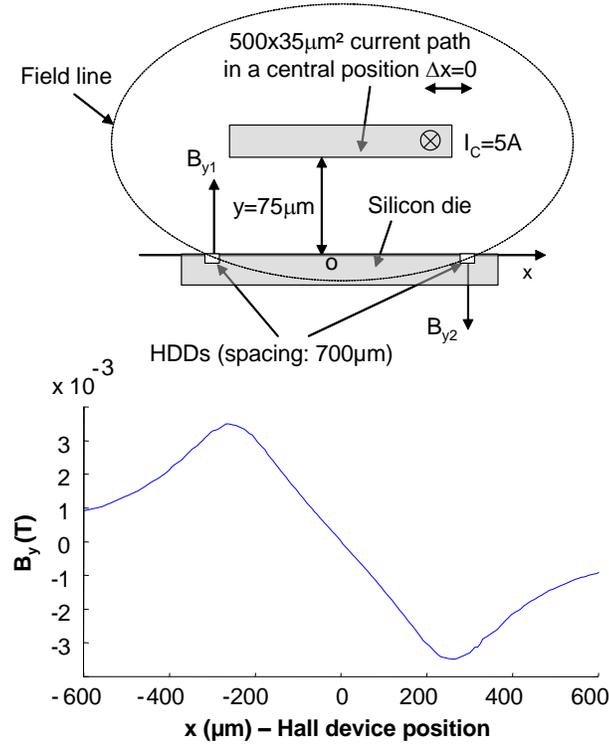


Fig. 2. Cross section and FLUX2D<sup>®</sup> simulation result for  $I_C=5A$  rms.

In the case presented in figure 2, the parasitic field  $B_p=0$  and the curve represents the amplitude of  $B_y=B_{Cy}$  according to the position of the HDD along the  $x$  axis. As expected, the simulation results show that the magnitude of  $B_y$  is symmetrical with respect to the position of the current path. It features maximum absolute values of more than 3mT at roughly  $x=\pm 275 \mu\text{m}$ .

The field  $B_{diff}$  is now defined as the difference between the fields applied upon each HDD such as

$$B_{diff} = B_{Cy1} - B_{Cy2} \quad (3)$$

Values as high as  $|B_{diff}|=6\text{mT}$  can be expected for  $I_C=5A$  rms if the HDDs are placed at the points where the magnitude of  $B_y$  is maximum, i.e. at  $\pm 275 \mu\text{m}$  with respect to the center of the current path. Yet it could be interesting to place the HDDs at a distance a little greater, for instance at  $\pm 350 \mu\text{m}$ , which has

minor consequences on the magnitude of  $B_{\text{diff}}$  but helps reducing its variations when the current path is shifted by  $\Delta x$  from its ideal central position (figure 2:  $\Delta x=0$ ) as depicted on figure 3. This aspect is advantageously exploited at packaging as discussed in section VI.

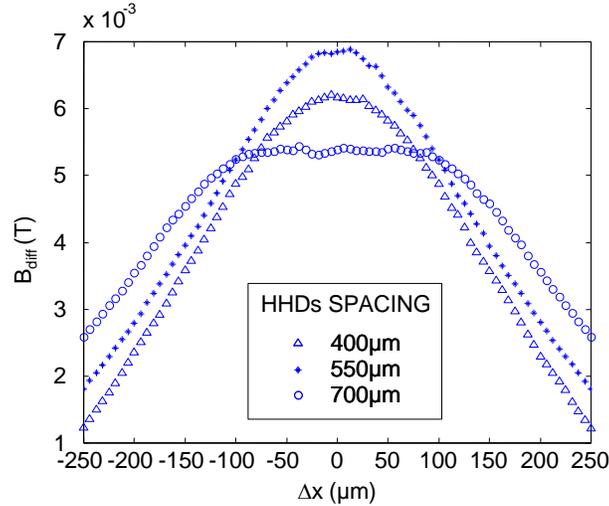


Fig. 3. Evolution of  $B_{\text{diff}}$  according to the current path's shift for 3 values of HHD spacing.

The accuracy of the current sensor mainly depends on the signal to noise ratio of both the HHDs and the instrumental chain. As a matter of fact proper signal conditioning allows efficient resolution enhancement of the silicon HHDs that feature weak sensitivity in comparison with other technologies but that can advantageously be embedded together with the appropriate CMOS integrated electronics without any additional post-processing.

### III. SENSING FRONT-END

As presented in figure 4, the analog sensing front-end is made up of the three following staple elements:

- A HHD used as the magnetic field sensing element.
- A low-noise biasing structure.
- A low-noise pre-amplifier.

The goal of this module is to raise the sensing element's output signal  $V_H$  to a level high enough to be exploited for further signal processing. Production of a high signal to noise ratio is here the major design constraint.

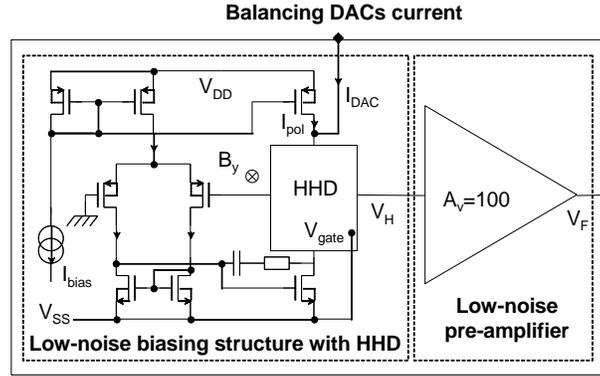


Fig. 4. Structure of the magnetic field sensitive front-end.

The HHD is based on a conventional N-well resistor structure built in the P-type substrate of the CMOS technology. Yet it features a polysilicon gate drawn upon the N-well layer. The CMOS technology implies that a thin oxide is thermally grown before the polysilicon gate deposition, leading to a Si/SiO<sub>2</sub>/Polysilicon structure similar to a PMOS transistor active area. When a negative voltage is applied upon the gate, a depletion zone appears in the silicon under the oxide. As shown in figure 5, this zone reduces the effective thickness,  $t_e$ , of the HHD, which increases its current related sensitivity given by:

$$S_I = \frac{K_H}{I_{pol}} = \frac{GR_H}{t_e} \quad (4)$$

where  $R_H$  denotes the Hall coefficient,  $I_{pol}$  is the biasing current of the HHD and  $G$  stands for a geometry dependent correcting factor [5].

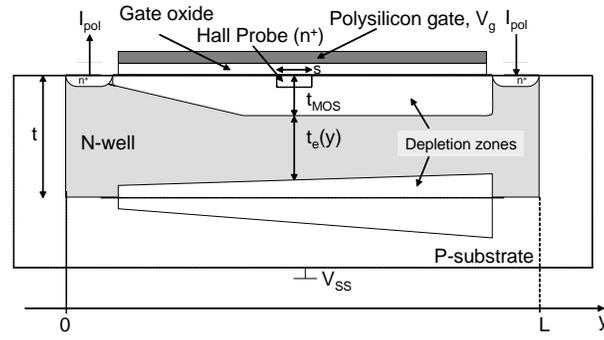


Fig. 5. Cross-section of the gated HHD.

From the classical theory of the PMOS structure [7], we can establish that when  $V_g$  become lower than the MOS structure threshold voltage, the extension of the depletion zone reaches a maximum value. The profile of this depletion zone along the HHD is then as shown on figure 5. Nevertheless, in submicron technologies, the gate oxide cannot be considered as a perfect barrier for electrons, which can tunnel through this very thin oxide. In that case, the HHD can be seen as a MOS tunnelling diode and the depletion zone further extends, placing the MOS tunnelling diode into deep depletion [8]. Yet, in either case, for a given biasing current of the HHD, i.e.  $I_{pol}$ , the best sensitivity is obtained for  $V_g = V_{SS}$ , the lower supply voltage. Tests carried out on  $50 \times 26 \mu\text{m}^2$  prototypes, built in a  $0.6 \mu\text{m}$  CMOS technology, revealed a sensitivity  $S_I$  as high as  $113 \text{V/AT}$  [6].

The HHD is inserted in the output stage of an operational amplifier that simultaneously performs the current biasing with  $I_{pol} = 1.5 \text{mA}$  and the HHD's output voltage referencing to ground. The chip's power supply is symmetrical (i.e.  $\pm 2.5 \text{V}$ ).

The Hall voltage  $V_H$  is pre-amplified by the gain stage  $A_v = 100$  and the front-end's output signal is

$$V_F = A_v S_I I_{pol} B_y + V_{off} \quad (5)$$

where  $B_y$  is the vertical component of the total magnetic field and  $V_{off}$  is the offset voltage from both the biased HHD and the pre-amplifier itself.

Since the total noise of an electronic structure tends to increase with the number of devices, we opted for operational transconductance topologies owing to the small number of transistors they require. The front-end reaches  $5.2 \mu\text{T}$  resolution on a bandwidth extending from  $5 \text{Hz}$  to  $1 \text{kHz}$ . Details on the design of the low-noise biasing amplifier and the signal preamplifier are available in [6].

#### IV. DIFFERENTIAL INSTRUMENTAL CHAIN

The common mode signal rejection for the structure shown in figure 1 is performed by connecting the two identical front-end modules to a differential instrumental chain (figure 6).

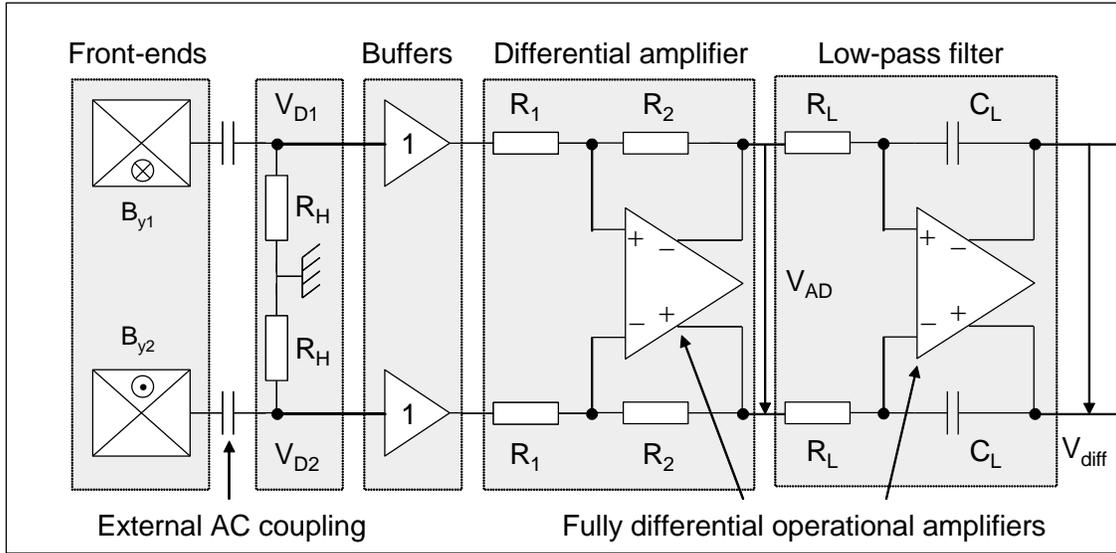


Fig. 6. Architecture of the differential instrumental chain.

##### A. AC coupling

The first stage of this fully analog unit is a pair of first order high-pass filters (HPFs) referenced to ground for AC coupling, which allows offset suppression that might clamp the differential amplifier's output. The cut-off frequency is about 10Hz in order to let unfiltered the first 50Hz harmonic of the current to be measured. The HPFs also dramatically reduce the  $1/f$  noise of the front-ends that mainly contributes to the total noise in CMOS systems dedicated to low-frequency applications. Higher cut-off frequency would help improving the signal to noise ratio but it would also induce higher phase shift and harmonics measurement problems.

The voltage downstream the filters has no DC component anymore and in the band pass, its expression is given by:

$$\begin{cases} V_{D1} = A_{v1} S_{I1} I_{pol1} B_{y1} = K_1 B_{y1} \\ V_{D2} = A_{v2} S_{I2} I_{pol2} B_{y2} = K_2 B_{y2} \end{cases} \quad (6)$$

A highly resistive layer has been used for the filter's resistor integration ( $R_H=500k\Omega$ ). As for the

coupling capacitors they are external to the circuit because of the low cut-off frequency, which would imply unacceptable silicon surface in case of integration.

### B. Differential amplifier

The voltages  $V_{D1}$  and  $V_{D2}$  are applied on either input of a fully differential amplifier for further signal amplification. The differential amplifier's output voltage depends on the gain resistor's ratio,  $A_D=R_2/R_1$ :

$$V_{AD}=A_D(V_{D1}-V_{D2}) \quad (7)$$

In order to achieve proper common mode rejection, the amplifier needs to be self-immune against common mode parasitic. The best way to achieve efficient rejection consists in using fully differential operational amplifiers with balanced differential outputs [9]. The balancing principle presented in figure 7 is based on the control of the output operating point through a common mode feedback amplifier. In our case this operating point is 0V, midway between the symmetrical power supply voltages.

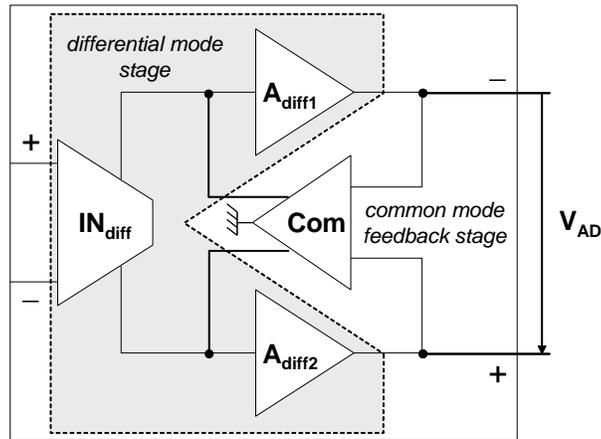


Fig. 7. Fully differential operational amplifier structure.

Stability is the major concern for back-fed structures. The common mode control system actually needs to be efficient on the whole differential amplifier's bandwidth. The solution applied here to tackle down this problem consists in using identical topologies for both the differential structure and the common mode control feedback amplifier as proposed in [10].

The schematic topology of the fully differential operational transconductance amplifier (OTA) used is given in figure 8. The output  $OUT+$  and  $OUT-$  respectively correspond to the positive and negative

outputs of figure 7. The inputs  $V_{P1}$ ,  $V_{P2}$ ,  $V_{P3}$  and  $V_{CONT}$  are used for static biasing.

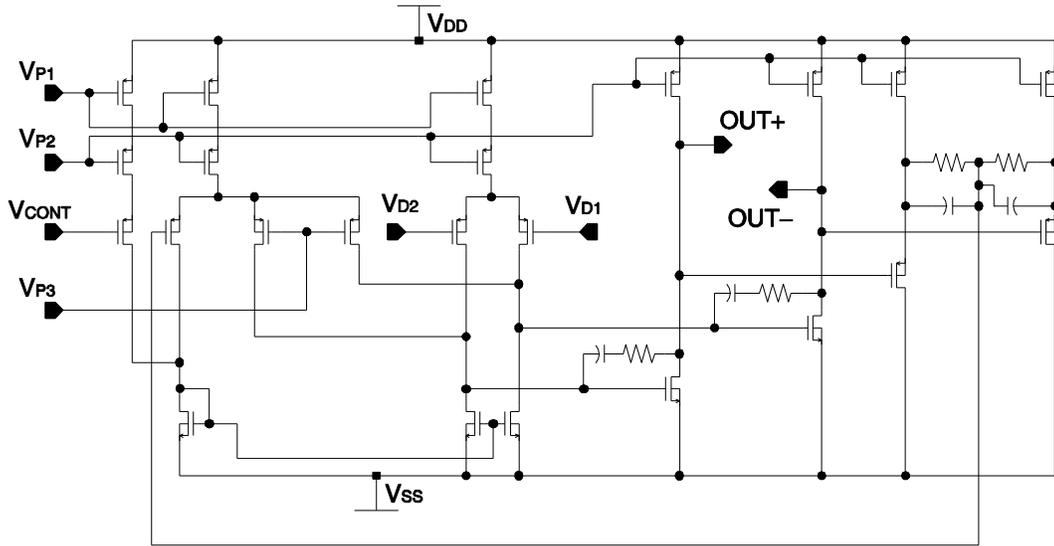


Fig. 8. Fully differential OTA.

### C. Active Low-pass filter

The accuracy of the current sensor directly depends on the acceptable noise level. Low-pass filtering is then necessary in order to limit the whole system's bandwidth and thus to reduce the total equivalent noise at the output of the HHDs, which essentially results from the front-ends. Indeed, the noise of the differential chain is divided by the front-end's preamplifier gain and has consequently minor contribution when referred to the HHDs' output.

The structure of the first order active filter is based on the same fully differential OTA as for the differential amplifier. The cut-off frequency has been set to 1.5 kHz in order to allow 30<sup>th</sup> (25<sup>th</sup>) harmonic detection of the current to be measured. According to the preliminary field estimate (about 3mT on each HHD for  $I_C=5A$ ) and the front-end's resolution on this bandwidth (about 5 $\mu$ T), the expected precision of the current sensor should then be better than the targeted 0.5% accuracy for  $I_C=5A$  nominal current.

This filter also has an anti-aliasing function for future on-chip implementation of an analog to digital converter at the instrumental chain's output.

#### D. Limitations of the instrumental chain

In the light of expressions (2), (3), (6) and (7), for  $K_1=K_2$ , any common mode parasitic fields  $B_p=B_{p1}=B_{p2}$  is perfectly rejected. Thus the output voltage  $V_{AD}$  only depends on the difference between the vertical components of the useful magnetic signal produced by the current  $I_C$  to be measured:

$$V_{AD}=A_D K_1 (B_{Cy1} - B_{Cy2}) \quad (8)$$

As a consequence, exact lateral positioning of the current path between the HHDs is not required owing to the differential sensing structure. This characteristic is quite important in terms of packaging post-processing cost.

However, in practice  $K_1$  might be different from  $K_2$  because of possible fabrication-related mismatching of the front-ends. In order to evaluate the consequences of a possible imbalance let us first consider the following variable changes:

$$\begin{cases} B_{Cy1} - B_{Cy2} = B_{diff} \\ \frac{B_{Cy1} + B_{Cy2}}{2} = B_{com} \end{cases} \Rightarrow \begin{cases} B_{Cy1} = B_{com} + \frac{B_{diff}}{2} \\ B_{Cy2} = B_{com} - \frac{B_{diff}}{2} \end{cases} \quad (9)$$

When the current path is centered between the HHDs,  $B_{com}=0$ . Otherwise,  $B_{com}$  is a common mode induction superimposed to  $B_{diff}$ . If a common mode parasitic signal  $B_p$  appears and adds to the useful  $B_{com}$  signal, the instrumental chain's output voltage  $V_{diff}$  (see figure 6) reads:

$$V_{diff} = A_D \left[ (K_1 - K_2)(B_{com} + B_p) + \frac{K_1 + K_2}{2} B_{diff} \right] \quad (10)$$

assuming that the low-pass filter has unity gain on its bandwidth. This equation shows that in case of imbalance ( $K_1 \neq K_2$ ) it is impossible for the differential chain to discriminate between  $B_{com}$  and  $B_p$ , and to achieve proper EMC. As a consequence balancing is then mandatory.

## V. BALANCING SYSTEM

The instrumental chain features an auto-balancing system in order to give efficient EMC performances to the current sensor.

During the balancing process, no current  $I_C$  is injected in the path. The principle basically consists in applying only a common mode magnetic field on the Hall devices. This is advantageously achieved with

present sub-micron CMOS technologies that provide at least 3 metal layers and thus enable coil integration [3]-[11] upon each HHD with great precision (figure 9). Thanks to the small surface of the HHDs ( $26 \times 50 \mu\text{m}^2$ ) and hence of the coils, a 2mT peak to peak (p-p) common mode field ( $B_{bal}$ ) is obtained by injecting a 500Hz periodic current  $I_{coil}=20\text{mA}$  p-p in the serially connected coils.

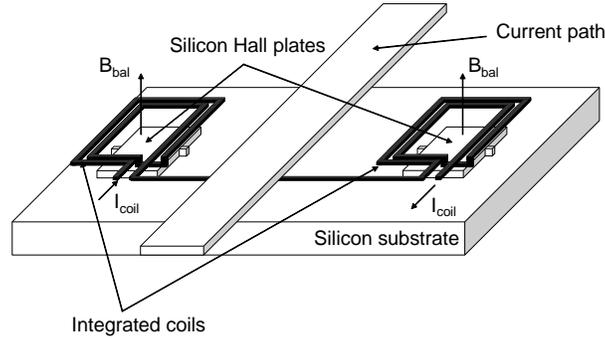


Fig. 9. Current path and integrated coils positioning on the HDDs.

The consequence of possible imbalance in the differential chain is a 500Hz residual AC signal  $V_{diffres}$  at the output of the chain:

$$\begin{aligned} V_{diffres} &= A_D (K_1 - K_2) B_{bal} \\ &= A_D (A_{v1} S_{I1} I_{pol1} - A_{v2} S_{I2} I_{pol2}) B_{bal} \end{aligned} \quad (11)$$

The whole instrumental chain is then trimmed by controlling two 8-bit digital to analog converters (DACs) that either increase or decrease the biasing current  $I_{pol2}$ , and thus increase or decrease the absolute sensitivity of the HHD of front-end 2, via the input appearing in figure 4, until  $V_{diffres}$  is cancelled. The least significant bit of the DAC was chosen corresponding to  $1\mu\text{A}$ .

This process has been automated by integrating on the same substrate a digital control unit (figure 10). A comparator with hysteresis evaluates the residual periodic voltage. The value of its hysteresis directly depends on the instrumental chain's output noise level and avoids spurious switching of the comparator.

In case of imbalance this comparator delivers a 500Hz square signal as long as the amplitude of  $V_{diffres}$  is higher than the hysteresis level  $V_{hyst}$  and remains in a still digital high or low position at balance. The HDDs' biasing currents are initially theoretically identical. In case of imbalance the lower 8-bit current DAC is scanned starting from the maximum current ( $-255\mu\text{A}$ ), which can be sunk from the biasing

current of HHD of front-end 2, up to  $0\mu\text{A}$ . If balance hasn't been reached the upper 8-bit current DAC is scanned starting from  $0\mu\text{A}$  up to the maximum current ( $255\mu\text{A}$ ) that can be added to the biasing current of HHD of front-end 2. This trimming-current range is sufficient to correct practical fabrication-related mismatching. Moreover, the  $1\mu\text{A}$  increment step provides a balancing accuracy better than 0.2% for a sensor initial biasing current  $I_{\text{pol}}=1.5\text{mA}$ .

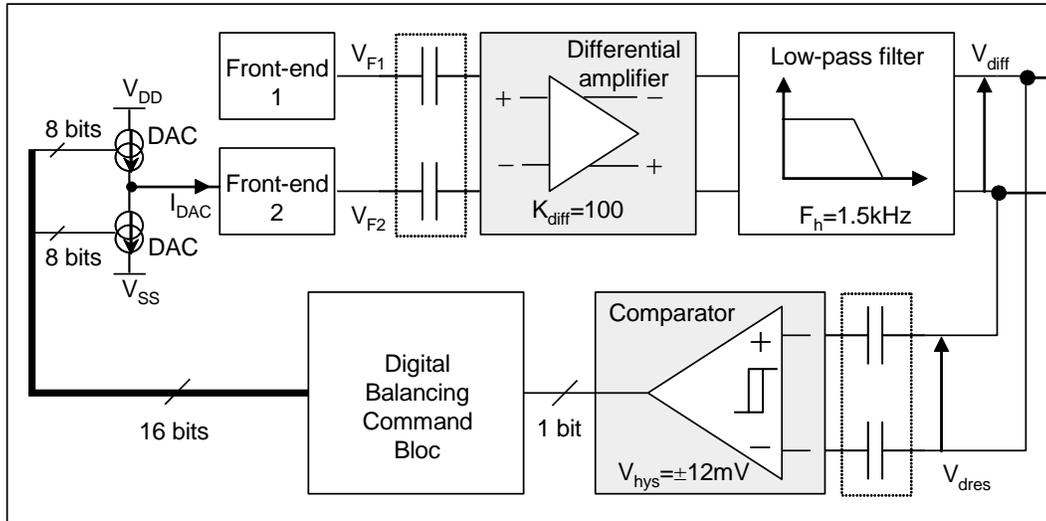


Fig. 10. Structure of the complete microsystem.

## VI. PACKAGING AND EXPERIMENTAL RESULTS

The total oxide thickness of standard CMOS technologies cannot guaranty high galvanic isolation. An external  $I_C$  current path solution has then been retained. The lowest current detection limit is ruled by the front-ends' resolution and the magnitude of the magnetic field generated by the current to be measured. The front-ends' resolution, which is actually strongly related to the silicon HHDs resolution and the CMOS technology noise performances has been optimized as discussed in section III.

At this point, the only way to further improve the current sensor's sensitivity is to place the current strip as close to the HHDs as possible. The chosen solution consists in etching the path on a highly isolating  $50\mu\text{m}$  thin-film flexible circuit. As already mentioned in section II, this flexible circuit doesn't require great accuracy positioning. This remark is particularly true if the spacing between the HHDs is slightly bigger, i.e.  $700\mu\text{m}$  (figure 2), than the ideal value, i.e.  $550\mu\text{m}$  corresponding to the spacing for

which the HHDs get maximum amplitude field. As shown in figure 3, in our case (i.e. HHD spacing =  $700\mu\text{m}$ ), a  $\pm 100\mu\text{m}$  accuracy on the current path positioning is sufficient. Not only does this feature ease the positioning and sealing of the flexible circuit but it also minimizes the need for calibration since the shifting has no significant consequence on the magnitude of  $B_{\text{diff}}$  (almost constant) on the range  $\Delta x \approx \pm 100\mu\text{m}$ . Of course this implies that the distance,  $y$ , between the flexible circuit and the chip's surface has to be constant, i.e.  $75\mu\text{m}$ . Yet, even though the isolation layer of the flexible circuit has a guaranteed thickness of  $50\mu\text{m}$ , the thickness of an adhesive layer is liable to variations. Therefore, during packaging, the thin-film flexible circuit is kept in position over the chip's surface and a specific coating is deposited to perform the sealing (figure 11). Such a process ensures both minimal as well as constant distance between the current path and the HHDs from one current sensor to the other. Measurements showed that isolation better than  $5\text{kV}$  is ensured with the thin-film material used.

According to standards, practical external parasitic field sources encountered in most industrial applications are located at distances at least greater than  $1\text{cm}$ . Furthermore, the copper path has a  $500 \times 35\mu\text{m}^2$  section and the distance between the HHDs is chosen close to  $700\mu\text{m}$  as discussed above and in section II. With this spacing, the parasitic field gradient from one sensing element to the other is negligible. As a consequence, the sensor achieves proper EMC characteristics.

In order to help thermal power dissipation the path can be wider at each extremity.

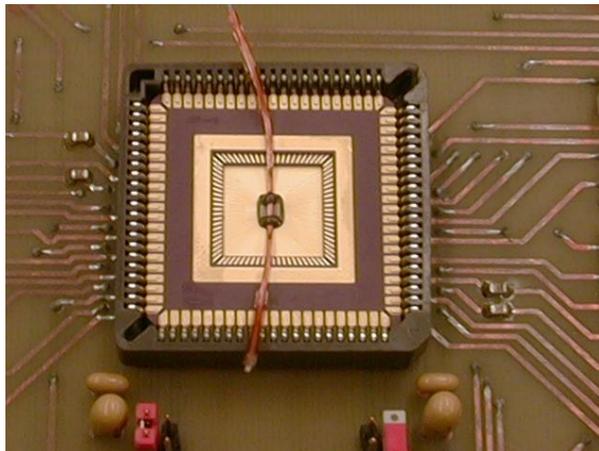


Fig. 11. Integrated current sensor prototype.

The layout of the microsystem fabricated in a  $0.6\mu\text{m}$  CMOS technology is proposed in figure 12. The chip's surface is  $2\times 3\text{mm}^2$ . The bonding pads are only located on two opposite edges to facilitate the current path's positioning. The presented prototype features numerous additional pads for test purpose.

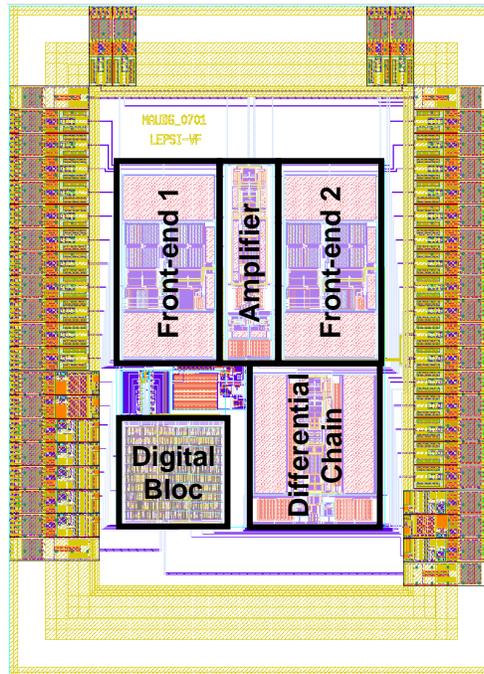


Fig. 12. Layout of the microsystem.

Figure 13 presents the response of the prototype to a 50Hz and 50mA rms current. Results clearly show that the sensor is able to detect and measure currents lower than 50mA rms.

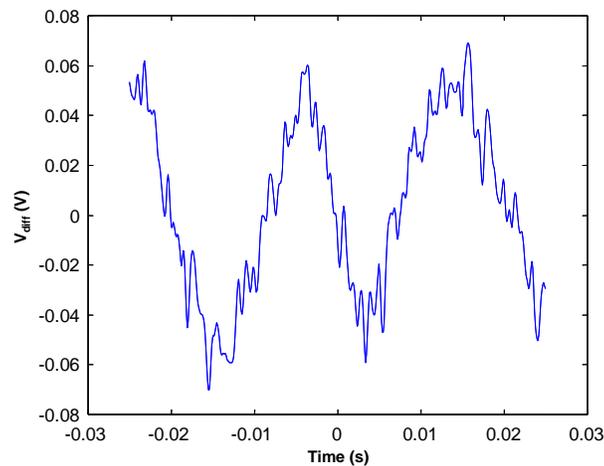


Fig. 13. Current sensor's response to a 50Hz and 50mA current.

Additional tests have been carried out in order to extract linearity and temperature characteristics of the sensor according to international norms for current sensors and energy meters (IEC44-1 and IEC1036).

The linearity error (ENL) is defined as follows:

$$ENL=100 \times \frac{|I_{eff}-I_C|}{I_C} \quad (12)$$

where  $I_{eff}$  is the measured rms current and  $I_C$  is the calibrated current at the input of the sensor. Figure 14 shows the ENL obtained by averaging the output signal of the instrumental chain for further noise reduction. This averaging is performed on 500 points covering 10 periods of the 50Hz current in order to determine  $I_{eff}$  used in the ENL calculation. Accuracy better than 0.5% on a range extending from 250mA to 5A has been verified, which enables class 1 qualification of the current sensor.

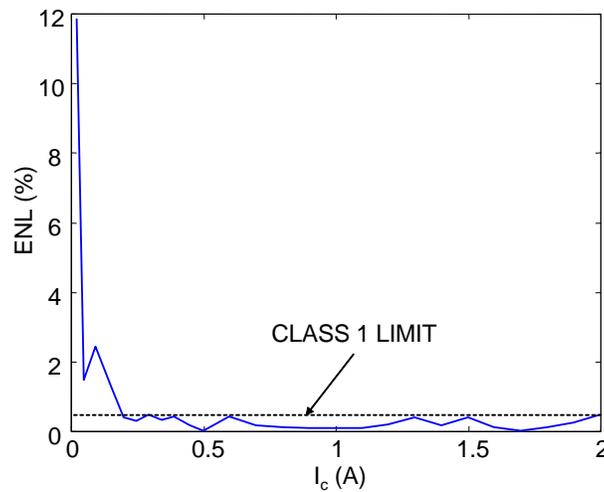


Fig. 14. Linearity error of the current sensor.

The temperature tests have been carried out by injecting a permanent 1A nominal  $I_C$  current and submitting the sensors to temperature variation extending from  $-20^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$ . The chip was glued in a ceramic standard package thanks to a soft glue that helps limiting the piezoresistive effect on the HHDs [12]. The overall output variation is smaller than  $\pm 0.5\%/^{\circ}\text{C}$  on the whole temperature range, which also enables class 1 qualification of the current sensor (figure 15).

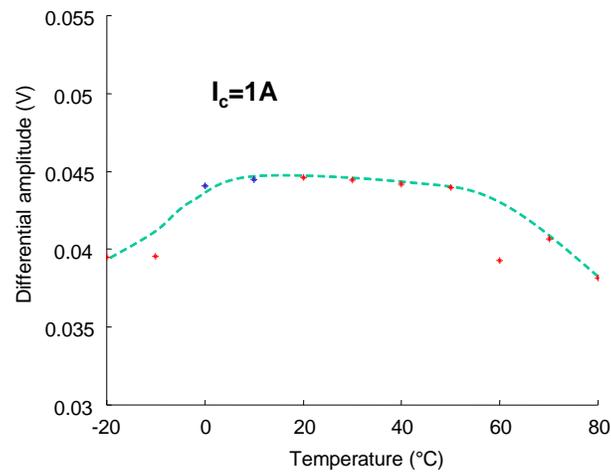


Fig. 15. Temperature effect on the current related sensitivity.

The auto-balancing sequence has been monitored by measuring the biasing voltage drop on the HHDs controlled by the DACs. Only one prototype out of five needed balancing. As shown in figure 16, the biasing current needs to be decreased in order to perform suitable balance of the instrumental chain. As a consequence, the final biasing voltage drop (i.e. after the balancing sequence) is lower than the initial value.

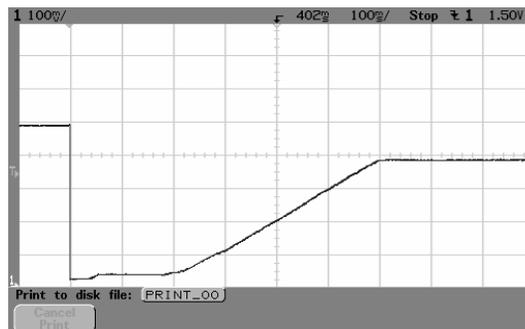


Fig. 16. Biasing voltage drop of the controlled HHD during balancing sequence.

These variations should take their origins in the freeze-out effect the submicronic technologies below  $0.8\mu\text{m}$  suffer [12] as well as in the variation of the biasing current of the HHDs, not stabilized in temperature.

Figure 17 shows the result of the balancing on the sensor's behaviour when excited by both a 1A-50Hz current to be measured and a common mode magnetic field with  $250\mu\text{T}$  amplitude and 500Hz frequency.

The residual ripple induced by the common mode signal when the differential chain is imbalanced clearly disappears after the balancing sequence.

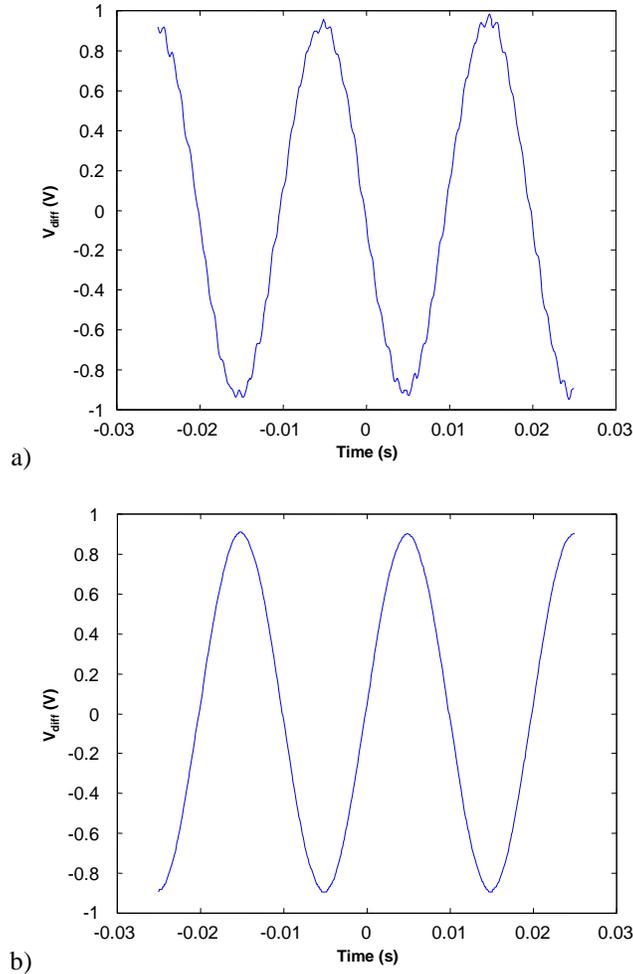


Fig. 17. Differential chain output: a) before balancing, b) after balancing.

## VII. CONCLUSION

A current sensor exclusively based on a standard CMOS microsystem has been presented. We demonstrated that improved silicon Hall effect devices allow accurate sensor design without any additional post-processing but only through appropriate analog and mixed signal processing and packaging. This sensor allows 5A nominal 50Hz (60Hz) AC current measurement with 0.5% accuracy over 1.5kHz bandwidth and qualifies for class 1 energy measurement applications. It is intended to be used in industrial applications where 30<sup>th</sup> (25<sup>th</sup>) harmonic detection is required.

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