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An HDL-Based Methodology

for VLSI Design of AC Motor Controller

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Abstract –This paper presents a methodology to design a CMOS Very Large Scale Integration (VLSI) controller for Alternating Current (AC) motor control. Step by step, Top-down methodology based on Hardware Description Languages (HDL) with mixed simulation was used to study digital adaptation and architecture implementation of the control algorithm. An application using the proposed methodology was studied: the Direct Torque Control (DTC) of an AC motor. The DTC is described and VLSI examined. Analog and digital models were used to describe the algorithm implementation, specific binary format and architecture. The Register Transfer Level (RTL) model for DTC controller was validated by mixed simulation. The ASIC layout was created using Austria Mikro System standard cell library for 0.8µm CMOS. Finally, we compared this VLSI approach with software implementation and co-design methodology.

1. INTRODUCTION

AC motor control has made significant progress since the 1980's thanks to microelectronic advanced features in digital processors. Most research has focused on control strategies based on digital processors, such as Microprocessors or Digital Signal Processors (DSP). However, with Application Specific Integrated Circuit (ASIC) technologies [1], mixed and digital AC drive systems can be integrated in a single chip. VLSI can be used for real-time control requiring reliability and performance [2], reducing the number control system components and guaranteeing architecture confidentiality.

In this paper, the authors first present a general Top-down methodology based on HDL to improve digital VLSI ASIC design for AC motor control. Methodology design flow is described in detail in section 2. This

methodology is used to design a specific vector control of AC motor, called Direct Torque Control [3], [4]. DTC has a simplified structure and requires no mechanical sensors. The DTC case will be used to describe the proposed methodology step-by-step.

2. HDL-BASED DESIGN METHODOLOGY

2.1. Design approach

Our research focussed on the System-On-Chip (SOC) design of an AC motor control system, which required semi-custom standard-cell-based ASIC. To do this, we needed to model and simulate a complete AC drive system. High level design tools, such as Matlab-Simulink CAD, are used to design Microprocessor, Micro-controller or DSP digital control. In Matlab-Simulink, "DSP Builder" or "System Generator" dedicated tools, by Altera and Xilinx Inc. respectively, can be used to design Field Programmable Gate Arrays (FPGA). Moreover, motion control Intellectual Property-cores (IP) can be developed using HDL and targeting Programmable Logic Devices or FPGA or bought from specialized IP design firms [5]. However, these solutions do not allow final semi-custom ASIC design. In our approach, using existing methodology [6], we developed an improved HDL-based design flow for VLSI design of AC motor controller. The most commonly used digital HDL are Verilog or Very High-speed integrated circuit Hardware Description Language (VHDL). We chose VHDL for high level and behavioral digital control design. VHDL, based on discrete time models, can be used for behavioral modeling of power electronics, analog elements or AC motors ([7], [8]). However, VHDL is based on event-driven techniques; without temporal analysis, it is not the HDL best suited for general drive system design. Hence, we chose analog HDL which can describe differential and algebraic equations that vary continuously with time. Therefore, for modeling analog and power elements of the AC motor drive system, we chose SpectreHDL, a Cadence proprietary analog language standardized in 1994.

We developed an HDL-based Top-down design where the digital controller was linked, in real context, to sensors, power and analog components. To ensure predictability of final ASIC prototype, CAD tools simulate the digital closed-loop control with analog and power elements (power converter, sensors, AC motor, interface, …). Thus, the design can be evaluated quickly. Simulation before prototyping allows us to correct eventual errors more easily and cost effectively. Top-down conception allowed us to design the control IC from the functional specifications to the final implementation details. Moreover, the use of HDL throughout the design provides continuous system validation and makes the digital design independent of the target technology. This methodology is presented in Fig. 1.

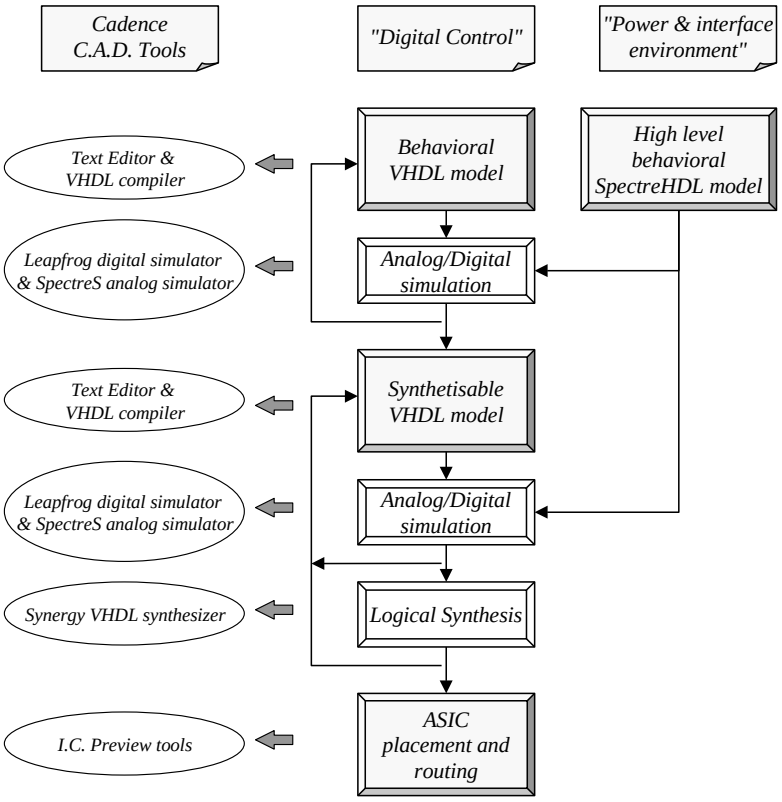


Fig. 1 – *Methodology design flow*.

First, in the behavioral VHDL model of AC motor controller, after validating the control, the designers examine the digital adaptation of the control algorithm. This step is dedicated to algorithm implementation; it optimizes control calculations and determines the digital properties. Next, a final synthetisable VHDL model is described at Register Transfer Level (RTL). This VHDL model corresponds to an ASIC architecture. Some structural descriptions can be easily and quickly tested by reusing VHDL functions previously validated [9] to reduce silicon area and improve algorithm treatment time. At each step of the two first stages, the control is functionally validated by mixed simulation in both the power and analog environments. Mixed VHDL-SpectreHDL simulation is a key element in our design flow and is described in detail in section 2.2.

The final stage is physical design. Synthesis, place and route of the final RTL model of the digital controller are determined using Cadence. The objective is to create the digital controller in standard CMOS technology ASIC with the same RTL description. FPGA can also be prototyped. However, FPGA macro-functions have not been used and synthesis results give no information about maximal frequency and silicon area ASIC.

2.2. SpectreHDL/VHDL mixed simulation

The design of the VLSI-based AC motor controller can be improved using mixed simulation. Indeed, analog models (sensors, amplification, electronic power, load, etc.) can be designed and included in a mixed environment to study the digital control model in closed-loop. Hence, a mixed simulation environment based on Cadence CAD tools and on VHDL and SpectreHDL languages was developed.

To model the digital controller, we used a standard digital VHDL language. Ideal analog and power elements were modeled using SpectreHDL. For mixed simulation, SpectreHDL high level behavioral models for ideal power and analog elements were written. Fig. 3 shows general mixed simulation environment for an AC motor control: the *power block* SpectreHDL models an AC motor, load and power electronics, the *interface block* SpectreHDL models electrical sensors, acquisition electronic and Analog-Digital Converters (ADC) ; the *control block* VHDL models the AC motor control algorithm.

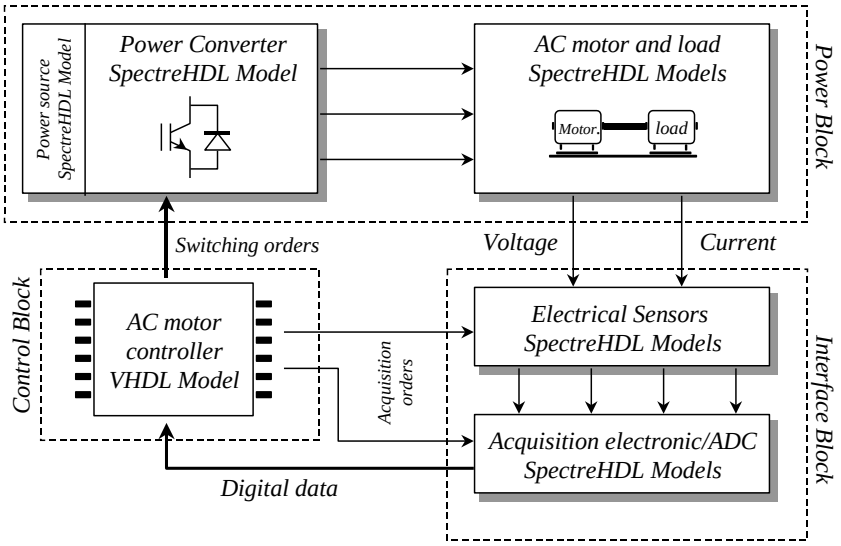


Fig. 2 – *Mixed simulation environment.*

Two simulators were used: Leapfrog simulator for the VHDL description and SpectreS simulator for SpectreHDL models (Fig.3). Simulators communicate through Inter Process Communication (IPC) based on UNIX sockets. IPC functions are automatically controlled and are transparent for the users. The VHDL model of the digital controller can be thereby simulated and functionally validated throughout the design flow in real power and analog context.

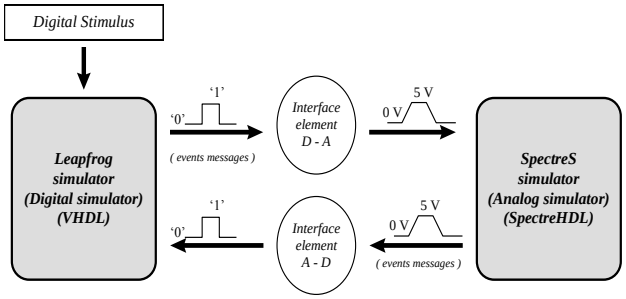


Fig. 3 - *Communication between analog and digital simulators.*

3. BEHAVIORAL ANALYSIS AND MODELING IN DTC CASE

3.1. DTC basic principle

The basic principle of DTC of an AC motor is to calculate the instantaneous values of stator flux φ_s and electromagnetic torque Γ_{elm} in the AC motor, Fig.4 [10].

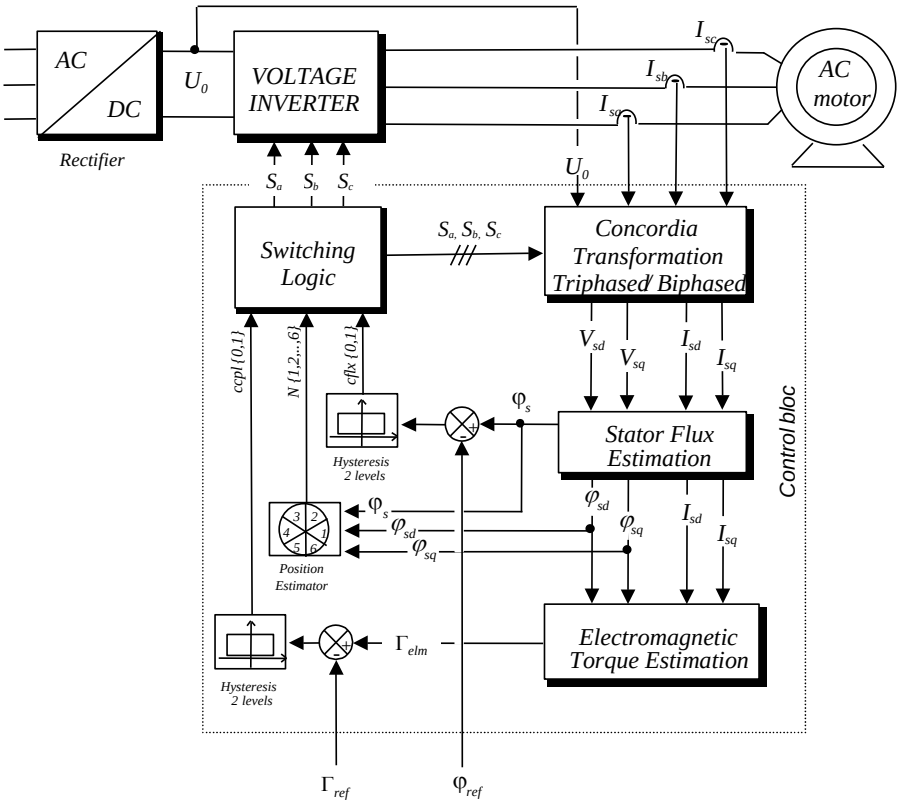


Fig. 4 - *Direct Torque Control structure.*

Stator voltage components (V_{sd}, V_{sq}) on perpendicular (d,q) axis are determined from measured values (U_0 and $I_{sa,b,c}$), Boolean switching controls (S_a, S_b, S_c) by:

$$\begin{cases} V_{sd} = \sqrt{\frac{2}{3}} \cdot U_0 \cdot \left(S_a - \frac{1}{2}(S_b - S_c) \right) \\ V_{sq} = \frac{1}{\sqrt{2}} \cdot U_0 \cdot (S_b - S_c) \end{cases} \quad (1)$$

And stator current components (I_{sd}, I_{sq}):

$$\begin{cases} I_{sd} = \sqrt{\frac{3}{2}} \cdot I_{sa} \\ I_{sq} = \frac{1}{\sqrt{2}} \cdot (I_{sb} - I_{sc}) \end{cases} \quad (2)$$

Hence, with expression (1) and (2), stator flux components are calculated as:

$$\varphi_{sd,q}(t) = \varphi_{sd,q}(0) + \int_0^t V_{sd,q}.dt - R_s \cdot \int_0^t I_{sd,q}.dt \quad (3)$$

And the stator square flux modulus as:

$$\varphi_s^{\,2} = \varphi_{sd}^{\,2} + \varphi_{sq}^{\,2} \quad (4)$$

Electromagnetic torque calculation uses flux components (3), current components (2) and p, pair-pole number of the induction machine:

$$\Gamma_{elm} = p \cdot (\varphi_{sd} \cdot I_{sq} - \varphi_{sq} \cdot I_{sd}) \quad (5)$$

Every calculation cycle, a digital table gives the Boolean switching controls $S_{a,b,c}$ for voltage inverter switches. These signals depend on stator flux angular position and hysteresis comparison.

3.2. High level functional validation

DTC principle is functionally validated, using real standard VHDL format [11]. This format avoids quantization errors due to data binary format. We could functionally validate the control principle with a high level behavioral model of AC motor control by comparing mixed simulation results with waveforms from an analog SpectreHDL model of the AC motor. Mixed simulation results validated the mixed simulation environment and particularly ideal high level SpectreHDL models. Figures 5 and 6 present the mixed simulation for electromagnetic torque with parameters shown in the appendix. Fig 5 presents estimated torque response to a step from 5 N.m to 10 N.m at t=20 ms. Torque was correctly regulated around the reference with an accuracy corresponding to the defined hysteresis band.



Fig. 5- *Torque response to a step from 5 N.m to 10 N.m at t=20 ms.*

Fig. 6 shows torque simulation results for AC motor analog SpectreHDL model and for real VHDL model of the controller. Electromagnetic torque was correctly regulated around torque reference (Γ_{ref} = 10 N.m) with an accuracy corresponding to the hysteresis band. Figure 6 shows agreement between analog torque, obtained from SpectreHDL model, and digital estimated torque. The time shift between the two signals corresponded to treatment time to compute torque from analog values.

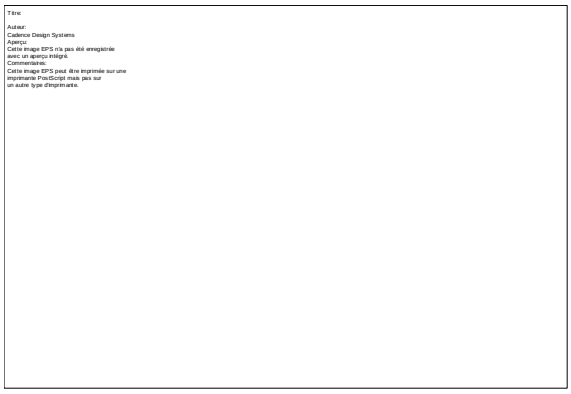


Fig. 6 – *Zoom on analog and digital torque.*

3.3. Digital adaptation

In the ASIC design, specific digital properties had to be studied: data binary format (word length, fixed or floating point), mathematical and numerical calculation methods and quantitization effects. Final digital properties were defined to minimize estimation error, which would have degraded control performance.

3.3.1. DTC algorithm optimization

Voltage and current integration terms (3) were calculated separately, using different numerical integration methods for a better accuracy. The choice of integration method depended on the signal shape. Thus, since voltage components, V_{sd} and V_{sq}, are calculated from the constant voltage U_0 and Boolean switching controls $S_{a,b,c}$ (1), the rectangle method was used for the voltage integral calculus. Since the currents are sinusoidal, the

trapezoid method was used for current integral calculus. Furthermore, square flux modulus was calculated to avoid complex implementation of square root function (4).

Fig. 7 shows the improved digital algorithm for DTC at kT_s time, where T_s is the sampling time. Each step defines specific calculations, which were carried out either in parallel or sequentially.

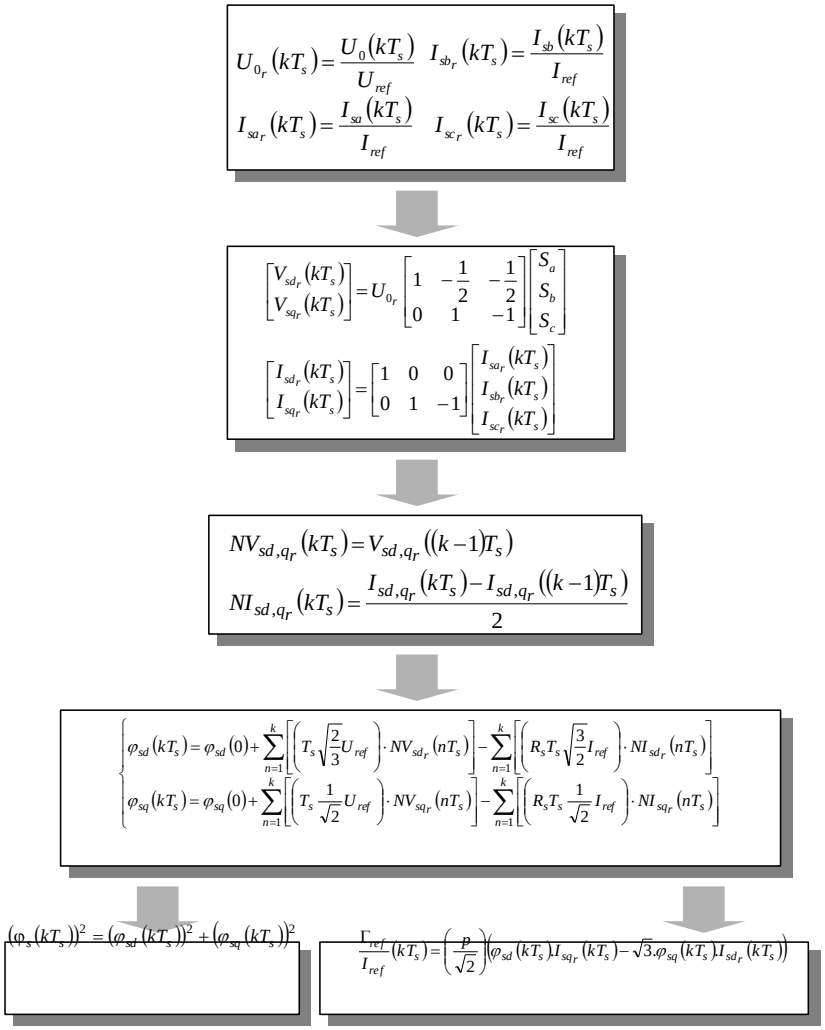


Fig. 7 – *Digital adapted DTC Algorithm.*

First, analog signals were sampled and digitized. To normalize sampled magnitudes of ADC input in [-1, +1], scale factors (I_{ref} and U_{ref}) were applied to the analog signals. Reduced values, noted with r suffix, were used to calculate current and voltage components.

To reduce the number of multiplication for $\varphi_{sd,q}$ calculations (3), we grouped constants (sampling time, scale factors, Concordia constants and stator resistor value) into four terms: $\left(T_s\sqrt{\frac{2}{3}}U_{ref}\right)$, $\left(T_s\frac{1}{\sqrt{2}}U_{ref}\right)$, $\left(R_sT_s\sqrt{\frac{3}{2}}I_{ref}\right)$ and $\left(R_sT_s\frac{1}{\sqrt{2}}I_{ref}\right)$.

Finally, after iterative calculations for $\varphi_{sd,q}$, square flux modulus and electromagnetic torque are calculated in parallel.

3.3.2. Specific binary format

We chose a specific binary fixed-point format, presented Fig. 8, since the floating-point format would require too long execution time for mathematical operators and occupy too much silicon.

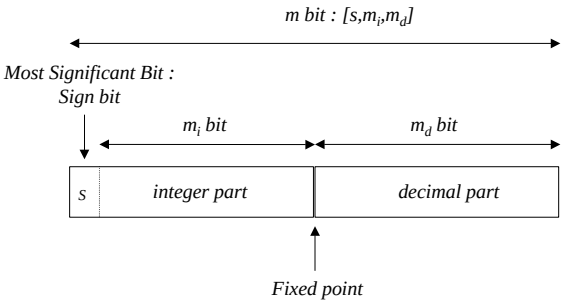


Fig. 8 – *Fixed-point format [s,m_i,m_d]*.

To define the specific fixed-point format, we took two major control characteristics into account:

- Maximal value of operation results,
- Estimated control value accuracy.

First, the maximal computed value defines the integer size m_i, which avoids overflow. In the DTC, this maximal value is obtained for V_{sd_r} in full wave operation and is expressed by:

$$\sum_{n=1}^{\frac{T}{2T_S}}\left[\left(T_s\sqrt{\frac{2}{3}}U_{ref}\right)V_{sd_r}\left((k-1)T_s\right)\right]=\sqrt{\frac{2}{3}}\frac{TU_0}{3} \tag{6}$$

where T is stator signal period. Bit number of integer part m_i is established as:

$$m_i \geq \log_2\left(\frac{TU_0}{2\sqrt{2}}\right) \tag{7}$$

The decimal part must minimize estimation error of the control parameters. In our approach, we assumed that the rectangular numerical integral method for V_{sd,q_r} introduces no digital torque estimation error. Furthermore, we minimized torque estimation error by selecting a low sampling time T_s to reduce the influence of calculation errors $\Delta\int R_s I_{sd,q}$. To ensure torque estimation accuracy, m_d , compared to n in the external ADC, should be:

$$m_d >> n \tag{8}$$

Consequently, the specific binary format is fixed by conditions (7) and (8). Thus, with the parameters in appendix, m_i value is equal to 3. Furthermore, since the ADC format used in most AC motor control applications is 10-bit or 12-bit, we chose m_d equal to 20-bit to get a fixed-point format standard with a multiple of 8 bit. The resulting specific binary format can be written as [s,3,20].

3.4. Digital properties

Fig. 9 presents torque estimation error $\Delta\Gamma$ between analog and digital torque by mixed simulation for ADC format size and sampling time T_s with the [s,3,20] binary format. ADC format size mostly influenced torque estimation error. Nevertheless, for the two ADC format sizes studied, estimation error increased slightly at low sampling time values (10µs): this is due to the low coefficient values used in the iterative sums for flux component calculations (Fig. 7). In fact, when sampling time becomes too short, the binary format [s,3,20] is no longer suitable for coding coefficients in flux component calculations. As a result, we chose a 12-bit external ADC and limited T_s to a minimal value about 10µs.

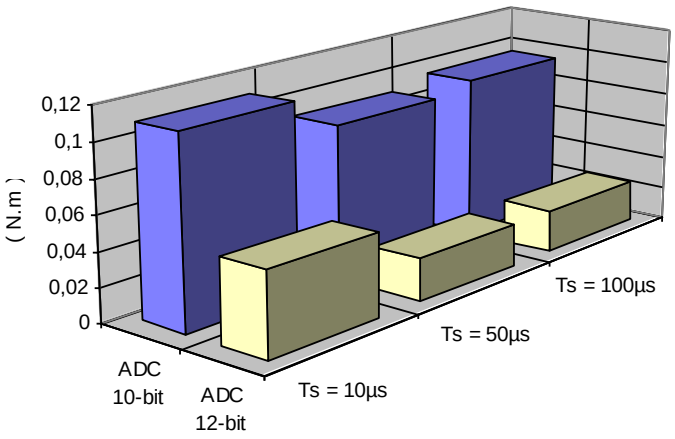


Fig. 9 – Torque estimation error versus ADC formats size and sampling time T_s.

4. VLSI ARCHITECTURE IMPLEMENTATION

4.1. DTC synthetisable model

In order to integrate the DTC digital algorithm, we divided the controller into five modules: FIRST IN FIRST OUT (FIFO) memory, PARALLEL COMPUTE UNIT (PCU), CORE COMPUTE UNIT (CCU), CORRECTOR UNIT (CU) and FINITE STATE MACHINE (FSM). The resulting architecture is presented in Fig. 10. FIFO reduced the number of ASIC input buses and ADC. Thus, only a *n* size external fast ADC could be used. The adr_mux signal gives a selection order to multiplexe the voltage and current analog values before Analog to Digital conversion. DIN_FIFO input bus is linked to ADC digital output.

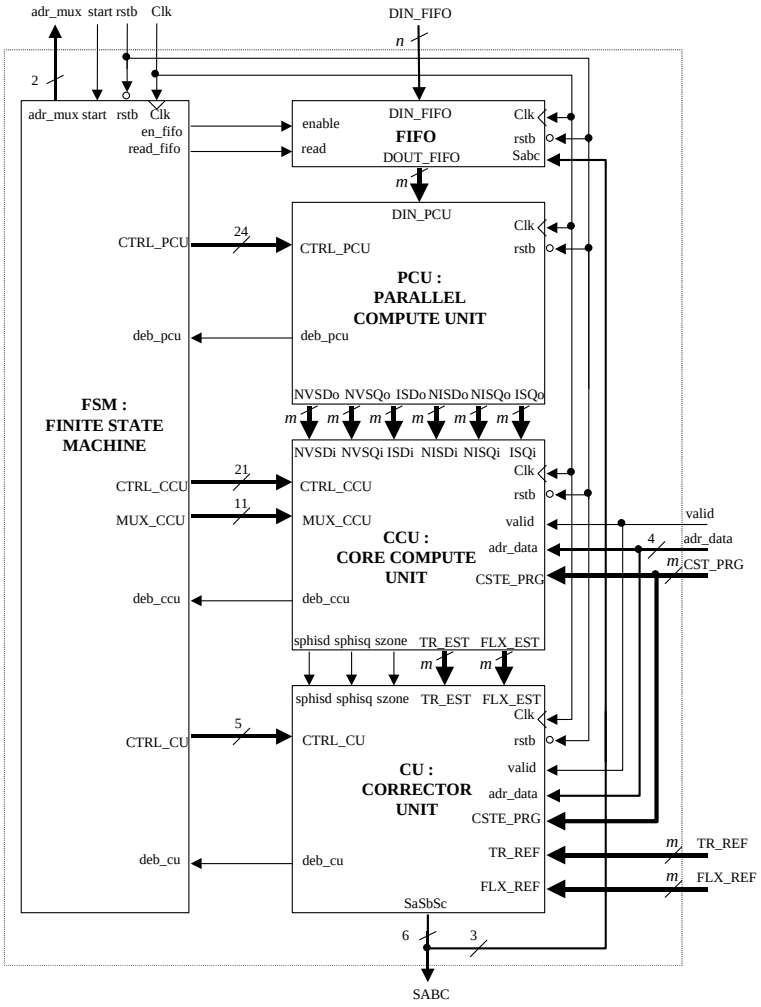


Fig. 10 – *Bloc diagram of DTC architecture.*

PCU calculated (d,q) voltage and current in parallel, and partially calculated voltage and current integrals (see Fig. 7). To calculate flux components, square flux modulus and torque, we used the common mathematical expression of the digitalized algorithm describes in Fig. 7:

$$S = (A \times B) \pm (C \times D) \tag{10}$$

where the operands are either computed values or constants. The CCU includes two multipliers and an addition/subtraction operator for hardware implementation of expression (10). This unit is an Intellectual Property-core designed in our laboratory. CU included flux and torque hysteresis comparators, a stator flux position detector and a boolean switching table. FSM managed parallel and sequential calculations.

Mixed simulations were used to study and validate the final RTL description [12]. Simulation results in Fig. 11 validated torque.

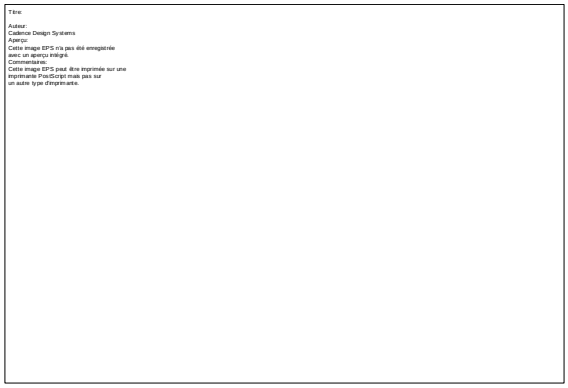


Fig. 11– *Estimated torque simulation result.*

4.2. ASIC placement and routing

The architecture discussed in the previous sections was implemented using the CMOS 0.8µm standard cell AMS library. We used Cadence Synergy to synthesize the RTL code to gate-level schematic [13]. Standard cell count for each unit is presented in Table 1. Total standard cell count, not including I/O pads, was about 20050.

Unit name	FIFO	PCU	CCU	CU	FSM
Standard cell count	401	3041	14383	1770	455
Total	20050				

Table 1: *Standard cell count for each unit.*

Fig. 12 shows ASIC layout made with Cadence Cell-Ensemble. Full ASIC size is 6.43mm * 7.1mm, equal to 45.65mm^2. The maximal frequency obtained by digital simulation for DTC chip is about 40MHz.

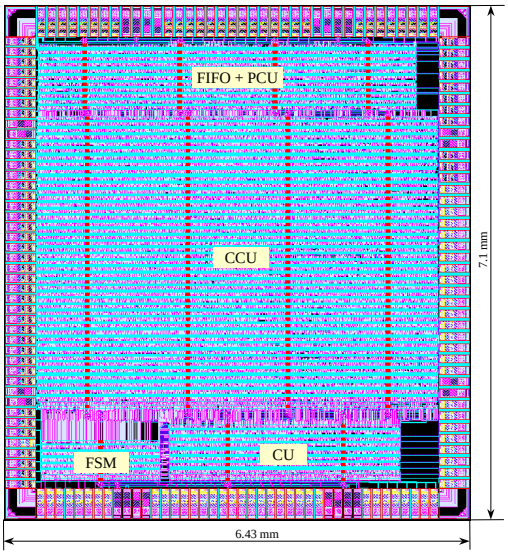


Fig. 12 – *ASIC layout.*

Design flow and VLSI of digital controller for AC motor were used to produce the layout presented Fig. 12. The chip has not been fabricated yet; it will be included in a near future in a mixed signal ASIC with ADC, analog interfaces and current measurement [14], developed at this time in our laboratory.

7. CONCLUSION

In this paper, we have presented a Top-down design methodology based on VHDL and SpectreHDL to design AC motor digital controllers. We have either presented an unique environment for modeling, simulation, functional validation and VLSI design of digital AC motor controller in its complete drive system, including power electronics and AC motor. The proposed methodology allows fast design development time and short time to market. More, models of various elements of AC drive systems can be further developed as reusable IPs, reducing future development time. The design of Direct Torque Control of an AC machine was used to illustrate and validate our methodology design flow.

VLSI of AC motor control is an alternative to conventional digital processors. Moreover, this hardware approach is a first step towards mixed SOC for AC motor control, including digital controllers, acquisition electronics, ADC and current measurement. Consequently, the proposed methodology seems to be better suited than software implementation or hardware/software design for full control system integration. Moreover, it allows us to resolve major design and mixed simulation difficulties when designing analog and power ASIC. Nonetheless,

an alternative to our methodology based on recent standardized VHDL_AMS (Analog Mixed Signal) language can also describe analog as well as digital elements. When using VHDL_AMS, SpectreHDL is no longer needed and a mixed simulator could be used throughout the design flow. However, our current laboratory Cadence tools cannot manage this VHDL analog superset.

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APPENDIX

Mixed simulation :	*AC motor parameters*
Torque reference is 10N.m Hysteresis band : +/- 0.25N.m Flux reference is 0.6Wb	3kW, 2-poles, 230/400V, 50Hz , U_0 = 300V R_s = 2,89Ω.