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Determining the minimal decoupling capacitor in a railway traction inverter using optimization

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Abstract- This paper aims determining the minimum decoupling capacitor C_{dec} for a railway traction inverter. It is defined when any increase of its value does not decrease the overvoltage at turn off anymore. A simple generic model is deduced from a full understanding of the switching cell behavior, including the effect of all stray inductances and all interactions within the switching cell. This model is used in an optimization process in order to obtain directly the minimal value of C_{dec} . The methodology is validated in comparison with time simulation, as well as using experimental results. It has been used to analyze the impact of the switching cell parameters on the minimum value of C_{dec} : switching speed, stray inductances and additional resistance have been considered.

I. INTRODUCTION

The railway industry is focusing on the advantages of using the SiC wide bandgap devices in traction applications. Within the European project “Shift2rail”[2], the potential benefits of using SiC MOSFETs in future converters are investigated, but also the potential impacts on module design. With the high speed commutation capability of these new switches, there is a strong need of properly designing a decoupling capacitor very close to the switching cell: therefore a small value is desired. In addition, this allows decreasing volume, weight and cost of the global system.

The goal of a decoupling capacitor is to reduce undesired events during the commutation, originated by stray inductance such as voltage overshoot. Additionally, at turn off, the output capacitance of the MOSFET oscillates with the stray inductance, generating high frequency ringing, inducing disadvantages such as Common Mode currents or radiated fields. The use of a decoupling capacitor C_{dec} allows thus compensating the impact of the stray inductive elements between the DC voltage source and the switching cell, and reduces the semiconductor peak voltage [3].

An empirical method to define the minimal decoupling capacitance is presented in [4]. An effective C_{dec} that achieves a fully decoupled condition without interfering the resonance between the power module stray inductance L_{pack} and the output capacitor C_{oss} is obtained using a rule defined as: C_{dec} must be 50 to 100 times larger than C_{oss} to achieve a good decoupled condition. However, this approach has no link with the minimal voltage overshoot and neglects the parasitic impedance of the decoupling capacitor.

If for a small power design, the value of decoupling capacitance is not really impacting its volume, this is not the case in high power traction inverters, where a specific bus bar has to be carefully designed to associate several capacitors in parallel, together with the power modules. We aim therefore minimizing this value, taking also into account the effective stray inductance of the association of all decoupling capacitors.

Fig. 1 presents a switching cell, where the input filter capacitor C_{filter} is replaced by an ideal voltage source due to its large value. The DC source (catenary) is not supposed to participate to the switching events, given the high value of the line inductance. L_{filter} in Fig. 1 represents the stray inductance between the filter capacitor and the switching cell, composed of a power module and the decoupling capacitor. It also takes into account the esl of the filter capacitor.

As clearly explained in [5], if C_{dec} is infinite, the overvoltage is generated by $L_{stray_pack} + esl$, L_{stray_pack} being the inductance of the semiconductor package and esl the stray inductance of C_{dec} . If C_{dec} is null then the overvoltage is generated by $L_{filter} + L_{stray_pack}$, and is usually higher, otherwise C_{dec} would not be necessary. Defining a value of C_{dec} that ensures that the voltage overshoot generated by this mix of stray inductances is limited to a maximum value is the objective of this paper. Other design criteria as the behavior under short circuit conditions can be used [6], but this paper is focused on the impact of switching speed and stray elements on the overvoltage as a function of the decoupling capacitor.

It should be noticed that in railway traction inverters, the value of the stray inductance between the DC bus capacitor tank and the decoupling capacitors (L_{filter}) might be quite low. The capacitor tank is indeed composed of a large number of paralleled components, thus leading to a low value of L_{filter} , since all Esl (Equivalent series Inductance) of electrolytic capacitances are paralleled. In addition, the link between this capacitor tank and the decoupling capacitors is very compact and as low inductive as possible. Therefore, interactions between filter and decoupling capacitors cannot be neglected.

The time domain waveform of the voltage on the semiconductor for different values of C_{dec} is illustrated in Fig. 2, based on simple simulations. The resonances between C_{oss} , C_{dec} and the parasitic inductances impact both semiconductor overshoot and the ringing during switching. A mix of low and high frequency ringing can be observed. In some case, the maximum voltage overshoot is even not reached at the first oscillation, but later (see the example of 500nF in Fig.2 where the maximum voltage does not occur at $\pi/2$).

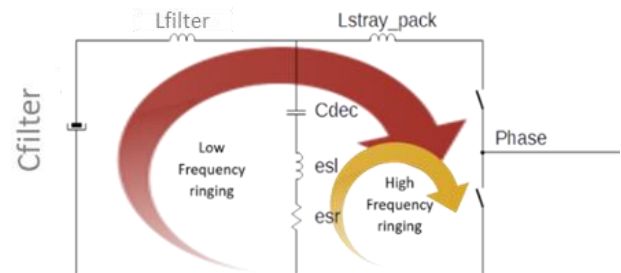


Fig. 1. Simplified switching cell and resonant circuits.

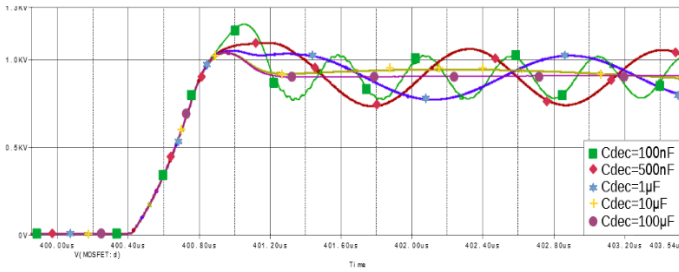


Fig. 2. Time domain simulation of the semiconductor voltage for different values of C_{dec} . Different behaviors and instant of maximum voltage.

The explanation of these phenomena comes from a simple current divider between the filter capacitors and the decoupling capacitor, including also the semiconductor's capacitance C_{oss} . The switching waveform excites an infinite number of frequencies, and furthermore resonances between all stray inductances, C_{dec} and the output capacitance C_{oss} of the semiconductors occur, as clearly illustrated in [7]. Therefore, the evaluation of the voltage overshoot cannot be obtained using the classical second order results.

Using the impedance comparison between the two branches (C_{dec} and C_{filter}) to determine a good decoupling condition is not obvious, since it has to be carried out for each individual frequency, each one contributing to the final result. It has thus been decided in this paper to use a time domain analysis, via a simplified representation to be considered in an optimization process. For this study, the representation of parasitic inductances is essential and must be studied carefully. The paper will start with introducing a rigorous electromagnetic model of a switching cell to account for all stray inductances of the layout. After simplifications, this equivalent circuit will be used into an optimization process to obtain the optimal value of the decoupling capacitance $C_{dec_optimal}$. It is defined as the minimal value necessary to obtain the minimal voltage overshoot i.e. when there is no longer interest in increasing C_{dec} . This value depends on several parameters as stray elements, switching speed or devices characteristics. Therefore, it is possible to have a direct link between $C_{dec_optimal}$ and all these parameters. The influence of these parameters on $C_{dec_optimal}$ will be discussed. All results will be validated using precise simulations and some measurements.

II. SWITCHING CELL ELECTROMAGNETIC MODEL

A. Defining the model

The electrical circuit representation of an industrial power inverter has to be carefully addressed. In traction inverters, the 3D integration is so complex that it is not possible to use distributed models of the interconnects, simply translating each part of the layout to R-L circuits as in [7]. Indeed the decoupling capacitors are plugged on a DC bus bar, also linked to the power modules.

A generic way to take into account all the parasitic inductances of a converter from its geometry is proposed in this section. Fig. 3 presents the "ONIX 671" converter, from Alstom, which will be used as a case study for optimization in section III. It is a three-phase inverter with a dissipative chopper leg.

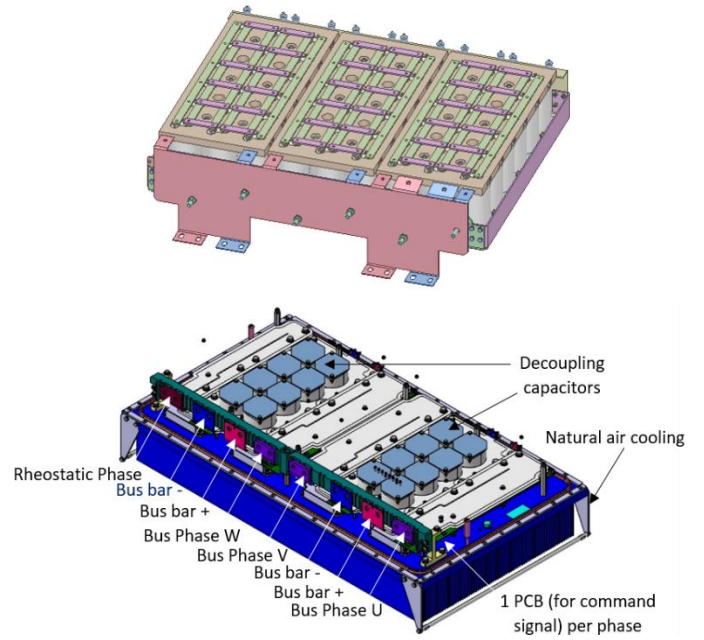


Fig. 3. Alstom converter ONIX 671. Top: 3x18 Electrolytic capacitor association (filter capacitor). Bottom: 4 power bus bars (2 used for 2 legs), 8 decoupling capacitors and 12 IGBT dual power modules 1.7kV / 1200A (3 per phase).

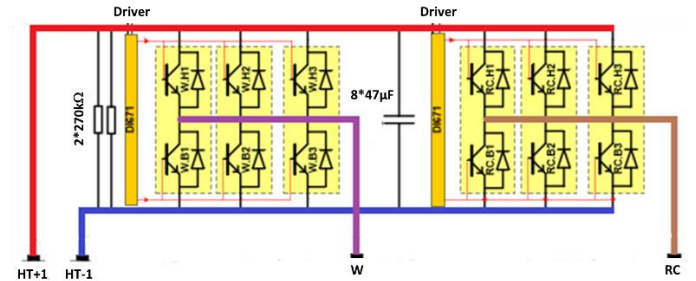


Fig. 4. Electrical schematics of phase W and rheostatic leg of power converter ONIX 671 from Alstom.

The maximum rms current per phase is 1020 A, and the rated DC bus voltage is 750-900 V. The maximum switching frequency is 1.5 kHz.

Each phase is composed of 3 dual pack IGBT 1.7 kV / 1200A power modules in parallel (Top IGBT + Bottom IGBT) [8]. The electrical schematics of phase W and the dissipative leg of ONIX 671 is displayed in Fig. 4. This structure will be considered to illustrate the generic representation in terms of electrical circuit, and will be validated by simulation and measurements. As already stated, the transposition of a complex industrial 3D geometry to an electric scheme is not straightforward. Indeed, the electrical connections are made using bus bars, which connect several components. It is not a simple inductance between the input and the output of a wire or a PCB track. In this context, the circuit representation requires a generic approach.

In order to reproduce the inductive effects due to the layout, a possible option is to use the PEEC method [9], which means usually replacing each conductor by a stray inductance and couplings with the rest of the structure. However, this solution

generates as many equivalent circuits as studied layouts, and does not allow a generic study of the phenomena involved in a commutation. Furthermore, the use of laminated bus bar structures does not facilitate identifying separate portions of the circuits which can be replaced by lumped elements, since the current flow in a plate is not really known. Therefore, we propose a global approach based on the number of Input/Outputs of a conductor. If a conductive link is only associating two points, it will be replaced by a single inductor (with coupling with the rest of the structure). However, if it is used to connect $N_{port} > 2$, the electrical circuit will be composed of $N_{port}-1$ inductors and resistors. One point among the I/O ports will be considered as a reference and linked with the others with R-L circuits (+couplings). It is worth noting that the full PEEC matrix in this representation exhibits both real and imaginary part. In other words, not only the inductors but also the resistors are coupled. Physically, this corresponds to common resistive path within the same conductor and eddy currents induced in the rest of the geometry. This generic representation has already been used and validated in several previous papers [10] [11].

Fig. 5 presents a simple example of this representation. First, we identify the system inputs / outputs that correspond to the interface points between the cabling model (bus bar) and other system components. Then, all points are connected electrically in groups. Among each group, a reference point is chosen arbitrarily. With this representation is possible to account for the impedances (and couplings) between any of the points connected together.

To illustrate the approach, let us consider the Alstom ONIX 671 power converter of Fig. 3. The DC bus is composed of 3×18 Electrolytic capacitors, and 2 power bus bars, each one linking the power modules to 8 decoupling capacitors (Fig. 6).

Even in this complex geometry, the proposed method can be used to obtain an equivalent circuit presented in Fig. 7. In this figure, “Mod1+” and “Mod1-” on the power bus bar have been chosen the reference points.

Many conductors are involved during the switching event: the positive and the negative bus bars and one bus bar for each phase that links the semiconductors.

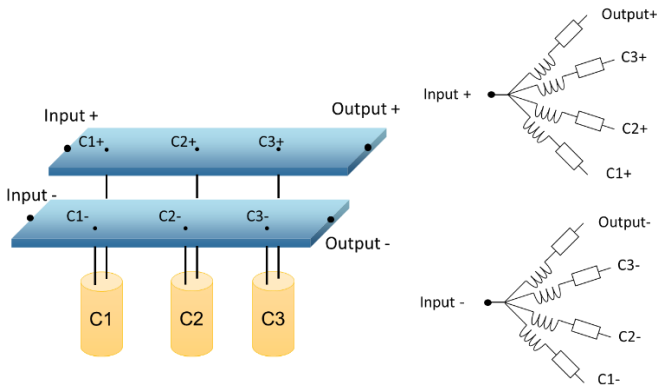


Fig. 5. Example of a circuit representation considering its input/output ports and reference port (real and imaginary couplings not displayed in this figure).

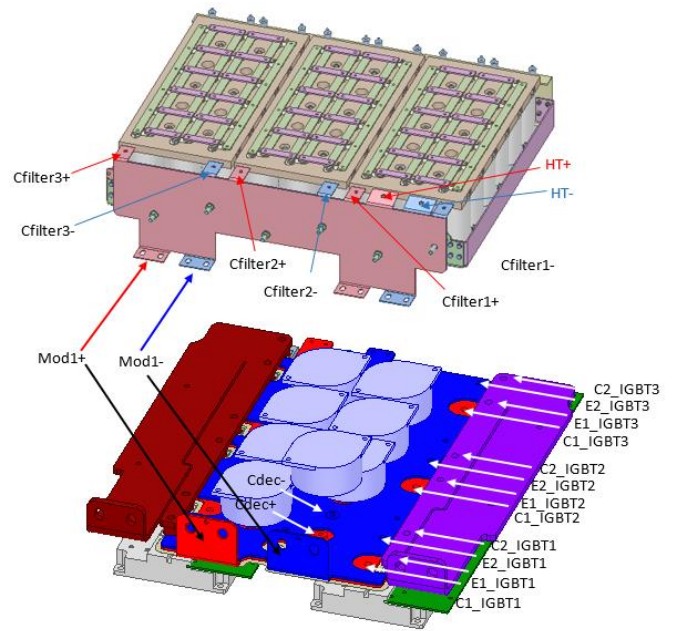


Fig. 6. Identification of the common points Mod1+ and Mod1- on the bus bars that connect the filter capacitors (top) and the bus bars that connect the decoupling capacitors and the semiconductors (bottom).

The positive conductor (Bus bar+) is connecting the positive pins of Cfilter, Cdec and the Collectors of the top IGBTs, and the negative conductor (bus bar-) is linking the negative pins of Cfilter, Cdec and the Emitters of the bottom IGBTs. Of course, we account for the intrinsic stray resistive and inductive behavior of the capacitors, the well-known esl (equivalent series inductance) and esr (equivalent series resistance) [12].

To simplify the representation of the 3×18 electrolytic capacitors, a global equivalent device has been considered, including the equivalent Esl of all capacitors, as well as all associated interconnects (Capacitor tank is displayed on the top of Fig. 6). For the 8 decoupling capacitors, the inductive link between the reference points mod+ and the plus of the capacitors pins, and mod- and the minus of the capacitors pins, is composed of three main parts: a main busbar (in blue and red in Fig. 6), mechanically supporting all 8 Cdec in parallel, and two phase busbars (dark red and magenta in Fig. 6) to close the loop.

After simulations, the impact of the main busbar, supporting the 8 Cdec was found very small in comparison with the two phase busbars, which have no overlap between plus and minus. Therefore, its impact has been neglect in comparison with the two lateral phase bus. This allowed simplifying the electrical representation, by replacing 8 Cdec with an equivalent circuit with $Esr/8$ and $Esl/8$. The contribution of the phase busbars is included in the model of Fig. 7, with the equivalent inductances connected to the reference points Mod1+ and Mod1-.

This circuit of Fig. 7 can be compacted by associating the stray impedances in series (and re-computing the couplings), what leads to the generic circuit of Fig. 8. In this circuit, Rfilter and Lfilter are the stray resistance and inductance of all paralleled Capacitors of the DC bus tank (Cfilter), in series with the parasitic behavior of the bus bar; Rdec and Ldec are the stray resistance and inductance of all paralleled Cdec, in series with the parasitic behavior of the bus bar; Rpack and Lpack are

the stray resistance and inductance of the device package [13], in series with the parasitic behavior of the bus bar.

Equations (1) to (6) provide the link between the elements of Fig. 7 and those of Fig. 8. The expressions of the couplings are given by (7)-(18). They are not displayed on these figures for clarity. To be noticed that couplings between capacitors and the rest of the structure have been neglected.

$$L_{filter} = esl + L1 + L2 + 2 \cdot M12 \quad (1)$$

$$R_{filter} = esr + R1 + R2 + 2 \cdot R12 \quad (2)$$

$$L_{dec} = esr2 + L3 + L4 + 2 \cdot M34 \quad (3)$$

$$R_{dec} = esr2 + R3 + R4 + 2 \cdot R34 \quad (4)$$

$$L_{pack} = Lm + L5 + L6 + 2 \cdot M56 + 2 \cdot M6m + 2 \cdot M5m \quad (5)$$

$$R_{pack} = Rm + R5 + R6 + 2 \cdot R56 + 2 \cdot R6m + 2 \cdot R5m \quad (6)$$

$$M_{filter_dec} = M13 + M14 + M23 + M24 \quad (7)$$

$$R_{filter_dec} = R13 + R14 + R23 + R24 \quad (8)$$

$$M_{filter_pack} = M15 + M16 + M1m + M25 + M26 + M2m \quad (9)$$

$$R_{filter_pack} = R15 + R16 + R1m + R25 + R26 + R2m \quad (10)$$

$$M_{dec_pack} = M35 + M36 + M3m + M45 + M46 + M4m \quad (11)$$

$$R_{dec_pack} = R35 + R36 + R3m + R45 + R46 + R4m \quad (12)$$

All resistances of the interconnects have been evaluated from Ansys Q3D at 1 MHz. This overestimates the resistive effects, which depend on skin effect. However, using complex equivalent circuits to represent frequency dependent resistance in a time domain simulation was not considered necessary.

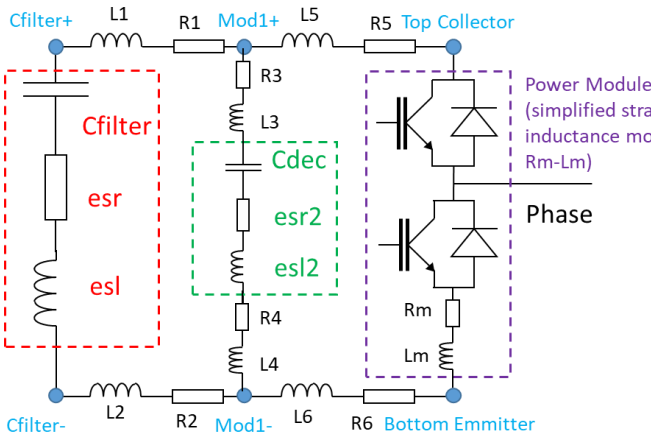


Fig. 7. ONIX 671 equivalent circuit (before simplification). Coupling not displayed for clarity

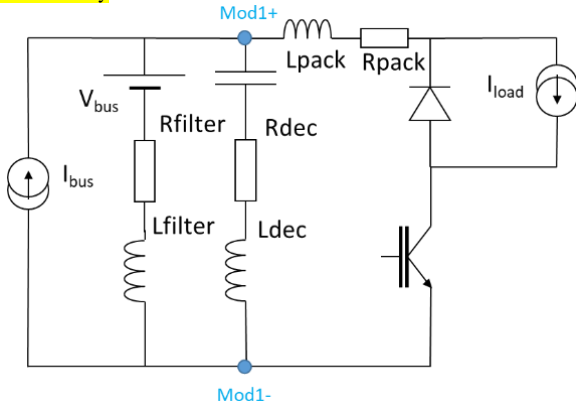


Fig. 8. Simplified equivalent electrical circuit of Fig.7 (coupling not displayed), used in a chopper cell to focus on switching events. I_{bus} represents the current delivered by the power source, and C_{filter} has been replaced by a DC voltage source V_{bus} . The load is modeled by a simple DC current source I_{load} .

B. Switching effect representation

To avoid time simulation with semiconductor models, which are sometimes originating convergence issues, a simple model reproducing the effects of switching has been used. This model replaces the power switches by a simple current source I_{ex} , with a parallel impedance (Norton model, Fig. 9). This impedance is defined by the output capacitance of the semiconductor, C_{oss} , to keep a physical link between the proposed model and the real switch. This approach has already been used for instance in [7], [14]. The current source is roughly a linear current slope with the same turn off speed (dI/dt) as the power switch. Therefore the number of parameters is reduced to the minimum: the switching speed (dI/dt) and C_{oss} . These two elements, together with stray inductances and decoupling capacitance are the main responsible of switching events, overshoot and ringing [15].

The circuit model corresponding to the power converter ONIX 671 is presented in Fig. 10. The DC operating point is represented with current and voltage sources: C_{filter} is large enough to keep a constant voltage during commutation, so it is replaced by a DC voltage source, V_{bus} (800V in the following). Of course, the corresponding stray elements are kept.

I_{ex} is a square waveform with an arbitrary duty cycle, swinging from 0 to desired current (1000A in the following). I_{bus} provides the average value of I_{ex} , so if duty cycle is 0.5, $I_{bus} = 500A$. Note that this choice of duty cycle and I_{bus} does not fix the switching conditions and is completely arbitrary.

As explained before, all values of the stray elements displayed in Fig. 10 have been obtained with a 3D simulation using Q3D. The mutual coefficients between all stray inductances and resistances have also been computed, but in the particular case of this geometry, they were so small that they have been neglected.

The esl and esr values of the filter and decoupling capacitors have been identified through impedance measurements: $esr = 1m\Omega$, $esl = 25nH$ for C_{dec} . The low esr /low loss is one of the reason for choosing this technology for railway, as well as robustness.

III. DEFINING THE OPTIMAL DECOUPLING CAPACITANCE

A. Optimization problem statement

We are looking for the minimal decoupling capacitance value since it will correspond to the minimal volume and therefore the best possible integration. This optimum decoupling capacitance is obtained above a specific value C_{dec_opt} which provides no more benefit on the voltage overshoot $\Delta V = V_{MOS\ peak} - V_{bus}$.

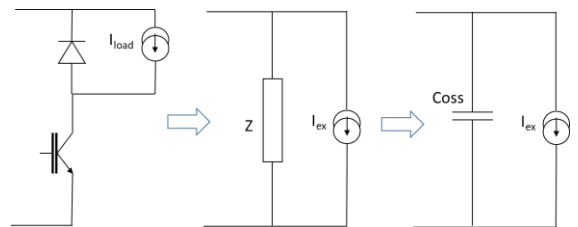


Fig. 9. Proposed model to simulate the MOSFET voltage overshoot.

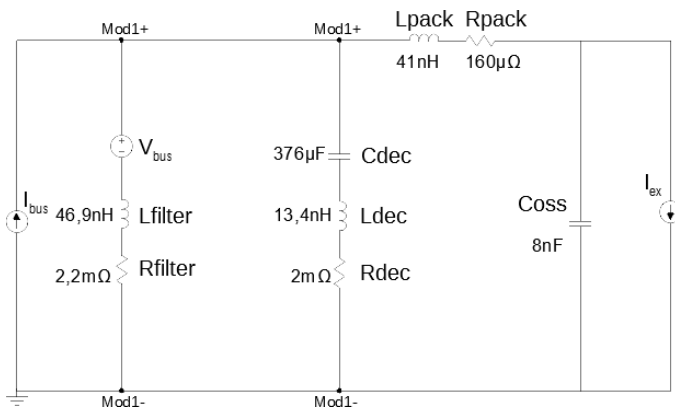


Fig. 10. Complete model circuit of power converter ONIX 671 for $C_{dec} = 8 \times 47\mu\text{F}$. The operating point is $V_{bus} = 800\text{V}$, I_{ex} is a square waveform with 0.5 duty cycle swinging from 0 to 1000A, and $I_{bus} = 500\text{A}$ to provide the average value of I_{ex} .

The minimum voltage overshoot ΔV_{min} is obtained for an “infinite” C_{dec} value, actually $C_{dec} = 10\text{mF}$. C_{dec_opt} is deduced when the overvoltage ΔV is 5% more than this minimum value, i.e. $\Delta V = 1.05 \times \Delta V_{min}$.

Using the proposed model to determine the minimal decoupling capacitor is easier than controlling time domain simulations, since the number of parameters is reduced (especially regarding the MOSFET and diode model), simulation time is much lower and no convergence issue can be expected.

B. Simple model for optimization

To validate the model of Fig. 10, experimental measurements have been carried out in a simple chopper configuration for the switching of one leg, using a double pulse test [15].

The setup is displayed in Fig. 11 and Fig. 12. It uses only one IGBT module and one phase. The objective is to measure the voltage overshoot on the top side IGBT for different values of decoupling capacitance and different switching speeds. The switched current was 1 kA and the voltage applied to the DC bus was 800 V. For voltage measurement, a 50 MHz bandwidth differential probe was used; the current measurement was performed with a Rowgoski probe.

The double pulse test was carried out for two switching speeds (2.5 kA/μs, 4.4 kA/μs) and the following decoupling capacitor values: 8x47μF; 4x47μF; 2x47μF; 1x47μF. The various dI/dt were obtained by modifying the gate resistor R_g of the driver.

The overvoltage as a function of the decoupling capacitance is displayed in Fig. 13. It is worth noting that when the amount of decoupling capacitors in parallel changes, the inductance and resistance of the switching loop also change. If C_{dec} increases (more capacitors in parallel) then L_{dec} decreases, and therefore the voltage overshoot $L_{dec} \cdot dI/dt$ also decreases. This phenomenon will be considered in the equivalent circuit, by changing the value of R_{dec} and L_{dec} according to C_{dec} change (Table I).

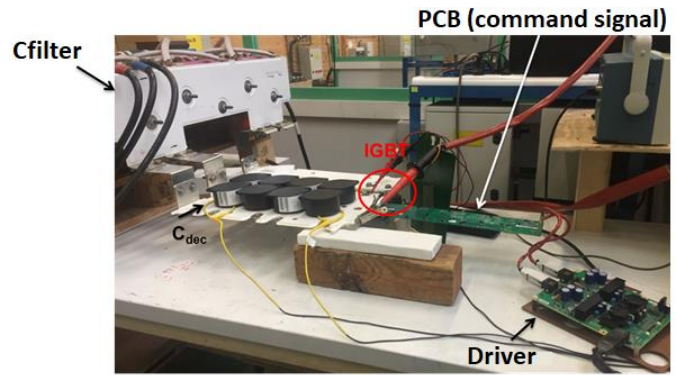


Fig. 11. Experimental bench using ONIX 671 power converter.

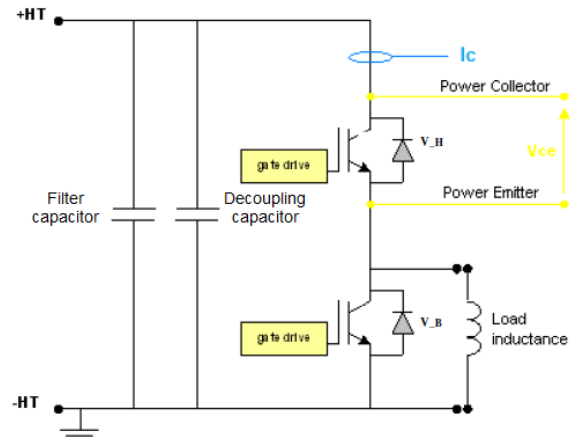


Fig. 12. Simplified equivalent circuit of the test bench from Fig. 11.

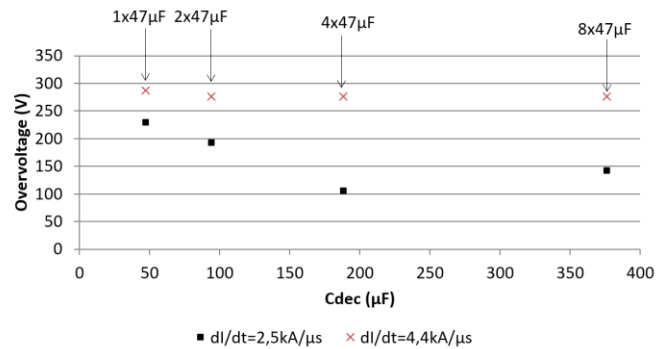


Fig. 13. IGBT overvoltage from Alstom test bench, in function of the decoupling capacitor value for two switching speeds (4.4kA/μs and 2.5kA/μs).

In experiment, it was only possible to use multiple values of 47μF (due to capacitor availability and bus bar structure), so a simulation approach was also considered to get results with other capacitor values. The circuit of Fig. 10 has therefore been used on Ansys Simplorer and results compared with the measurements, to validate this precise model. A dedicated IGBT model, mainly based on the MOSFET behavior, was used and its parameters extracted from datasheet (Mitsubishi CM1200DC-34S [8]). The switching speed in simulation was controlled by varying the value of the gate resistance R_g , as in experiments. C_{dec} , R_{dec} and L_{dec} have been changed according to the number of paralleled Capacitors, as indicated in Table I. The results are presented in Fig. 14. Despite some differences in the absolute values, the evolution of the curves is

very similar. Even if the voltage measurement was carried out with care, using a very low inductance path for the voltage probe, the voltage measurement may have been disturbed by external field, what might explains the difference between the experiment and the simulation.

TABLE I. SUMMARY OF DIFFERENT TESTS CONDITIONS

Test Condition	Cdec [μ F]	Ldec [nH]	Rdec m Ω
1 x 47 μ F	47	35.3	2.9
2 x 47 μ F	94	22.8	2.4
4 x 47 μ F	188	16.5	2.1
8 x 47 μ F	373	13.4	2.0

An interesting property is to be noticed, especially for $dI/dt = 2.5 \text{ kA}/\mu\text{s}$: the voltage overshoot is minimal for $C_{dec} = 4 \times 47\mu\text{F}$, and increases for $8 \times 47\mu\text{F}$. This results from the interaction of resonances between all elements of the circuit (C_{oss} , C_{dec} and stray inductances), which originate a minimal voltage spike for this specific value of C_{dec} . Unfortunately this property cannot be used to obtain an optimal value for C_{dec} , due to too high sensitivity to all stray elements.

Once validated in comparison with experiment, this circuit has been used to extend the capacitance variation C_{dec} . For each time domain simulation, the values of C_{dec} , L_{dec} , R_{dec} change according to (13)-(15):

$$C_{dec} = N \times 47\mu\text{F} \quad (13)$$

$$L_{dec} = 10.275 \text{ nH} + 25\text{nH}/N \quad (14)$$

$$R_{dec} = 1.875\text{m}\Omega + 1\text{m}\Omega/N \quad (15)$$

the constant terms in (14) and (15) being the contribution of the busbars.

The simplified model of Fig.10 (for $8 \times 47\mu\text{F}$) has then been compared with the precise simulation of Simplorer. Fig. 16 shows the overvoltage on the IGBT terminals as a function of the decoupling capacitance (from $10\mu\text{F}$ up to 10mF i.e. “infinity value”), for a dI/dt of $4,4 \text{ A}/\mu\text{s}$. Even if there is a difference, the general trend is the same, what is important for optimization purpose. The simple model is thus able to reproduce the impact of a change in C_{dec} . The differences can be explained since the current source in the model uses a linear behavior, which is not the case in reality and in Simplorer simulations. In addition, changing the value of C_{dec} , L_{dec} and R_{dec} elements of the switching loop has an impact on the switching speed (variation of $\pm 200 \text{ A}/\mu\text{s}$ noticed during experiments).

Since the simplified model gives the correct trend, it has been implemented in an optimization process to obtain the optimal value of the decoupling capacitance. This is described in section C.

C. Optimization process

The optimal value of C_{dec} is obtained using the function ‘fzero’ from Matlab®. It solves the circuit presented in Fig. 10 in Simulink®, calculating the semiconductor voltage in the time domain using trapezoidal resolution method. Values of C_{dec} , R_{dec} , L_{dec} are changed according to (13)-(15). The current

commutation speed is defined in Iex source. The Matlab function returns the optimal value of C_{dec} that minimizes the objective function defined as (16):

$$F_{obj} = (V_{MOS\ peak} - V_{bus}) - 1.05 \cdot (V_{MOS\ peak\ min} - V_{bus}) \quad (16)$$

$V_{MOS\ peak}$ is the semiconductor peak voltage obtained with C_{dec} , whereas $V_{MOS\ peak\ min}$ is the one obtained with an “infinite” C_{dec} (actually 10 mF).

Fig. 16 shows the evolution of the voltage overshoot ΔV_{mos} as a function of C_{dec} , for 3 different commutation speed. C_{dec_opt} is indicated with a star on the curves. The voltage overshoot obtained at C_{dec_opt} is 5% more than the minimal possible value, according to our optimization strategy. To be noticed that the minimum overvoltage obviously increases with dI/dt .

By comparing the three test cases from $2.5\text{kA}/\mu\text{s}$ to $5.2\text{A}/\mu\text{s}$, (Fig. 16) it can be seen that the optimal decoupling capacitance for a faster system ($373 \mu\text{F}$) is lower than for a slower system ($410 \mu\text{F}$) using our condition regarding the relative overvoltage definition.

This is quite intuitive since higher dI/dt implies higher equivalent frequency, and therefore a lower value of capacitance is needed for reaching the same impedance. However, this is much higher than the empirical method, which suggests using 50-100 times C_{oss} (i.e. 400 nF - 800 nF in the considered application) [4][7]. It shows that changing the criterion of C_{dec} selection has a huge impact on its value.

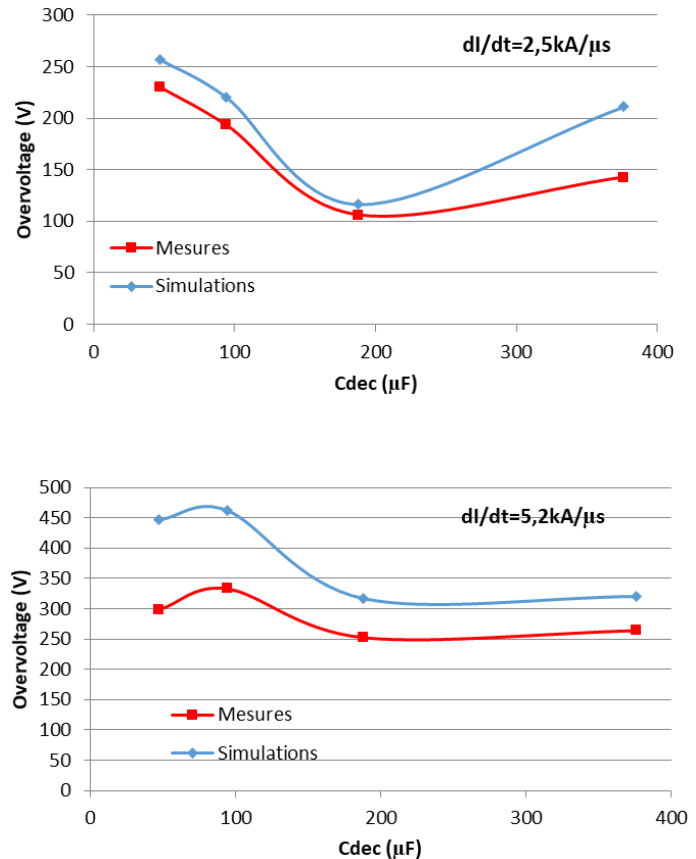


Fig. 14. Simulation results of the model in Simplorer simulation (♦) and test bench measurements (■) for two switching speeds.

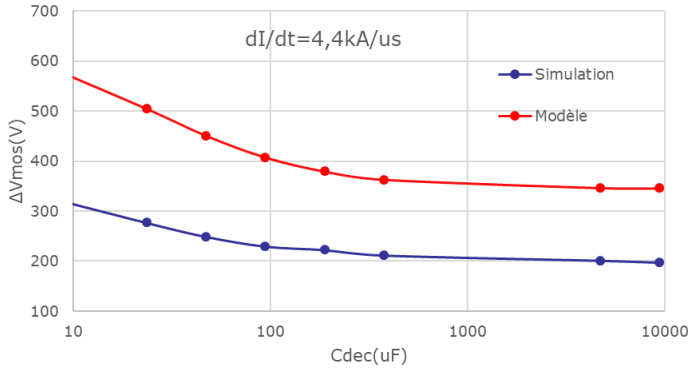


Fig. 15. Overvoltage on the IGBTs in function of decoupling capacitance (Simplorer and simple models comparison).

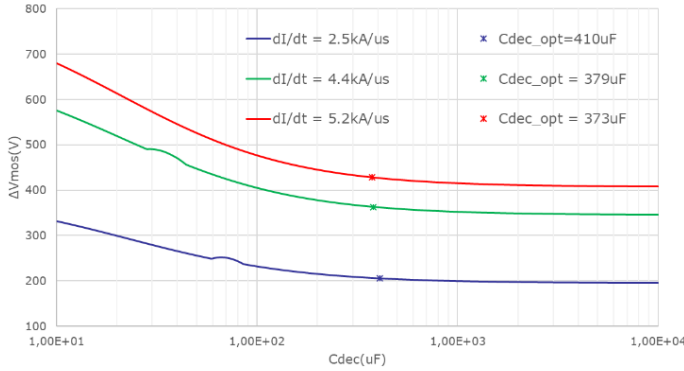


Fig. 16. Voltage overshoot vs Cdec and Cdec_opt.

This optimal result is actually really close from the original value of Cdec ($8 \times 47 \mu\text{F} = 376 \mu\text{F}$) in the ONIX 671 converter, but it is also linked to the choice of technology (Esl and Esr of the capacitor chosen as a reference, busbar, semiconductor package).

To check the impact of the objective function, it has been changed from 5% to 10% of the overshoot obtained for an infinite Cdec. The optimal value Cdec_opt changes from $410 \mu\text{F}$ to $181 \mu\text{F}$ for $dI/dt = 4.4 \text{ kA}/\mu\text{s}$ and from $380 \mu\text{F}$ to $197 \mu\text{F}$ for $dI/dt = 2.5 \text{ kA}/\mu\text{s}$. This is quite interesting for the designer: accepting a voltage overshoot a bit larger may help in reducing the value of decoupling capacitor, and therefore facilitate its integration.

Since all stray elements and switching speed impact the optimal decoupling capacitance, a sensibility study has been carried out in the next section.

IV. SENSIBILITY STUDY

The first parameter to be changed was the switching speed. In the previous section, it was already noticed that a change of a factor 2 in the switching speed was only originating a variation of 10% in the optimal value of decoupling capacitance ($410 \mu\text{F}$ to $373 \mu\text{F}$). However, higher change has been investigated, corresponding to a change from Silicon IGBT to Silicon Carbide MOSFET. The results (without changing the other elements of the circuit) is a huge decrease of the optimal decoupling capacitor, as displayed in Table II.

TABLE II. IMPACT OF CURRENT COMMUTATION SPEED

dI/dt [A/μs]	Cdec_opt [μF]
5.2	373
33	2.6
52	1.6

Unfortunately, even if the gain in term of Cdec_opt is impressive, one has to take care to the overvoltage which will occur on the device: without changing the package ($L_{\text{pack}} = 41 \text{ nH}$) the situation of dI/dt as high as 33 or 52 $\text{kA}/\mu\text{s}$ is not possible, leading to voltage overshoots of some kilovolts. Of course the full interconnect topology has to be redesigned when changing from IGBTs to SiC MOSFET. The proposed optimization method will be useful to determine the optimal decoupling capacitance corresponding to the new low inductive layout, as it will be illustrated in the conclusion.

To help in understanding the effect of other parameters, few additional sensibility studies have been carried out.

Lpack obviously directly influences the overvoltage. However, during the sensibility study, it was noticed that increasing Lpack allows reducing the value of Cdec_opt. This was not intuitive at all, but it is useless since the aim is not to increase the voltage overshoot.

The influence of Ldec (which originates from both Esl and bus bar stray inductive behavior) has also been studied. Once again, increasing Ldec results in higher voltage overshoot. Overall, Ldec and Lpack have the same role as they are both part of the switching loop. From a design point of view, there is no interest in increasing the value of Lpack and/or Ldec to reduce Cdec as this would increase the overvoltage.

Another remark is that for low values of the parasitic inductance of the capacitor tank, Lfilter, the electrolytic capacitors participate in decoupling and the voltage overshoot is reduced. Obviously, it is not possible to reduce Lfilter too much, otherwise Cdec would not be necessary at all.

As noticed in previous section, increasing the switching speed (dI/dt) decreases the need for a high Cdec value, and at the same time increases the voltage overshoot. The overall impact of dI/dt on Cdec is actually limited by the values of the parasitic inductances.

By applying the same approach for different parasitic resistance values of the decoupling capacitor, Rdec, it has been observed that the Cdec_opt changes considerably (Fig. 17). This is explained by an increased damping of the MOSFET voltage. Due to the large number of circuit equations, it was not easy to predict this with classic second-order models. For Rdec between $2 \text{ m}\Omega$ and $10 \text{ m}\Omega$, the optimal decoupling capacitor remains around $250 \mu\text{F}$, but if $R_{\text{dec}} = 50 \text{ m}\Omega$, the optimal decoupling capacitor is divided by two, and even by 10 for $R_{\text{dec}} = 100 \text{ m}\Omega$. In order to verify the impact of a resistor in series with the decoupling capacitor, the ONIX 671 structure has been simulated using Simplorer, with $dI/dt = 5.2 \text{ A}/\mu\text{s}$ and an additional resistance of $100 \text{ m}\Omega$ (Fig. 18). The value of Cdec_opt is displayed on this figure. The losses in the

additional resistance have been evaluated around 130W in a real situation of PWM inverter, which for this power range may be acceptable, if it can be evacuated. However the gain on the integration has to be carefully evaluated, since this solution is clearly not easy to implement.

All previous results are summarized in Table III, which illustrates the impact of all stray elements on both overvoltage and optimal value of decoupling capacitor.

TABLE III. SUMMARY OF SENSIBILITY STUDY

Parameter	Cdec_Opt	Overvoltage
Lpack	+	++
Ldec	+	++
Lfilter	+	+
dI/dt	++*	++
Rdec	++	+**

* limited by maximum allowed overvoltage and stray inductances
 ** for reasonable values of Rdec

V. CONCLUSION

The aim of this paper was to propose a methodology to size the minimal decoupling capacitor for high power traction inverters used in railway. The proposed condition was the voltage overshoot in the time domain, which results from complex interactions between Coss, Cdec and all stray inductances brought by the 3D layout and components. The chosen condition was to define the "optimal" decoupling capacitance when the voltage overshoot is 5% more than using an infinite Cdec.

First, a generic method to account for the stray inductance of the geometry has been introduced. This is more than roughly evaluating the contribution of a stray inductive behavior with some order of magnitude, but really provides a close link with the layout and the number of devices in parallel used to realize the decoupling function.

To be implemented in an optimization process, the time domain simulation using precise semiconductor models is not very convenient, due to potential convergence issues and amount of time. Therefore, a simple equivalent model using a linear slope for dI/dt associated with the device's capacitance has been used. This model has been validated in comparison with precise simulations, these ones being validated themselves with measurements. This simple model used in optimization has allowed obtaining the minimal value of decoupling capacitance according to the chosen criterion, in the example of the traction inverter ONIX 671. The value is much higher than the one obtained in previous work using different criterion and lower power.

Sensibility study has been carried out to evaluate the most impacting factors on Cdec_opt, and it has been shown that the commutation speed may help in decreasing this value, but also that this should be combined with a clear reduction of the stray elements, to avoid large voltage overshoots. Indeed, the

proposed criterion checks the relative voltage overshoot, but the absolute voltage has also to be limited. Therefore, the proposed design method should be integrated in a full design process, as illustrated in Fig. 19.

Finally, the possibility of further reduction of Cdec_opt using an additional series resistance has been proposed, but should be considered with care, regarding the amount of losses generated and heat dissipation issues for high power structures.

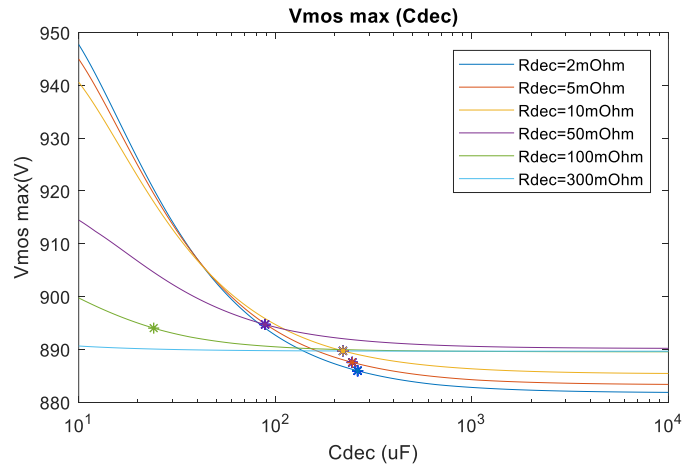


Fig. 17. MOSFET peak voltage as a function of the decoupling capacitor (Cdec) for different parasitic resistance values of Rdec (bus bar and esr of the decoupling capacitors).

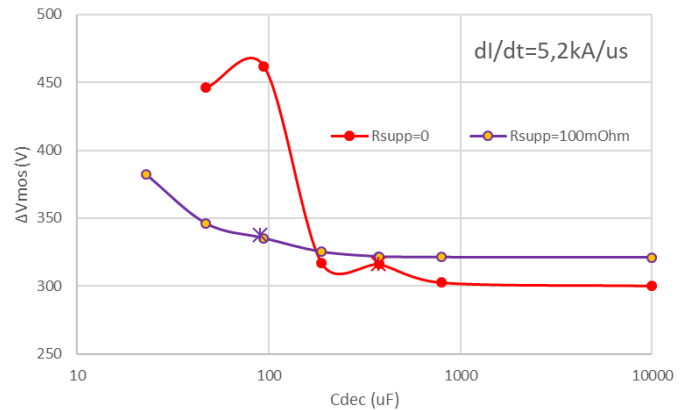


Fig. 18. Overvoltage on the IGBT vs decoupling capacitance with and without a 100 mΩ series resistance Rsupp (Simplorer simulations).

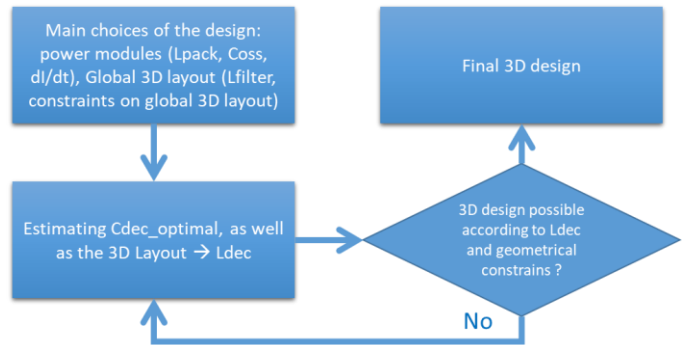


Fig. 19. Illustration of the proposed optimal sizing method inside a full 3D layout design process.

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