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Alexandre Bucamp, Christophe Coinon, Sylvie Lepilliet, David Troadec, Gilles Patriarche, et al.. In-plane InGaAs/Ga(As)Sb nanowire based tunnel junctions grown by selective area molecular beam epitaxy. *Nanotechnology*, 2022, 33 (14), pp.145201. 10.1088/1361-6528/ac45c5 . hal-03547003

**HAL Id: hal-03547003**

**<https://hal.science/hal-03547003>**

Submitted on 28 Jan 2022

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# In-plane InGaAs/Ga(As)Sb nanowire based tunnel junctions grown by selective area molecular beam epitaxy

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Received xxxxxx

Accepted for publication xxxxxx

Published xxxxxx

## Abstract

In-plane InGaAs/Ga(As)Sb heterojunction tunnel diodes are fabricated by selective area molecular beam epitaxy with two different architectures: either radial InGaAs core / Ga(As)Sb shell nanowires or axial InGaAs/GaSb heterojunctions. In the former case, we unveil the impact of strain relaxation and alloy composition fluctuations at the nanoscale on the tunneling properties of the diodes, whereas in the latter case we demonstrate that template assisted molecular beam epitaxy can be used to achieve a very precise control of tunnel diodes dimensions at the nanoscale with a scalable process. In both cases, negative differential resistances with large peak current densities are achieved.

Keywords: selective area growth, molecular beam epitaxy, in-plane nanowire, Esaki tunnel diodes

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## Introduction

Nanoscale tunnel heterojunctions have been exhaustively investigated for the fabrication of electron devices aiming either at reducing the power consumption of digital circuits [1] or at targeting submillimeter wave sources and detectors [2]. In both cases, highly staggered heterostructures associating As and Sb based III-V semiconductors are particularly exploited because the narrow interband tunneling barrier they provide is essential to combine a high tunneling current with a steep curvature in their I-V characteristics [3]. The reduced cross-section of the tunneling interface required to manage a good electrostatic control of the tunneling current or to reduce the junction capacitance can be achieved with an aggressive top

down etching of a two dimensional epitaxial layer. Even though very small dimensions can be achieved, trap assisted tunneling related to surface states on etched mesa side walls cannot be avoided with this strategy [4]. Bottom-up approach based on gold assisted Vapor Liquid Solid (VLS) grown vertical nanowires is a good alternative to avoid etching [5] but the achievement of abrupt interfaces with a good control of ternary alloy composition is quite tricky due to the accumulation of III-elements in the catalyst. Selective area (SA) epitaxy based on the fabrication of a dielectric template prior to the growth allows a very good control of the dimensions of the tunneling interface as well as a direct passivation of heterojunction sidewalls as demonstrated for InAs/GaSb broken gap tunnel diodes with metalorganic chemical vapor deposition (MOCVD) [6] or Molecular Beam

Epitaxy (MBE) [7] and more recently for MOCVD grown InGaAs/GaAsSb Tunnel Field Effect Transistors (TFET) [8].

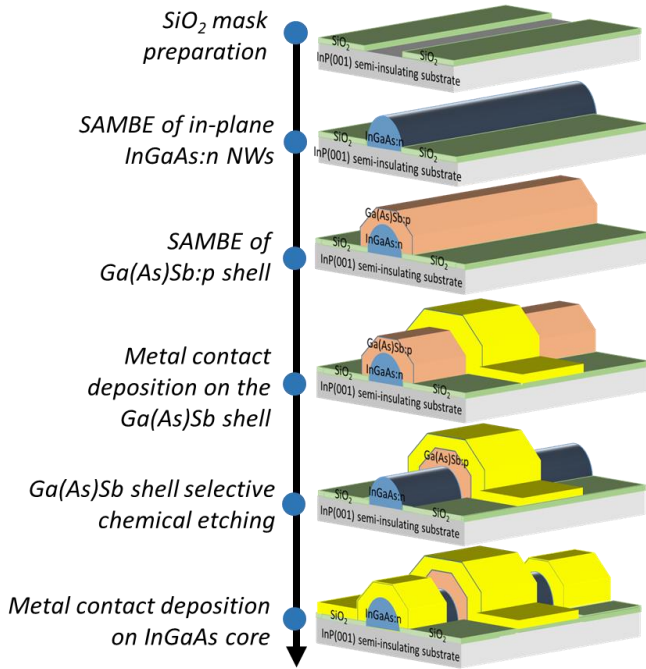


Figure 1 - Process flow for in-plane core-shell tunnel diode fabrication

In this paper, we investigate the properties of InGaAs/Ga(As)Sb tunnel diodes fabricated by in-plane SAMBE into the nanoscale openings of a dielectric mask. Different approaches are considered: from core-shell to in-line configurations with either nearly lattice matched or highly lattice mismatched systems. The impact of interface dislocations as well as alloy composition close to the tunneling interface on the I-V characteristics of the tunnel diodes is discussed.

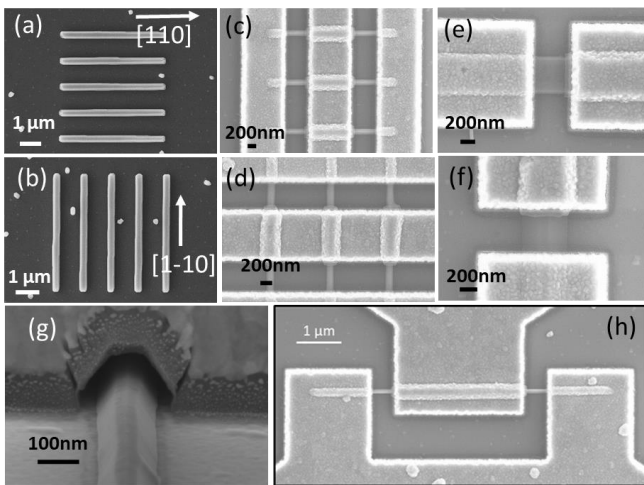


Figure 2 – SEM images of InGaAs/GaSb heterostructures (sample A) after growth inside an array of 100nm wide SiO<sub>2</sub> mask openings oriented in the [110] (a) or the [1-10] (b) directions. SEM images of the same arrays after device fabrication (c and d) and of devices fabricated from 1μm wide openings (e and f). Bird view SEM image showing the etching of the GaSb shell under the Ti/Au contact (g). SEM image of a single NW device showing the access configuration of the devices under test (h).

## 1. Device fabrication

### 1.1 Core-shell tunnel diode fabrication

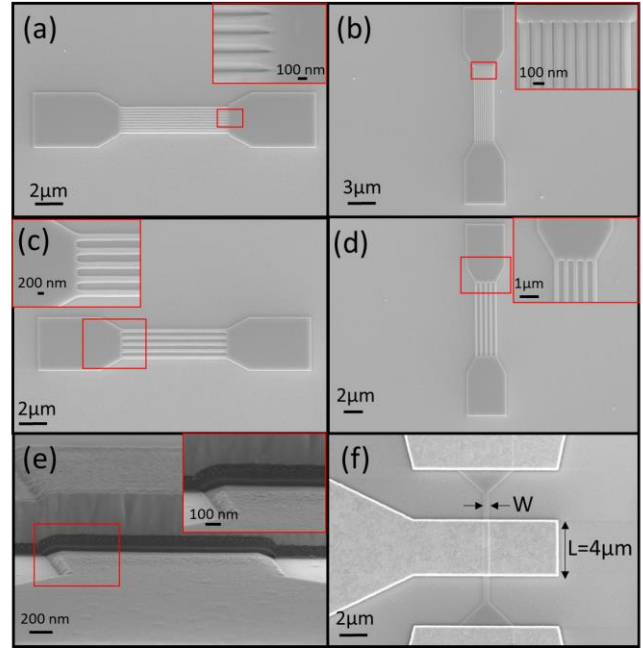


Figure 3 – SEM images of InGaAs/GaAsSb heterostructures (sample B) after growth inside an array of 100nm wide SiO<sub>2</sub> mask openings oriented in the [110] (a) or the [1-10] (b) directions and inside an array of 200nm wide SiO<sub>2</sub> mask openings oriented in the [110] (c) or the [1-10] (d) directions. Insets are zooms on the connection with the contact mesa (red rectangles). Bird view SEM image of a 2μm wide device highlighting the etching of GaAsSb under the Ti/Au contact (e). Plan view SEM image of a single NW device showing the configuration of the access and the dimensions of the devices under test (f).

In-plane core-shell tunnel junctions are fabricated from InP (001) semi-insulating substrates covered by a SiO<sub>2</sub> mask patterned with nanoscale openings with a width from 50nm to 1 μm according to the process described in ref. [9]. Atomic hydrogen assisted MBE is then used for InP surface deoxidization under As<sub>4</sub> flux and then for selective growth of InGaAs lattice matched to InP inside the mask openings using a growth rate of 0.2 ML.s<sup>-1</sup>, a temperature of 480°C and a V/III flux ratio of 2.5 [10]. InGaAs is n-type doped with Silicon to about 10<sup>19</sup> cm<sup>-3</sup> for a nominal deposited thickness of 50 nm. p-type doped Ga(As)Sb is subsequently grown under atomic hydrogen flux using the same substrate temperature but with

a growth rate of  $0.1 \text{ ML}\cdot\text{s}^{-1}$  to ensure a good selectivity for the growth. For sample A, 100 nm GaSb, p-type doped with silicon, are grown with a Sb/Ga flux ratio of 3.5 whereas 50 nm GaAsSb, p-type doped with beryllium, are used for sample B. As and Sb flux of  $0.25$  and  $0.1 \text{ ML}\cdot\text{s}^{-1}$  respectively are used for the growth of this alloy after optimization of the composition using X-ray diffraction on two dimensional layers. Both for GaSb and GaAsSb, a p-type doping of about  $2 \times 10^{19} \text{ cm}^{-3}$  is targeted. Standard e-beam lithography, Ti/Au evaporation and ammonia-based chemical etching of the shell material complete the fabrication process, as described in figure 1. Single as well as arrays of parallel NWs have been designed. In the case of lattice mismatched heterostructure (sample A), arrays of NWs are connected with the contact metal pads whereas, for the InGaAs/GaAsSb heterostructure, close lattice matching enables the design of larger area mesa connecting parallel NWs in order to reduce the access resistance. Plan-view Scanning Electron Microscope (SEM) images of InGaAs/GaSb and InGaAs/GaAsSb devices for different crystallographic orientations, different mask opening widths and at different steps of the process are depicted in figure 2 and figure 3 respectively.

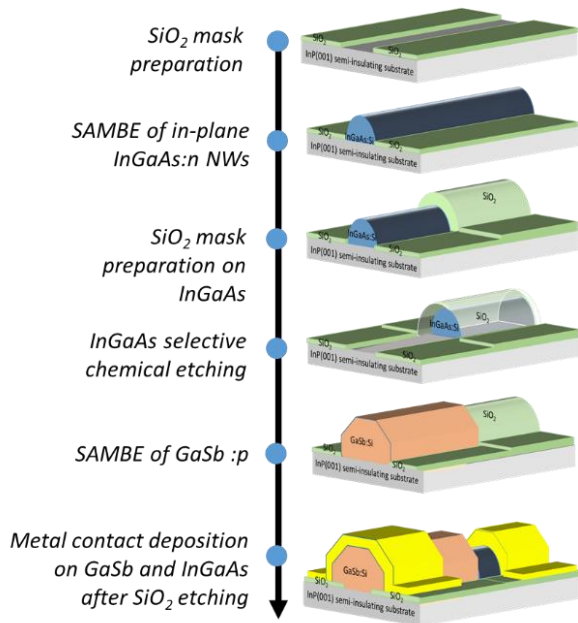


Figure 4 – Process flow for in-plane in-line tunnel diode fabrication.

### 1.2 In-line tunnel diode fabrication

InGaAs/GaSb in-line tunnel diodes (sample C) are fabricated using the two-step SAMBE process described in figure 4. 30nm thick InGaAs:Si in-plane nanostructures are first grown using the same conditions than for samples A and B (figure 5a). These structures are then partially masked with  $\text{SiO}_2$  using the same process as for the previous mask (figure 5b). InGaAs is then chemically etched down to the InP substrate using orthophosphoric acid based etchant (figure 5c

and 5d). This chemical etching results in an under-etching of InGaAs of about 40nm. After being outgazed under ultra-high vacuum, the sample is re-introduced in the MBE chamber for III-V oxide removal in the mask openings using atomic hydrogen exposure combined to thermal annealing under  $\text{As}_4$  flux at  $480^\circ\text{C}$ . 100 nm Si-doped GaSb ( $p=2 \times 10^{19} \text{ cm}^{-3}$ ) are then deposited by SAMBE using the same growth conditions than for sample A and B (figures 5e and 5f). After growth,  $\text{SiO}_2$  mask is opened on InGaAs and Ti/Au contacts are deposited on each part of the NWs by means of e-beam lithography and metal evaporation (figures 5g et 5h).

## 2. Material characterization

Structure and composition analysis of the samples are performed at the end of the process by extracting thin cross-section lamellas from the active part of the devices using Focus Ion Beam (FIB) etching. Scanning Transmission Electron Microscopy (STEM) is carried out on a Titan Themis 200 (FEI) instrument equipped with a spherical aberration corrector on the probe and the energy-dispersive X-ray spectrometry (EDX) analysis system super X ( $0.7 \text{ sr}$  solid angle of collection). The accelerative voltage was 200 kV.

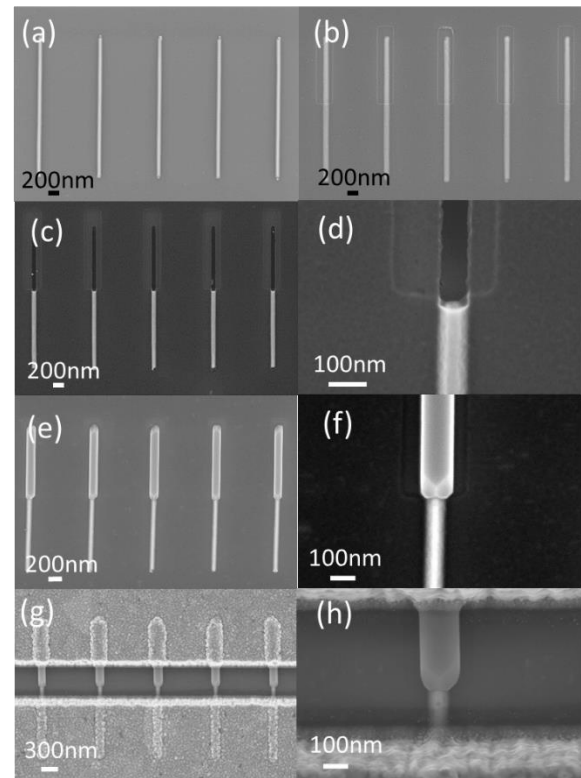


Figure 5 – Plan view SEM images after different steps of the fabrication of sample C: after the growth of InGaAs inside an array of 50nm wide  $\text{SiO}_2$  mask openings (a), after masking a part of these NWs with  $\text{SiO}_2$  (b), after chemical etching of the unmasked part of the NWs (c and d), after regrowth of GaSb (e and f) and after metal contact deposition (g and h).



## 2.1 InGaAs/GaSb core-shell nanostructures (sample A)

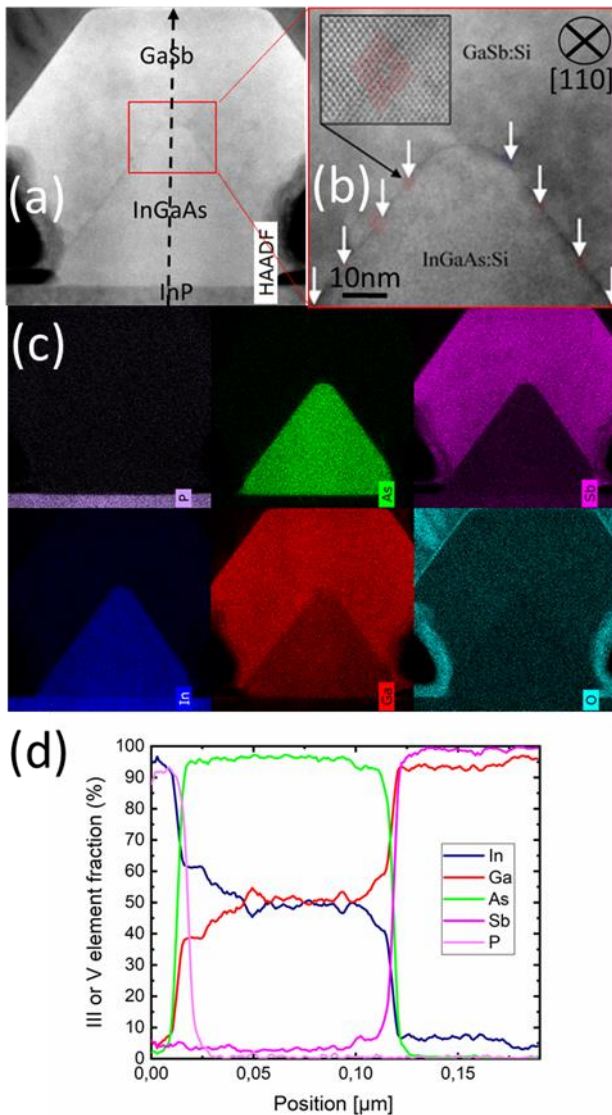


Figure 6 – TEM analysis of an InGaAs/GaSb NW (sample A) grown inside a 100nm wide opening along [110] direction: HAADF image (a), zoom on the InGaAs/GaSb interface (b) with interface dislocations marked by a white down arrow and highlighted in the inset image, EDX analysis (c) evidencing Phosphorous (mauve), arsenic (green), antimony (pink), indium (dark blue), gallium (red) and oxygen (light blue), composition profile along the dashed line indicated in figure a).

Figure 6 and figure S1 (in supplementary material) display the TEM analysis performed on sample A for NW devices grown inside a 100nm wide SiO<sub>2</sub> opening oriented in the [110] and [1-10] directions respectively. Despite the large lattice mismatch between GaSb and InGaAs, the High Angle Annular Dark Field (HAADF) images (Fig. 6a and S1a) indicate the absence of threading dislocations in the shell material. Figures 6b and S1b show that the mismatch is accommodated with an array of misfit dislocations (MD)

confined at the interface between InGaAs and GaSb. For the [110]-oriented device, the InGaAs core exhibits a triangular shape delimited by (111) planes in which is lying the array of MDs (white arrows). As highlighted in the inset of figure 6b, these MDs are 60° dislocations. For the [1-10]-oriented device, the InGaAs core is delimited by (111) and (113) facets at the topmost of the nanostructure (Fig. S1b) in which are lying 60° MDs (white down arrows) and two 90° MDs (white up-arrows) at the extreme top as highlighted in the inset images. EDX images (Fig. 6c and S1c) and the composition profile extracted in the middle of the NW (Fig. 6d and S1d) confirm the abruptness of the P/As and As/Sb interfaces with however a slight increase of In and Ga contents at InP/InGaAs and InGaAs/GaSb interfaces respectively. The different shapes of the InGaAs core and of its composition profile observed in both orientations are attributed to the different nature and thus the different surface energy of the facets in the two crystal orientations [10]. In the [110] direction, As-terminated (111)<sub>B</sub> facets are formed whereas III-element terminated (111)<sub>A</sub> and (113)<sub>A</sub> facets are formed in the other direction. The different properties of these facets in term of energy, roughness and reconstruction may explain different diffusion lengths for III-element adatoms and thus the different composition profiles that are observed.

## 2.2 InGaAs/GaAsSb core-shell nanostructures (sample B)

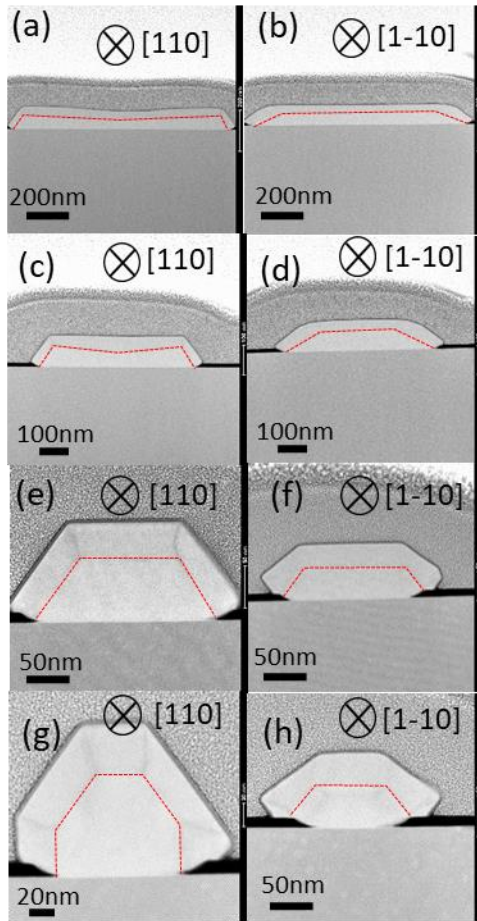


Figure 7 – HAADF images of the cross-section of in-plane InGaAs/GaAsSb nanostructures grown inside [110]-oriented (left images) or [1-10]-oriented (right images) SiO<sub>2</sub> openings of different widths from 1 $\mu$ m to 100nm (top to bottom). The interface between InGaAs and GaAsSb is highlighted by a red dashed line.

For sample B, the evolution of the shape of the InGaAs core with the width of the openings for a 50nm-thick deposition can be observed in the cross-section HAADF images displayed in figure 7. For large apertures (500nm and larger), InGaAs nanostructures are shaped with a (001) top surface (with a slight cusp) delimited by (111) and (113) lateral facets that form angles of 54° or 25° with the mask surface for [110] or [1-10]-oriented nanoribbons respectively. For smaller openings (200nm and below), (001) and (113) facets progressively disappear in aid of (111) facets. In the [110] direction, we can notice that the lateral growth of InGaAs on the SiO<sub>2</sub> mask is limited leading to the formation of vertical (-110) and (1-10) facets. The darker areas in the GaAsSb shell starting from InGaAs core angles can also be observed in these images. They indicate a strain field probably related to composition inhomogeneities.

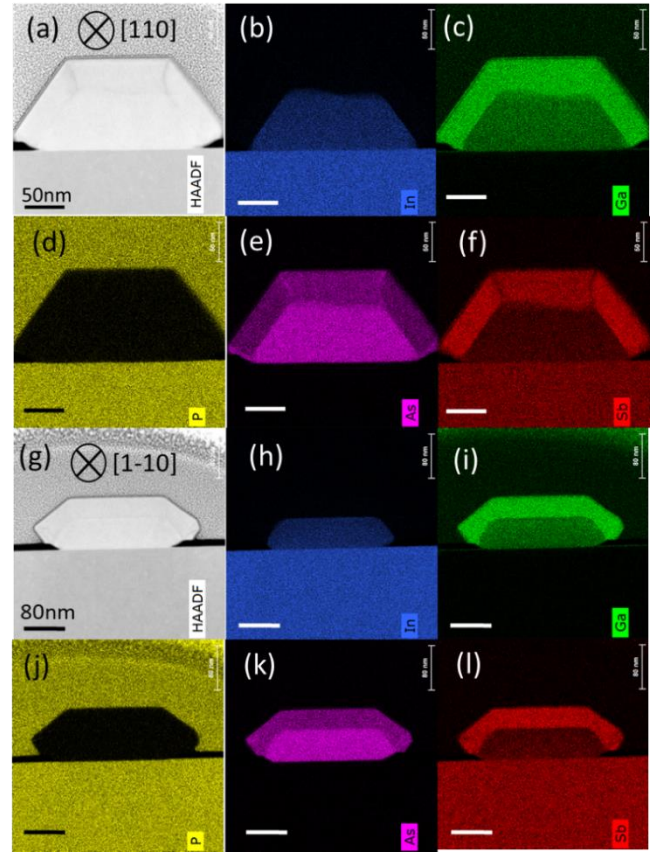


Figure 8 – TEM analysis of an in-plane InGaAs/GaAsSb NW of sample B grown inside a 200nm wide opening oriented either in the [110] or in the [1-10] direction. HAADF (a) and chemical composition (b-f) of the [110] NW. HAADF (g) and chemical composition (h-l) of the [1-10] NW.

The chemical composition displayed in figure 8 for 200nm wide in-plane InGaAs/GaAsSb NW confirms this hypothesis. We can clearly distinguish in the arsenic and antimony maps of the [110] NW, a slightly lower concentration of antimony in GaAsSb lying on top of the (001) InGaAs with respect of the GaAsSb part lying on the (111) surface of InGaAs. This phenomenon is even more pronounced in the angle. For Arsenic, the reverse phenomenon occurs. A quantitative analysis of the composition of the alloys in those different areas is proposed in figure 9. It confirms the previous observation with an As/(As+Sb) ratio of about 58-59% in the GaAsSb deposited on top of InGaAs for both orientation and larger than 63% on side facets for [1-10] NWs whereas a composition close to the InP lattice matched alloy (GaAs<sub>0.49</sub>Sb<sub>0.51</sub>) is measured for the material deposited on the (111) facets of [110]-oriented NWs. In the angles, the As content reaches up to 68% for this direction. Concerning III-elements, we can notice, as for sample A, a slight increase of the gallium content of InGaAs in the growth direction (zones 1, 2 and 3 in Fig. 9) whereas some residual indium (about 2%) can be measured in GaAsSb.



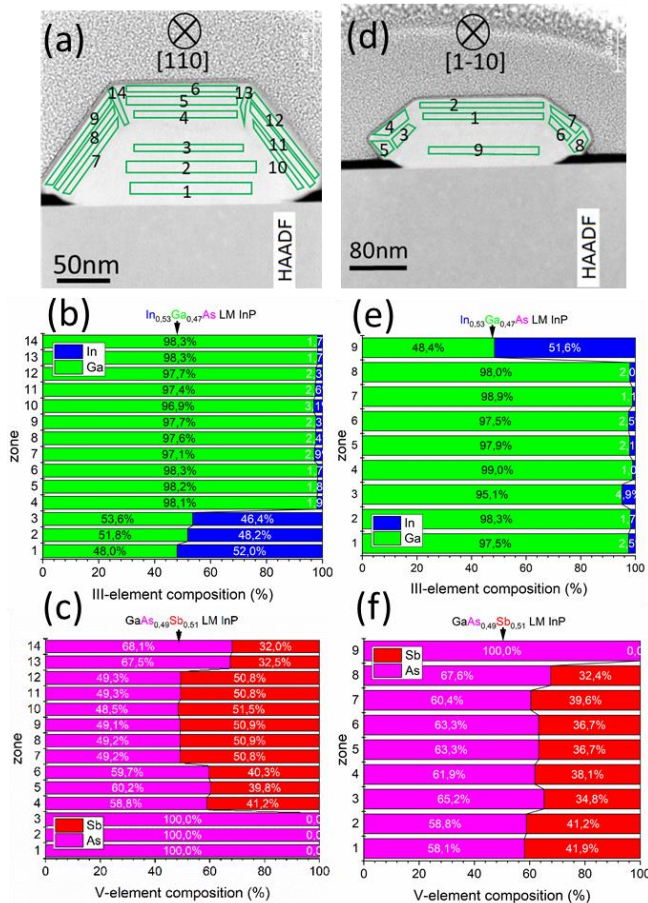


Figure 9 – Analysis of the alloy composition in different areas of the cross-section of a GaAsSb/InGaAs NW (sample B) grown inside 200nm wide openings oriented either in the [110] (left) or [1-10] (right) orientations.

The different GaAsSb composition in the sidewalls of the nanostructures between [110] and [1-10] oriented devices comes along with a different crystal quality along this (111) interface. Whereas a rather abrupt InGaAs/GaAsSb interface and a low defect density are achieved in the sidewalls of the nanostructures for the [110] NW, a more diffuse interface and the presence of microtwins in GaAsSb can be observed when NWs are along the other direction (figure S2).

The analysis of the chemical composition for NWs grown inside 100nm wide openings proposed in figures S3, S4 and S5 of the supplementary information evidences the same difference between [110] and [1-10] orientations.

### 2.3 InGaAs/GaSb in-line nanostructures (sample C)

The in-line configuration of sample C makes the cross-section analysis of the tunneling interface very difficult on narrow NWs. For that study, dedicated patterns grown inside 1µm wide openings were used as shown in Figure 10. For such large area patterns, the mismatch between InGaAs and GaSb can result in the presence of occasional voids along this

interface located in the region where InGaAs has been etched under the SiO<sub>2</sub> mask before GaSb regrowth. However, we can see, as it has been observed for narrow openings in figure 5, that the major part of the under-etched area (and the one where cross-section lamella has been withdrawn) is filled with GaSb. This is confirmed by the EDX analysis of figure 10 where a GaSb region under the SiO<sub>2</sub> mask can be clearly distinguished. This means that Ga and Sb adatoms are able to diffuse on the InP surface to reach the InGaAs interface under the mask. The HAADF image of figure 10c indicates a quite good material quality in this region with only two stacking faults lying in (111) planes near the InGaAs/GaSb interface. We believe that this defects originating at the GaSb/InP interface are probably due to the large lattice mismatch between the two materials and that they may disappear in GaSb nanostructures grown inside narrower SiO<sub>2</sub> openings. Indeed, STEM analysis performed on 150nm thick GaSb NWs grown inside narrower apertures (figure S6) indicates that these nanostructures can be free from threading defects in this case, the mismatch being accommodated by a regular array of MDs at the interface with the InP substrate [11]. In these images, as well as in the one of large ribbons from sample C shown in figure 10, we can notice the presence of a thin arsenic layer at the interface between GaSb and InP, which is due to the deoxidization of the InP surface under As<sub>4</sub> and atomic hydrogen flux.

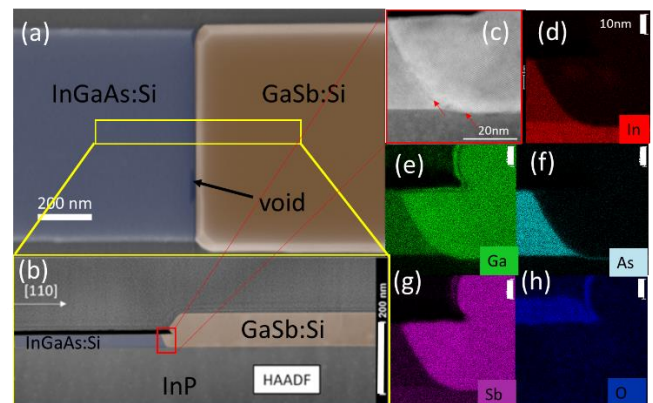


Figure 10 – Material analysis of in-plane InGaAs/GaSb tunnel junctions fabricated from a 1µm wide mask opening (sample C): false coloured plan view SEM image of the junction (a) showing the area where the TEM lamella observed in HAADF mode (b) has been extracted, zoom on the InGaAs/GaSb interface (c) with staking fault marked by red arrows, EDX analysis evidencing indium (d), gallium (e), arsenic (f), antimony (g) and oxygen (h).

## 3. Device characterization

### 3.1 Core-shell tunnel diodes

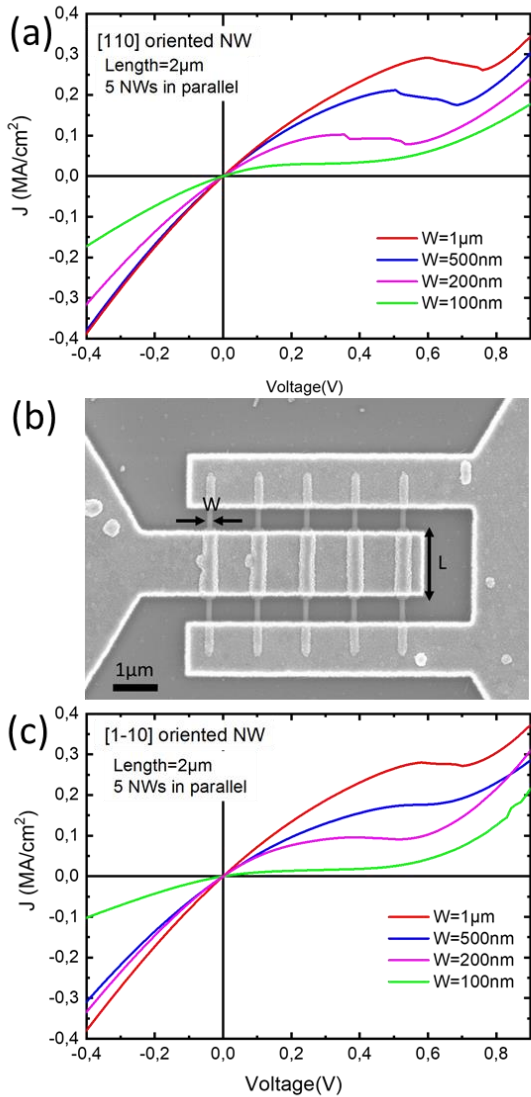


Figure 11 – Electrical characteristics of core-shell InGaAs/GaSb tunnel diodes (sample A) grown inside 5 parallel mask openings of different widths (from 100nm to 1 $\mu$ m) oriented either in [110] direction (top graph) or in [1-10] direction (bottom graph). The geometry of the devices is displayed in the SEM image (b).

Diodes from sample A composed of 5 parallel NWs with a GaSb contact length of 2 $\mu$ m and oriented in [110] and [1-10] directions are characterized at room temperature for different SiO<sub>2</sub> opening widths from 100nm to 1 $\mu$ m. The current is normalized with respect to the footprint area of InGaAs under the GaSb contact to estimate a value for the current density. The characteristics of the diodes, displayed in figure 11, exhibit an Esaki diode behavior with a large reverse bias current and a negative differential resistance (NDR) that can be observed for the widest diodes. The largest peak current density of about 300kA.cm<sup>-2</sup> is obtained for these diodes with a similar evolution for [110] and [1-10] oriented devices. For 100nm (and to a lower extent for 200nm) wide diodes, the

characteristics seem impacted by the series resistance as both tunneling current density (for negative voltage) and thermionic current density (for large positive voltage) are reduced. This could be related to the poor access resistances on InGaAs NWs. Transmission Line Measurements (TLM) performed on sample A for 100nm wide InGaAs NWs with different lengths and for which the GaSb shell has been completely removed reveal a contact resistance of about 300 $\Omega$  and a linear resistance of the NW of about 370 and 270  $\Omega/\mu$ m for [110] and [1-10] oriented NW respectively (figure S7). As the length of InGaAs NW between the two contacts of the diodes is 500nm, this means that the total access resistance for 5x100nm wide diodes is about 55  $\Omega$  and 36  $\Omega$  for [110] and [1-10] oriented NWs respectively (5 NWs with two contact each in parallel).

The J-V characteristics measured for single NW devices from sample B exhibit different evolutions with respect to the width of the mask openings (figures 12a and 12b). First of all, owing to the larger effective band gap at the InGaAs/GaSb interface [12], the current density is reduced with respect to sample A. In addition, the peak to valley current ratio (PVCRR) can be as large as 3 for the widest [1-10]-oriented devices and for the narrowest [110]-oriented devices (Figure 12c and 12d). The evolution of the diode characteristics with respect to their width is different for the two orientations. While for [1-10]-oriented devices PVCRR monotonically decreases, for [110]-oriented ones, it exhibits a minimum value for a 1 $\mu$ m width before increasing for the narrowest devices. Figures 12e and 12f show that this behavior is related to the peak current density evolution which decreases for narrow devices in the [1-10] direction whereas the opposite phenomena can be observed for the other orientation (except for the 100nm wide device). Taking into account the shape of the InGaAs core oriented along [110] which is delimited by (001) top surface and (111) side facets and the one along [1-10] which is delimited by (001) top surface and smaller angle (113) facets, we have plotted the relative importance of the different facet lengths with respect to the width of the opening (figures 12e and 12f). The strong correlation observed between the peak current and the relative importance of facets suggests that the tunneling current is mainly flowing through the (111) or the (001) interface for [110] or [1-10]-oriented devices respectively. For 3 $\mu$ m-wide openings, the relative importance of the current tunneling through side facets is reduced and the J-V curves are rather similar for both orientation. Beyond a tunneling current depending on the facet orientation, we can also notice that the reduction of tunneling current observed for narrow devices orientated along [1-10] direction goes along with a shift of the thermionic component of the current towards lower voltage (figure 12b). In the other orientation, thermionic component is not significantly varying down to 200nm but shift towards higher voltage for 100nm wide opening.



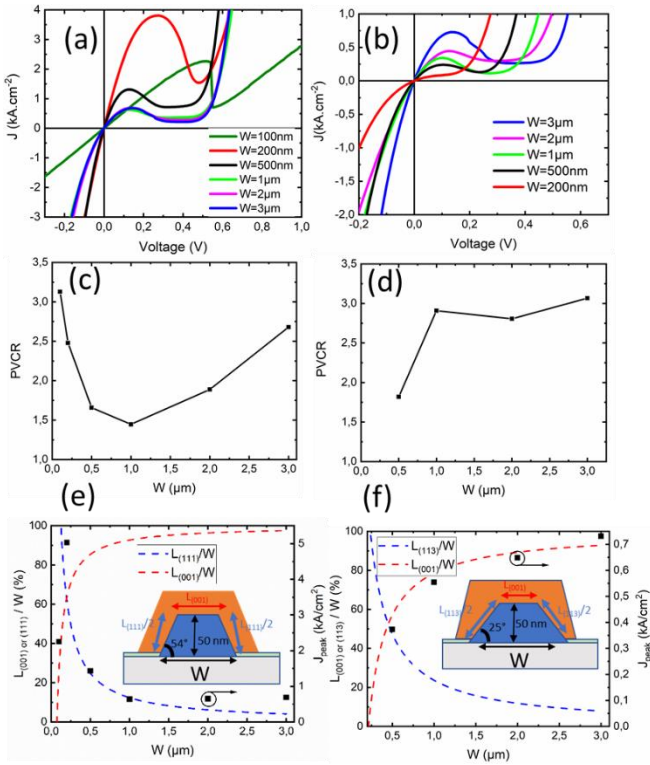


Figure 12- Current density vs voltage characteristics of in-plane InGaAs/GaAsSb tunnel diodes (sample B) of different widths and oriented along [110] (a) or [1-10] (b) directions. PVCOR deduced from  $J(V)$  characteristics (c and d for [110] and [1-10] directions respectively). Evolution of the peak current density with respect to the width of the diodes (black squares) compared to the theoretical evolution of the ratio between the length of the (001) (red dashed line) or the (111) or (113) (blue dashed lines) InGaAs facets for [110] (e) and [1-10] (f) directions respectively.

All these results are fully consistent with the material characterization results presented in part 2.2. For [1-10] devices, the higher As content observed in GaAsSb deposited on side facets (figures 9d, e and f) induces a larger effective bandgap at the lateral interface leading to a lower tunneling current density when the relative importance of these facets increases (for narrow devices). More, in this orientation, the conduction band offset is also reduced, resulting in the shift of the thermionic component of the current towards lower voltage. At the opposite, for [110]-devices, the larger Sb content in GaAsSb deposited on side facets (figures 9a, b and c) leads to a lower effective bandgap at these interfaces and thus increases the tunneling current density for narrow devices. In this orientation, the minimum conduction band offset between InGaAs and GaAsSb is at the (001) interface and thus no significant shift of the thermionic component of the current density is observed as the size is reduced down to 200nm (figure 12a). For the 100nm wide NWs, a large increase of the Ga content (57,5%) on the top of the InGaAs core (figure S5b) probably induces a barrier preventing electrons from flowing towards the top (001) interface. This

limits the thermionic current in this direction and also affects the tunneling current through the (111) facets as the series resistance (InGaAs resistivity and contacts) is obviously impacted by the larger Ga content at the surface of the NW. However, despite this, the high PVCOR measured for this NW confirms the good quality of the (111) tunneling interface.

### 3.2 In-line tunnel diodes

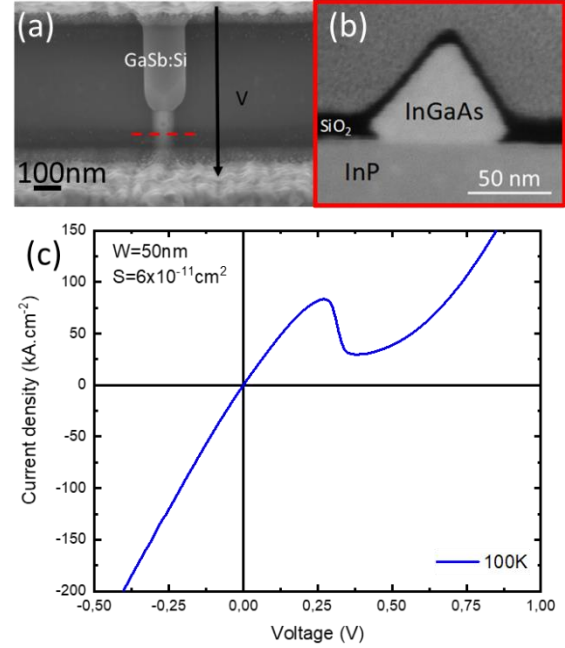


Figure 13 – SEM image of an in-plane in-line InGaAs/GaSb tunnel diode of sample C fabricated by two step SAG into a 50nm wide opening in the SiO<sub>2</sub> mask. The red dash line indicates where a lamella has been extracted by FIB to perform the STEM image (b). Associated  $J(V)$  characteristics measured at 100K (c).

For sample C, probably because of the presence of defects related to the mismatch accommodation between GaSb and InGaAs or InP, only some devices fabricated from the narrowest openings (50 or 100 nm wide) exhibit non-linear current-voltage curves characteristics of Esaki diodes. For these diodes, the current density is estimated by measuring the cross-section area of InGaAs using STEM (figure 13a and 13b). For 50nm wide mask openings, a cross-section of about  $6 \times 10^{-11}$  cm<sup>2</sup> is obtained. For this device, a peak current density of 83 kA/cm<sup>2</sup> with a PVCOR of 2.8 are reached at 100K (figure 13c). This values are comparable to the one obtained for InAsSb/GaSb NW diodes grown by Vapor Liquid Solid (VLS) epitaxy and transferred for processing [5]. An interesting behavior can also be noticed for this sample for tunneling devices fabricated from 100nm long GaSb nanocrystals inserted into a 100nm wide in-plane InGaAs NW (inset of figure 14). In this case, a symmetric I-V curve is measured with a NDR observed for both polarizations (figure 14), which is characteristics of back-to-back tunnel diodes and

indicates that the two tunneling interfaces exhibit similar properties [12].

The access resistances for the InGaAs and GaSb parts of the in-line tunnel junctions have been measured with TLM measurements on single InGaAs and GaSb NWs with different lengths (Figure S8). The reduced thickness of InGaAs with respect to sample A and B (30nm instead of 50 nm) results in much larger contact ( $3.8\text{k}\Omega$ ) and linear ( $1.1\text{k}\Omega/\mu\text{m}$ ) resistances. For GaSb NWs, a mean contact resistance of  $2.6\text{k}\Omega$  and a linear resistance of  $3.4\text{k}\Omega/\mu\text{m}$  are measured. As the length separating the tunnel interface from the two contacts is about  $1.5\mu\text{m}$ , this means that the access resistance in a 100nm wide in-line tunnel diode is as large as  $13\text{k}\Omega$ . This is lower than the resistance of the tunnel interface that can be deduced from the peak current and voltage ( $54\text{k}\Omega$ ) but it suggests that the properties of in-line tunnel junctions could be further improved by reducing the distance between contacts and connecting NW to a large area mesa as has been done for sample B.

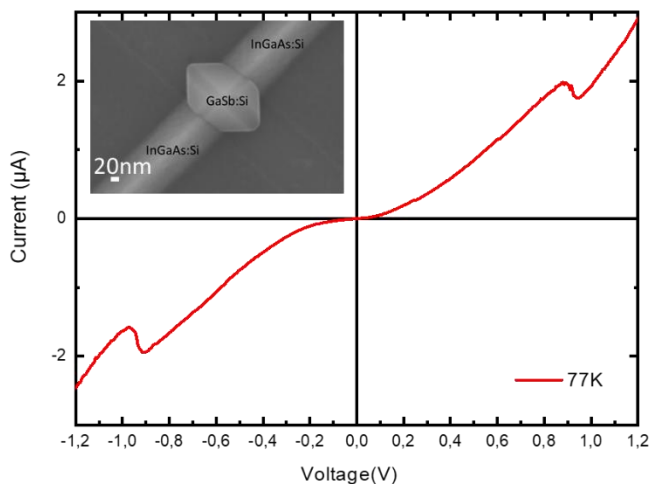


Figure 14 –  $I(V)$  characteristics of a tunnel diode formed by the insertion of a GaSb nanocrystal inside an InGaAs NW of sample C (SEM image of the device shown in the inset).

#### 4. Conclusion

We have shown different approaches for the fabrication of in-plane tunnel diodes in the staggered InGaAs/Ga(As)Sb system using selective area epitaxy. Despite the strain relaxation and interface dislocation formation, Esaki tunnel diodes with a large current density can be achieved in the InGaAs/GaSb system both with a core-shell geometry and in an in-line configuration minimizing the device capacitance. For the core/shell InGaAs/GaAsSb system, we have demonstrated a strong impact of the NW orientation on the composition profile of the alloys resulting in different diode electrical

characteristics. We believe that these results could contribute to the development of efficient tunnelling devices for high frequency detection or low power electronics.

#### 5. Acknowledgements

This work was partly supported by the French Renatech network, the European Community, the Région Hauts de France and the *Agence Nationale pour la Recherche* for funding the Titan Themis microscope through the EQUIPEX TEMPOS (10-EQPX-0050).

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