Improved Measurement Accuracy for Junction-to-Case Thermal Resistance of GaN HEMT Packages by Gate-to-Gate Electrical Resistance and Stacking Thermal Interface Materials

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Shengchang Lu, *Student Member, IEEE*, Zichen Zhang, *Student Member, IEEE*, Cyril Buttay, *Senior Member, IEEE*
Khai D.T. Ngo, *Fellow, IEEE*, and Guo-Quan Lu, *Fellow, IEEE*

***Abstract* – Accurate measurements of the junction-to-case thermal resistances of power devices or module packages are necessary for validating the thermal design of the package as well as of the entire converter system. Although accurate measurements can be obtained for Si and SiC packages by the JESD51-14 standard, no standard has been established for GaN packages. A main reason for this shortcoming is the lack of accurate techniques for measuring the device's junction temperature. In this work, a custom package of a (650 V, 150 A) eGaN HEMT with two gate pads was fabricated, and then its junction-to-case thermal resistance was measured by combining two techniques to improve the accuracy: (1) using the device's gate-to-gate electrical resistance as the temperature-sensitive electrical parameter; and (2) measuring the thermal resistance as a function of added layers of thermal interface materials. The first gives a sensitivity of 4.7 mΩ/°C and is instantaneous and immune to any transient behavior of the device. The second eliminates the need for accurate measurement of the case temperature. The package's junction-to-case thermal resistance was determined by extrapolating the discrete thermal resistance data points in the plot to zero layer of thermal interface. An analytical expression was derived to guide the extrapolation and was validated by FEA simulations. The measurement procedure was tested using two different thermal interface materials. The difference between the two experimental measurements was within 24%, and both are in good agreement with the simulated result.**

***Index Terms* – packaging of gallium nitride high electron mobility transistor, junction-to-case thermal resistance, gate-to-gate electrical resistance as temperature sensitive electrical parameter**

I. INTRODUCTION

Application of gallium nitride high-electron mobility transistors (GaN HEMTs) in power converters has the potential to further increase the efficiency and power density because of their low conduction loss, low switching loss, and high temperature capability [1-3]. However, packaging these fast-switching devices is challenging because of the requirement for low parasitics and low junction-to-case thermal resistance, $\mathcal{R}_{thJC}$ [4, 5]. One of the first steps in developing a device or module package is to layout the package structure and select materials, followed by running electrical and thermal simulations to determine package parasitics and thermal resistances. Experimental verification of the electrical and thermal simulations is key to ensure the success of a package development. Of the two, thermal measurements are more difficult and generally less accurate. And, this is especially so for GaN packages, hampering the development of GaN packaging. A main challenge of measuring $\mathcal{R}_{thJC}$ of a GaN package is the lack of accurate techniques to determine the device's junction temperature, T_j.

Although techniques for direct measurement of T_j have been developed [6, 7], a more widely practiced technique for measuring T_j is through one of the device's temperature-sensitive electrical parameters (TSEPs) [8-13], such as the threshold voltage (V_{th}), gate leakage current (I_g), drain current (I_d), or on-resistance (R_{on}). For Si and SiC power devices, the temperature dependence of any of the TSEPs is strong and well characterized. And, one can follow the IEEE JESD51-14 standard [14] to accurately measure the $\mathcal{R}_{thJC}$ of the package. However, the common TSEPs of a GaN HEMT lack sufficient sensitivity or stability due to charge trapping effect [15, 16] from device switching action. Recently in [17, 18], the researchers fabricated GaN HEMT devices with two gate pads. They showed that the gate end-to-end or gate-to-gate electrical resistance, R_{g2g}, can be used as a reliable TSEP. However, because they did not fabricate packages for their devices, they did not apply the technique to measure $\mathcal{R}_{thJC}$.

In this work, we packaged a commercial (650 V, 150 A) eGaN device with two gate pads for the purpose of accurately measuring $\mathcal{R}_{thJC}$ of the GaN package. Two techniques were combined to improve the accuracy: (1) using R_{g2g} as the TSEP and (2) making multiple thermal resistance measurements with stacked layers of a thermal interface material (TIM). The stacked-TIM technique was employed to reduce inaccuracy in determining the package case temperature. In the following, we describe the package fabrication and show that R_{g2g} of the device was a sensitive and stable parameter for measuring T_j. Then, a procedure is presented for determining the package $\mathcal{R}_{thJC}$ by extrapolating thermal resistance data measured at different layers of TIM. Finally, validation of the procedure is

demonstrated from measurements obtained using two different TIMs and the results of FEA thermal simulations.

II. GAN HEMT PACKAGE FABRICATION FOR THERMAL CHARACTERIZATION

The GaN HEMT chosen for this study is GaN Systems's Schottky type *p*-GaN gate HEMT rated for 650 V and 150 A with the part number of GS-065-150-1-D. The die has two gate pads connected internally. Fig. 1(a) is a schematic of the cross-section of the package and (b) a top view of a completed package. The GaN die was attached by silver sintering to a patterned direct-bond copper (DBC) substrate with a silver surface finish, and the three device terminals (gate, source, and drain) were connected by a 2-mil gold wire to the substrate. Copper leads were soldered to the DBC substrate for outside connections. The housing for mechanical support was made of Duration® polyethyleneimine (PEI) from Mitsubishi Chemical Advanced Materials. The space inside the housing was filled with a silicone (Nusil-2188 from Avantor) for insulation and protection.

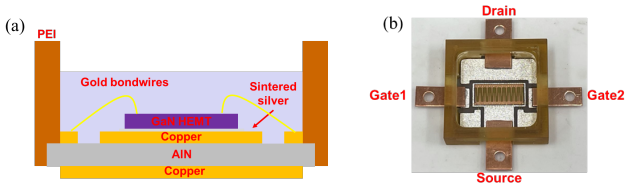

Fig. 1: (a) Schematic of the package cross-section; and (b) top view of a completed eGaN package.

III. TSEP CHARACTERIZATION

The two gate leads of the package shown in Fig. 1(b) were purposely added for ease of characterizing R_{g2g} as a TSEP. Fig. 2(a) shows the experimental setup. The package was clamped to a hotplate with two layers of a TIM and a thermocouple in between. The gate-to-gate electrical resistance was measured by the four-point probe method at a constant current of 50 mA. The hotplate was heated from room temperature to 120 °C at an increment of 5 °C, and R_{g2g} was recorded after the package temperature reached a steady state at each increment. Plotted in Fig. 2(b) is R_{g2g} versus temperature obtained on one packaged die. The dashed line is a linear fit to the data. Measurements on five different dice that were packaged in the same way showed a 3% device-to-device variation in R_{g2g}.

To compare R_{g2g} as a TSEP with the common TSEPs of Si and SiC devices, threshold voltage (V_{th}), forward voltage drop (V_{sd} or V_F), and on-resistance (R_{on}) of the packaged GaN device were also characterized. V_{th} was the gate-source voltage measured at I_D = 10 mA. V_{sd} (V_F) was the voltage drop across the device when it is operating in the third quadrant at 10 mA. R_{on} was measured at V_{GS} = 6 V and I_D = 40 A by a curve tracer. The three major factors considered in the comparison were: sensitivity, immunity to electron trapping, and online capability. For a fair comparison of the sensitivity, all the units of the TSEPs were converted to mV/°C. The raw and converted results are shown in Table I. The TSEP of V_{th} is the least sensitive. We also observed a shift in V_{th}, as high as 0.5 V, upon device switching. It was likely the result of electron trapping or hole accumulation/depletion[15, 16]. This makes V_{th} an unreliable TSEP for measuring T_J. Since GaN HEMTs have no build-in body diodes, V_{sd} is similar to V_{th} in the HEMT structure and thus is also influenced by electron trapping. R_{on} is the most sensitive TSEP and is also capable of online T_J measurement. However, it can be influenced by electron trapping during switching actions. The TSEP of R_{g2g} has good sensitivity. And, it is immune to electron trapping because it is simply the resistance of a copper trace in the device structure, thus it is also a good TSEP for online measurement.

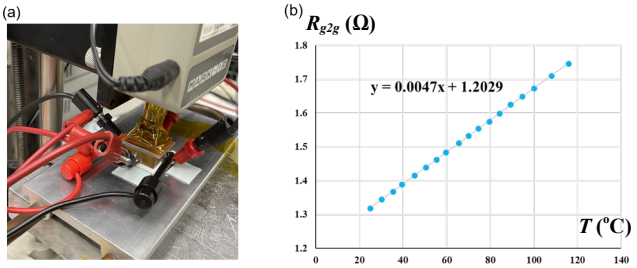

Fig. 2: (a) Overview of calibration setup; and (b) R_{g2g} versus temperature calibration result.

TABLE I.
COMPARISON OF DIFFERENT TEMPERATURE SENSITIVE ELECTRICAL PARAMETERS

TSEP	V_{th}	V_{sd} (V_F)	R_{on}	R_{g2g}
Raw Sensitivity	0.2 mV/°C	0.35 mV/°C	13.75 μΩ/°C	4.7 mΩ/°C
Converted Sensitivity in mV/°C	0.2 mV/°C	0.35 mV/°C	0.55 mV/°C	0.24 mV/°C
Immunity to electron trapping	No	No	No	Yes
Online T_J capability	No	No	Yes	Yes

IV. STACKED-TIM TECHNIQUE

Another requirement for accurate measurement of $\mathcal{R}_{thJC}$ is accurate measurement of the case temperature, T_C. The procedure prescribed in the JEDEC standard suggests making a hole or a groove in the heatsink for embedding a thermocouple. But the non-uniform distribution of the case temperature and a large temperature gradient between the case and heatsink make it difficult to accurately measure the case temperature. To avoid the T_C measurement error, Transient Dual Interface Measurement (TDIM) technique was proposed in [19]. With this technique, $\mathcal{R}_{thJC}$ is determined by finding the point of deviation between two transient cooling curves or structure function plots measured using different interface materials between the package and the heatsink. However, the transient heat flow inside the package may differ from the steady-state heat

flow. So, the TDIM result is not a true measure of $\mathcal{R}_{thJC}$, which is defined under a thermal steady-state condition. Furthermore, the TDIM result is influenced by subjective decisions in, e.g. offset correction and determination of the deviation location in the structure function plots [20].

To remove the influence of T_C measurement on the steady-state $\mathcal{R}_{thJC}$ measurement, we introduce the Stacked-TIM technique. The technique involves making multiple measurements of thermal resistance with varying number of layers of a TIM stacked between a package and a heatsink. Fig. 3(a) is a schematic showing a GaN package clamped to a heatsink with a few layers of a TIM in between. A buffer layer, which can be a TIM layer, is placed on top of the heatsink. A thermocouple is embedded between the buffer layer and the TIM stack. To ensure good thermal contact and minimal temperature measurement error, the thermocouple bead should be small, at least five times smaller than the buffer layer thickness. The thermocouple measures the temperature of the bottom surface of the TIM stack, labeled as T_{TIM}.

As the package is heated to a thermal steady state from the power dissipated by the device, T_{TIM} is measured by the thermocouple, and T_J is determined from R_{g2g} and the calibration curve shown in Fig. 2. The steady-state thermal resistance from device junction to the bottom surface of the TIM stack, $\mathcal{R}_{thJTIM}$ is found by:

$$\mathcal{R}_{thJTIM} = \mathcal{R}_{thJC} + \mathcal{R}_{thCTIM} = \frac{T_J - T_{TIM}}{P} \tag{1}$$

where $\mathcal{R}_{thCTIM}$ is the case-to-TIM thermal resistance. By varying the number of layers in the TIM stack or the total thickness, t, of the stack, a plot of $\mathcal{R}_{thJTIM}$ versus t is obtained, like the one depicted in Fig. 3(b). At t = 0, $\mathcal{R}_{thJTIM} = \mathcal{R}_{thJC}$, $\mathcal{R}_{thJC}$ can be obtained by extrapolating the data plot to the y-axis. Because of the heat spreading effect in the TIM stack, $\mathcal{R}_{thJTIM}(t)$ is a nonlinear function. Thus, one needs a nonlinear fitting curve of the data points to guide the extrapolation.

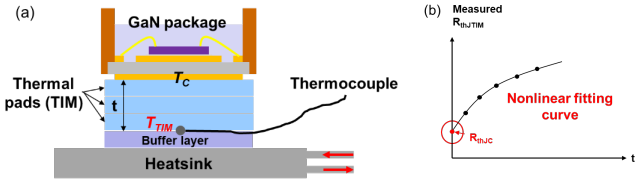

Fig. 3: (a) Schematic of the measurement setup with the Stacked-TIM technique, and (b) depiction of $\mathcal{R}_{thJTIM}$ versus t plot with the nonlinear fitting curve for extracting $\mathcal{R}_{thJC}$.

Fig. 4(a) and (b) show a simplified thermal model for finding an analytical expression for the fitting curve. Assuming a heat spreading angle, θ, in the TIM stack, $\mathcal{R}_{thCTIM}$ in Eq. (1) is derived to be:

$$\mathcal{R}_{thCTIM} = \frac{1}{k} \cdot \int_0^{t0} \frac{dt}{(x_1 + 2cot\theta \cdot t)(y_1 + 2cot\theta \cdot t)} \tag{2}$$

where k is the thermal conductivity of the TIM material, t_0 is the total thickness of the TIM stack, and (x_1, y_1) is (width, length) of the TIM area in direct contact with the package case. After the definite integration, $\mathcal{R}_{thJTIM}$ becomes:

$$\mathcal{R}_{thJTIM} = \frac{1}{k(y_1 - x_1)} \cdot \ln\left(\frac{t + \frac{x_0}{2cot\theta}}{t + \frac{y_0}{2cot\theta}} \cdot \frac{y_0}{x_0}\right) + \mathcal{R}_{thJC} \tag{3}$$

Thus, the nonlinear behavior of the $\mathcal{R}_{thJTIM}(t)$ fitting curve follows a natural log. And, the two unknowns, $\mathcal{R}_{thJC}$ and θ, can be obtained by fitting the data points to Eq. (3). However, the analytical function is cumbersome for data fitting. To simplify the following discussion, we set $\theta = 45°$, a reasonable assumption for heat spreading in a homogeneous substrate [21]. Now, Eq. (3) becomes:

$$\mathcal{R}_{thJTIM} = a \cdot f(t) + \mathcal{R}_{thJC} \tag{4}$$

where $a = \frac{1}{k}\frac{1}{y_0 - x_0}$, and $f(t) = ln\left(\frac{2t + x_0 + 2 \cdot t_{DBC}}{2t + y_0 + 2 \cdot t_{DBC}} \cdot \frac{y_0 + 2 \cdot t_{DBC}}{x_0 + 2 \cdot t_{DBC}}\right)$. ($x_0$, y_0) is (width, length) of the device chip as shown in Fig. 4(b). The only unknown in Eq. (4) is $\mathcal{R}_{thJC}$, which can be readily obtained by fitting the data points to Eq. (4).

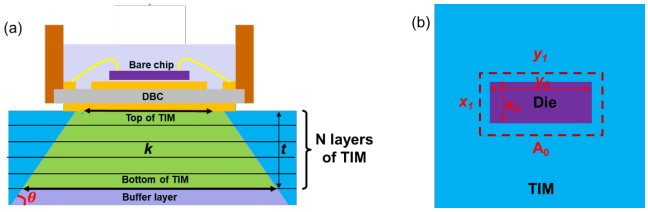

Fig. 4: A simple thermal model for deriving an analytical expression for the nonlinear fitting curve. (a) Cross-sectional view of heat spreading in the TIM stack; and (b) top view showing the dimensions of the die and the package case.

Fig. 5 is a flow chart summarizing the procedure for determining $\mathcal{R}_{thJC}$ by using R_{g2g} as the TSEP to measure T_j and the Stacked-TIM technique to avoid inaccurate T_C measurement. In the chart, n is the number of layers of TIM in the TIM stack, $T_{TIM\#n}$ is the temperature at the bottom of the TIM stack with n number of layers, and $R_{thJTIM\#n}$ is the thermal resistance from junction to the bottom surface of the TIM stack with n number of layers.

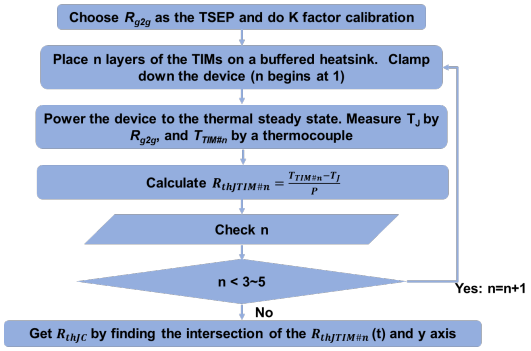

Fig. 5: A procedure for improved measurement of $\mathcal{R}_{thJC}$ of a GaN HEMT package using R_{g2g} as the TSEP and Stacked-TIM technique to avoid inaccurate measurement of the case temperature.

V. TESTING AND VALIDATION

We applied the measurement procedure described in the flow chart above to determine $\mathcal{R}_{thJC}$ of the GaN HEMT package in Fig. 1. Since the result should be independent of the type of TIM used for the measurement, we ran the measurements using two types of TIM: TIM_A (TG-A1250 from t-Global Technology) of 0.5 mm thick and TIM_B (TG-A6200) of 0.5 mm thick. With each type, a layer serving as the buffer was first laid down on a water-cooled plate. Then, a K-type thermocouple bead of 0.1 mm in diameter was placed at a location directly beneath the chip center, followed by layers of the TIM and the package under test. To ensure good thermal contact, the stacked structure was clamped together under a pressure suggested for each specific type of TIM.

For each TIM, five measurements were taken at thermal steady state, one for each layer of the TIM added to the TIM stack. The self-heating power was controlled to keep the same T_J in all the measurements. Plotted in Fig. 6 are the measured $\mathcal{R}_{thJTIM}$ in red and blue circles versus t from the test runs with TIM_A and TIM_B, respectively. The thickness, t, of the TIM stack is equal to the number of layers, n, multiply by the thickness of each layer. Each set of data points were fitted to Eq. (4). The dash lines in the figure are the fitted nonlinear curves. The measured junction-to-case thermal resistance, $\mathcal{R}_{thJC}$, at t = 0, was found to be 0.100 °C/W using TIM_A and 0.124 °C/W using TIM_B, a difference of 24%.

To further validate the measurement procedure, thermal simulations by finite element analysis (FEA) in ANSYS Workbench under Steady-State Thermal Analysis were run for each of the measurement configurations and for $\mathcal{R}_{thJC}$ of the package. The points plotted in red and blue crosses in Fig. 6 are the simulated $\mathcal{R}_{thJTIM}$ with TIM_A and TIM_B, respectively. The simulated and measured points nearly overlap with each other. The simulated $\mathcal{R}_{thJC}$ is 0.121 °C/W, which is also in good agreement with the two experimental values.

The difference between the two extracted $\mathcal{R}_{thJC}$ may partly be attributed to misplacement of the thermocouple bead off the designated location and the nonuniform temperature distribution in the buffer layer. A separate FEA thermal simulation showed that if the thermocouple was misplaced by 1 mm, the extracted $\mathcal{R}_{thJC}$, would be off by 12%. Another contribution to the difference may come from inaccurate or imprecise temperature measurement. We believe that by using a thermocouple with an ultra-small bead, the accuracy of $\mathcal{R}_{thJC}$ can be improved.

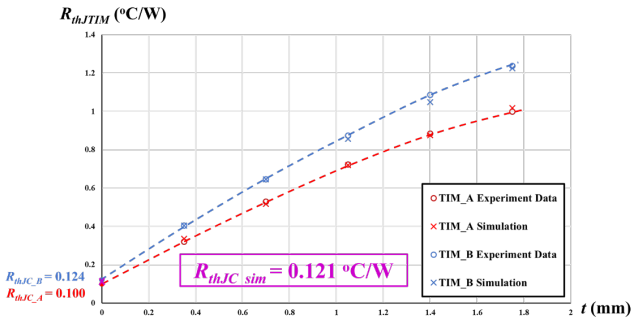

Fig. 6: Plots of the measured (red and blue circles) and simulated (red and blue crosses) junction-to-TIM thermal resistances with each TIM type. The dash lines are the fitted curves of the experimental data by using Eq. (4). The intercepts of the fitting curves on the y-axis are the experimentally determined $\mathcal{R}_{thJC}$.

VI. SUMMARY

A procedure was introduced to improve the accuracy for measuring the junction-to-case thermal resistance ($\mathcal{R}_{thJC}$) of GaN HEMT packages. The procedure takes advantage of a GaN HEMT with two gate pads for accurate T_j measurement by utilizing the gate-to-gate electrical resistance (R_{g2g}) as the TSEP with immunity to charge trapping and online measurement capability. The procedure also avoids direct case-temperature (T_C) measurement, which is inaccurate due to poor thermocouple/heatsink contact. Instead, the temperature at the interface between two thermal interface materials is measured. By varying the thickness of one TIM, e.g. through stacking multiple layers together, the junction-to-TIM thermal resistance, $\mathcal{R}_{thJTIM}$ versus the TIM stack thickness, t, is measured. Then, with the help of an analytical equation for the dependence of $\mathcal{R}_{thJTIM}$ on t, $\mathcal{R}_{thJC}$ can be determined by curve fitting and extrapolation to t = 0. The measurement procedure was tested using two different types of TIM on a custom package of an eGaN (650 V, 150 A) HEMT. The two measured $\mathcal{R}_{thJC}$ were found within 24% of each other. The measurements were also compared with FEA simulated results, and excellent agreements were observed.

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