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Design of zero bias power detectors towards power consumption optimization in 5G devices

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Abstract

This paper presents the design and characterization of zero bias power detectors, based on MOSFET transistors, integrated in SiGe 55-nm BiCMOS technology from ST-Microelectronics. The working frequency bands of the circuits are located in the range (38-55) GHz, dedicated to optimize the power consumption in 5G devices. Three NMOS categories available in the technology are used (GP, LP, HPA), the aim is to design several detectors based on different NMOS categories in order to compare their performances. In addition, a detector based on a stack of 6 LP transistors is designed in order to increase the dynamic range. Compared to recent works, the HPA detector exhibits a very good performance with very low noise equivalent power value (NEP) $3.8 \text{ pW}/\sqrt{\text{Hz}}$ and large dynamic range of 67 dB. The extracted voltage sensitivity values of these detectors are between (850 - 1400) V/W showing good agreements with the simulation results.

Keywords: 5G and IoT sensors, 55-nm BiCMOS, dynamic range, NEP, zero bias detector.

1. Introduction

The 5G is the new generation of mobile network that provides impressive data rate, thanks to the large frequency bandwidth, ultra-low latency, and ten-times geographic coverage. The IoT sensors are supported by the 5G systems, those sensors will be located everywhere (car, home, industrial health monitoring, etc.) providing many applications and increasing machine-to-machine connectivity [1]. Huge number of IoT sensors will be installed, hence, it will not be possible to provide batteries for all of these sensors [2]. Moreover, working at high frequencies leads to higher losses in transmission lines and lower devices efficiencies, hence, higher power has to be provided in order to compensate these losses. Therefore, energy efficiency is an important issue to be considered in 5G systems [3]. In this context, increasing the battery life time is proposed by harvesting the wireless energy in IoT devices [4]. In addition, several solutions are proposed in order to reduce power consumption in power amplifiers [5], [6]. The average power tracking (APT) technique is one of those solutions, where power detector is employed to track the slow (average) variations of the envelope signal in order modulate the biasing levels of power amplifiers. To take the full benefit of (APT) technique, the power consumption of the detector has to be minimum.

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In this context, we present the design and characterization of four zero bias detectors (ZBDs), based on MOSFET transistors, integrated in the 55-nm SiGe BiCMOS technology from ST-Microelectronics. The working frequency bands are in the range (38- 55) GHz allowing the detectors to cover several 5G bands [7]. Since the detectors presented in this work do not require any power source, they can be the optimum solution for the 5G applications, where high power efficiency is required (such as APT technique).

2. Design

The 55-nm BiCMOS technology provides three categories of low threshold NMOS transistors (named as GP, LP and HPA). The GP transistor stands for general purpose, it is considered as the standard NMOS transistor of the technology. The LP transistor stands for low power, it is used for low power and high frequency applications. The HPA transistor stands for high performance analog, it was developed for analog applications by exhibiting higher gain and linearity.

The objectives of this work are to: (i) Design three ZBDs based on single transistor (using GP, LP, HPA) as in Fig. 1 (a). The aim is to investigate the potential of those transistors in this application and compare their performances. In this work, we will name the detectors by the transistor name. (ii) Design a ZBD (named as LP Stack detector) based on stack of 6 (LP) transistors in order to achieve larger dynamic range (Fig. 1 (b)).

The Cadence virtuoso software (which provides the design kit of the technology) is used to design and simulate the detectors. Matching networks are designed at the detectors inputs allowing to absorb the maximum RF power (P_{in}), meanwhile avoiding standing waves. The DC block (MOM) capacitor is used to decouple the DC output voltage with the input RF circuits. The transistors are used in diode connected configuration without bias, thus, they are operated in sub-threshold region. The exponential dependence between the voltage and current of the drain is used for square-law detection. The resistor R_{att} (50Ω) is connected in series with the transistor in order to help matching the detector, and also, maintaining a linear response at higher levels of input power ($P_{in} > -30$ dBm) by absorbing (thus attenuating) part of input power (P_{in}). However, attenuating the RF power decreases the voltage sensitivity value (γ), therefore, using stack of 6 transistors is proposed in order to overcome this drawback.

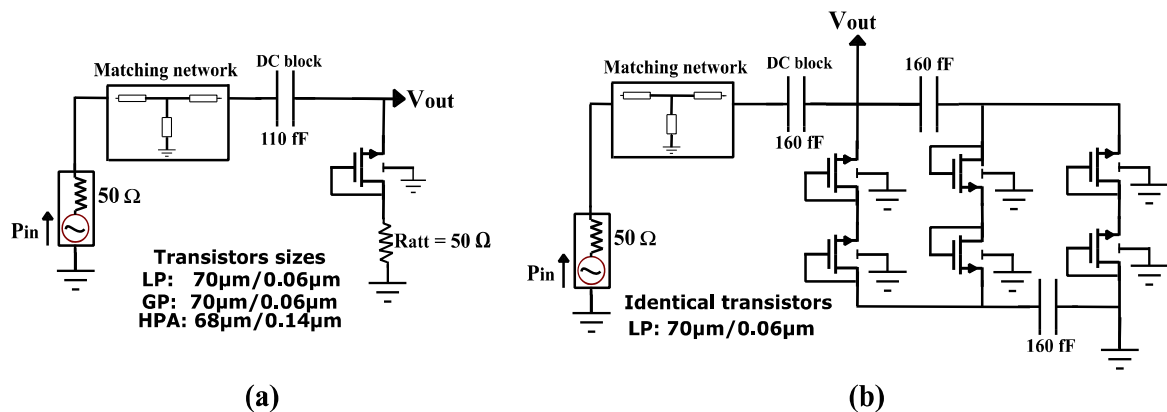


Figure 1. Detector schematic based on: (a) single transistor, (b) stack of 6 transistors.

When the RF power (P_{in}) is applied on stack of N identical transistors, each will absorb (P_{in}/N). Hence the compression point (in γ vs P_{in} curve) is increased by N times, meanwhile high sensitivity value is maintained since the total power (P_{in}) is absorbed and converted into DC. The stack of N transistors can be established using two topologies as shown in Fig .2. For DC and low frequencies, the transistors are connected in series for both topologies. However, they exhibit different impedances for the RF signal (high impedance for topology (a), and low impedance for topology (b)). Fig 1(b) shows a hybrid topology which we propose in order to obtain a moderate impedance. The number of stacked transistors is limited by the complexity of the required matching network, and also, the losses added by coupling capacitors.

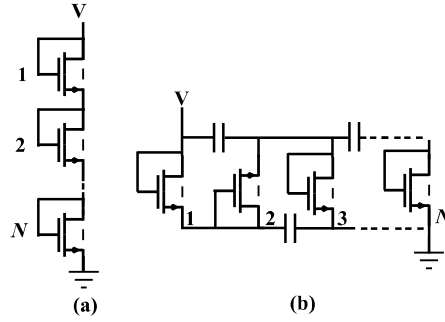


Figure 2. Stack of N transistors using: (a) series topology, (b) parallel topology.

The transistors are sized, so they exhibit certain impedances in order to produce the desired voltage sensitivity value. For small RF signal, the impedance of diode connected transistor can be represented by the channel resistor (R_p) in parallel with the parasitic capacitor (C_p). In GP and LP transistors, the impedance of C_p is more dominant than the R_p , thus, adding a series resistor (R_{att}) is necessary to help matching the detector by increasing the real part impedance. On the contrary, the R_p impedance in HPA transistor is more dominant, therefore, the HPA detector is designed without R_{att} .

Harmonic balance simulation is used to simulate the output DC voltage V_{out} when the input RF power is applied. In addition, matching the detectors for large signal input power (up to -10 dBm) is also verified using large signal S-parameter simulation (LSSP).

3. Measurements

3.1 Voltage sensitivity definition

When the input RF power is in the states (OFF) and (ON), we define the corresponding DC output voltages (V_{OFF}) and (V_{ON}) respectively. For low level of RF power, the voltage difference ($V_{OFF} - V_{ON}$) is proportional to the injected RF power (P_{in}). The voltage sensitivity (response coefficient in V/W) of the detector can be defined by:

$$\gamma = \frac{V_{OFF} - V_{ON}}{P_{in}} \quad (1)$$

3.2 Measurement of the reflection coefficient

Fig. 3 shows the measured and simulated S_{11} curves of the GP, LP, HPA and LP Stack detectors. These detectors are matched in the frequency bands (38-48), (40-50), (42-50) and (42-55) GHz respectively, where $|S_{11}| \leq -8$ dB. The measured S_{11} curves show some shifts in frequency compared to simulations, thus some deviations in S_{11} values are obtained. Those deviations are due to the accuracy limitations of the simulation models, and also, the small connection lines between the elements which are not included in the simulation schematics.

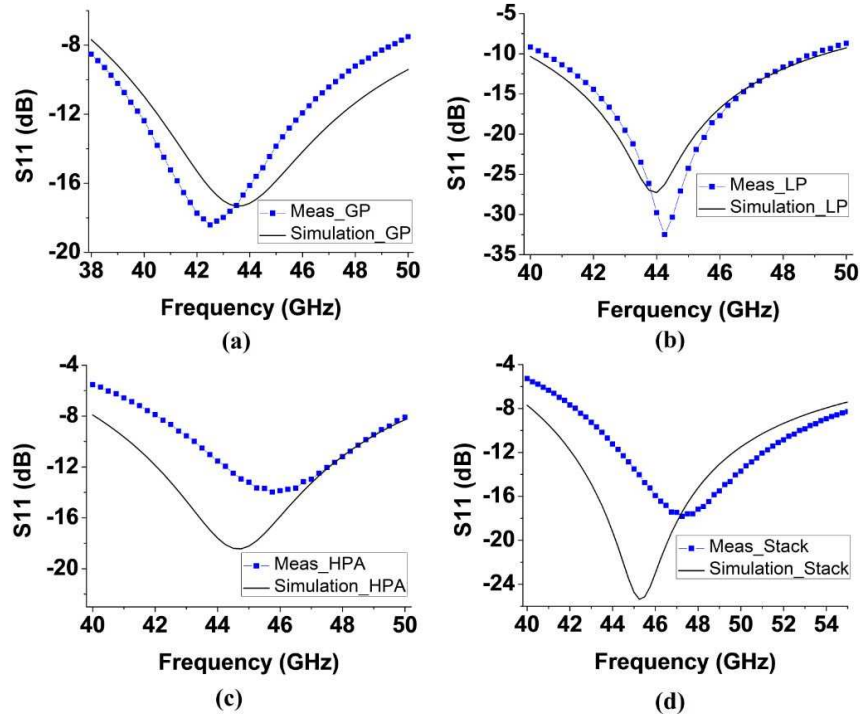


Figure 3. The measured and simulated S_{11} of the detectors.

3.3 Measurement of the voltage sensitivity

The block diagram of the bench used to extract the voltage sensitivity is shown in Fig. 4. The detector is probed using coplanar Infinity probe i67 at the input (RF side), and a high impedance Cascade (form-factor)-Microtech probe FPX-100X at the output (DC side). The DC voltmeter Agilent 34461A is used to measure the output DC voltage (V_{out}), this voltmeter has an internal impedance about 10 G Ω . The PSG (Performance Source Generator E8257D) is used to inject the RF power, where the input power P_{in} is defined at the input pad plane as shown in Fig. 4. In order to shift the reference power plane from P_{in}' to P_{in} , the losses of the RF cable and input pad are subtracted from the PSG injected power. To extract the voltage sensitivity values, the (V_{OFF}) and (V_{ON}) are measured and then applied in (1).

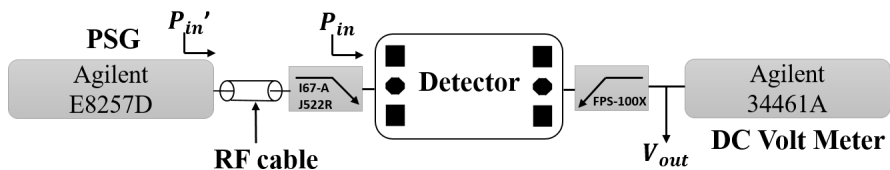


Figure 4. The bench diagram used to extract the voltage sensitivity.

Fig. 5 shows the measured and simulated sensitivity curves versus the frequency. Based on the obtained results, it can be concluded that: (i) The sensitivity curves are relatively flat in the frequency band of interest for the GP and HPA detectors. (ii) A good agreement is obtained between the simulation and measurement results, where the deviation is smaller than 10% for all the frequency band.

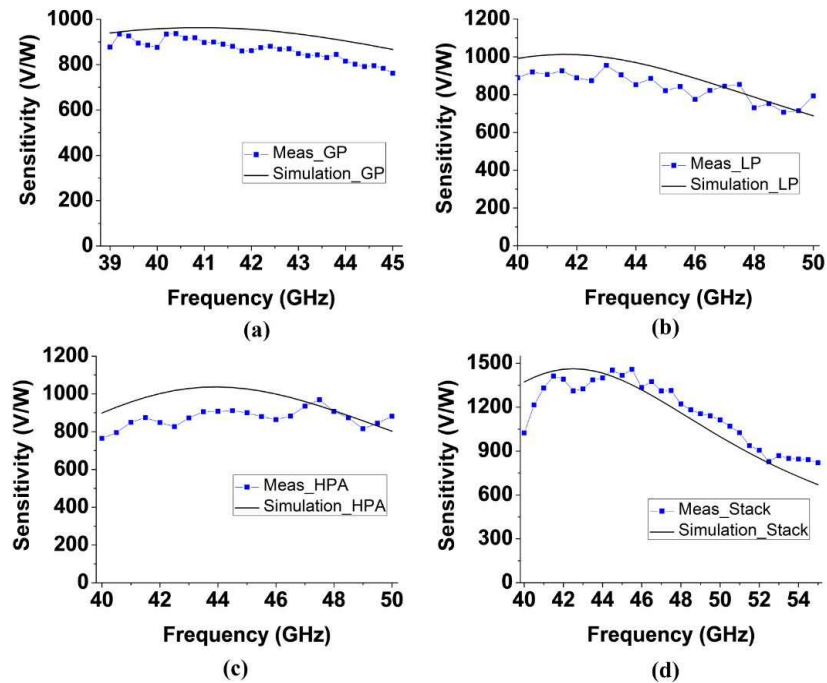


Figure 5. The measured and simulated voltage sensitivity curves vs frequency at $P_{in} = -30$ dBm.

Fig. 6 shows the measured and simulated sensitivity curves versus input power at 44 GHz. The compression point P_{in_max} is defined as the input power level for which the sensitivity value is degraded by 10% compared to its value in the linear zone.

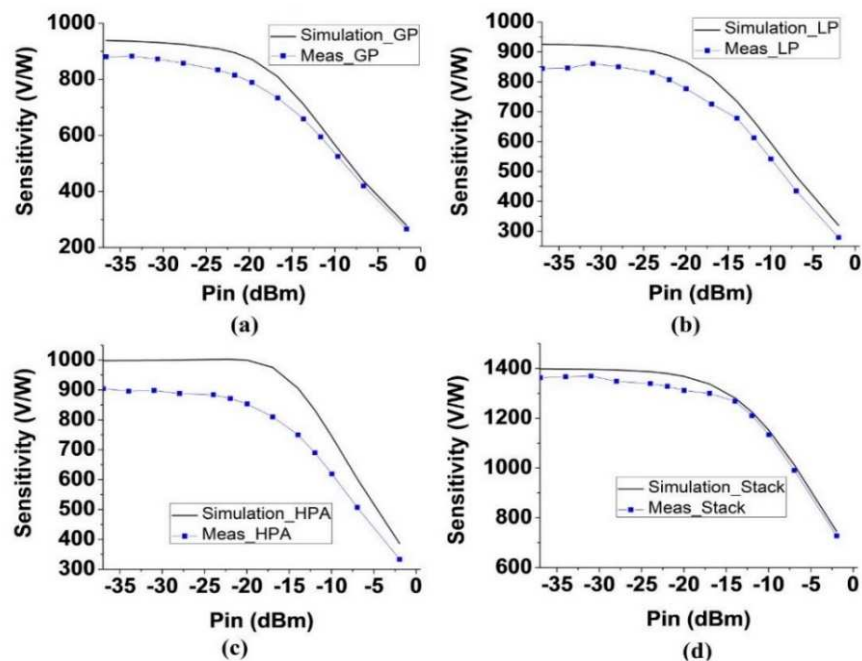


Figure 6. The measured and simulated voltage sensitivity curves vs input power at 44 GHz.

Based on the obtained results, it can be concluded that: (i) The P_{in_max} occur at (-20, -20, -17, -12) dBm corresponding to the GP, LP, HPA and LP Stack detectors respectively. (ii) The LP Stack detector exhibits higher level of P_{in_max} as expected.

In order to determine the dynamic range of the detectors (DR), extracting the value of the minimum detectable power (P_{in_min}) is required. The noise equivalent power (NEP) term is usually used to determine the P_{in_min} . The NEP value represents the detector noise floor normalized to 1 Hz of video bandwidth and is given in the following equation [8]:

$$NEP = \frac{V_{noise}}{\gamma} \quad (W/\sqrt{Hz}) \quad (2)$$

Hence
$$P_{in_min} = NEP \times \sqrt{BW} \quad (W) \quad (3)$$

Where BW is the video bandwidth, V_{noise} is the output noise voltage spectral density at low frequencies (in the video bandwidth). In the case of continuous RF wave CW (as the case of this work), the NEP value is equal to P_{in_min} value. Since the NMOSs are used in zero bias condition, the thermal noise is considered as the only source of noise generated by the video equivalent resistance R_V . In order to extract the R_V value, the voltage V_{ON} is measured (at $P_{in} = -30$ dBm) for loaded and unloaded detector. The DC equivalent circuit of the loaded detector is shown in figure 7.

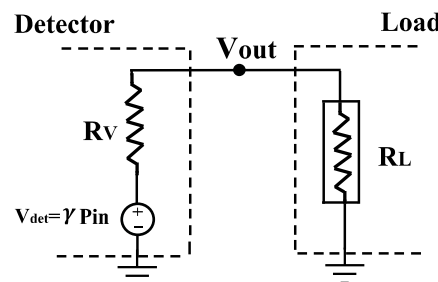


Figure 7. The DC equivalent circuit of detector loaded by resistance R_L .

The output voltage $V_{unloaded}$ is equal to V_{det} for the unloaded detector. When the detector is loaded by a resistor R_L , the output voltage V_{loaded} is given as in the following:

$$V_{loaded} = V_{unloaded} \frac{R_L}{R_L + R_V} \quad (4)$$

Based on the equation (4), the value of the video resistance can be extracted as the following:

$$R_V = R_L \left(\frac{V_{unloaded}}{V_{loaded}} - 1 \right) \quad (5)$$

The noise voltage can be calculated using the equation 6, and then the NEP value is calculated using equation 2.

$$V_{noise} = \sqrt{4KTR_V} \quad (V/\sqrt{Hz}) \quad (6)$$

Where K is the Boltzmann constant, T is the absolute temperature in kelvin. It is worth to mention that, higher sensitivity values can be obtained by decreasing the value of R_{att} or using smaller transistors sizes. However, the P_{in_max} will be decreased, and so, smaller dynamic range will be obtained. In order to make the comparison between the detectors performances, a figure of merit FOM is proposed taking into account the sensitivity and dynamic range:

$$FOM = DR \times \gamma \times 1E-7 = \frac{P_{in_max}}{P_{in_min}} \times \gamma \times 1E-7 \quad (V/W) \quad (7)$$

In equation (7), P_{in_max} and P_{in_min} are in Watt, the factor 1E-7 makes the FOM values in appropriate scale.

Table 1 summarizes the extracted parameters of the detectors, where several conclusions can be mentioned: (i) The HPA detector has the lowest value of NEP, and so P_{in_min} . In addition, it provides the largest dynamic range and the best performance as compared to other detectors. (ii) The LP Stack detector provides the highest P_{in_max} value, hence it can be used at higher levels of RF power. (iii) Using stack of N transistors (instead of single transistor) can enhance the detector performance as the case of LP and LP Stack detectors. (iv) A better detector performance is expected to be obtained by stacking HPA instead of LP transistors.

Detector	R_V (k Ω)	P_{in_min} @ CW (dBm)	NEP (pW/ \sqrt{Hz})	P_{in_max} (dBm)	DR (dB)	γ (V/W)	FOM (V/W)
GP	85	-74	42	-20	54	880	22.5
LP	4500	-65	322	-20	45	850	2.7
HPA	0.8	-84	3.8	-17	67	900	473
LP Stack	27000	-63	485	-12	51	1380	18

Table 1. The summary of the extracted detectors parameters at 44 GHz.

In the HPA detector, the total input power is absorbed in the transistor, therefore it exhibits higher performance compared to GP and LP detectors (where part of input power is absorbed in the R_{att} resistor).

Table 2 presents the comparison with other recent works. The HPA detector shows a very good performance by exhibiting very low NEP value (3.8 pW/ \sqrt{Hz}) and large dynamic range (67 dB). This performance is very interesting, where such large dynamic range is necessary to maintain the linear responses in the modern modulations, since their signals have high peak to

Ref.	Technology	Frequency (GHz)	NEP (pW/ \sqrt{Hz})	P_{in_min} (dBm)	DR (dB)	γ (V/W)
[9]	Glass substrate	40 – 75	-	-50	>50	15 (at 60 GHz)
[10]	Custom MMIC	DC – 70	-	-65	>60	121 (at 50 GHz)
[11]	Alumina 5 mil	57 – 65	-	-48	42	8250 (at 61 GHz)
[12]	GaAs/AlAs	15 - 35	20	-	-	1300 (at 24 GHz)
[13]	Commercial Schottky diode	2 – 18	5	-	-	2000 (at 18 GHz)
[14]	InGaAs (Schottky diode)	87.8	0.39	-	-	16005 (at 87.8 GHz)
This work (at 44 GHz)	55-nm BiCMOS	38 – 48 (GP) 40 – 50 (LP) 42 – 50 (HPA) 42 – 55 (LP Stack)	42 322 3.8 485	-74 -65 -84 -63	54 45 67 51	880 850 900 1380

Table 2. Comparison with other published power detectors.

average power ratios (PAPR).

4. Conclusion

The synthesis and characterization of four ZBDs were presented. Each detector is based on different category of MOSFET transistor, integrated in SiGe 55-nm BiCMOS technology from ST-Microelectronics. Compared to other recent works, the HPA detector exhibits a very good performance with very low NEP value and large dynamic range. It was also shown that the stack topology helps increasing the dynamic range. Since the HPA transistor exhibits better performance than the LP, realizing a detector based on stack of HPA transistors is planned as future work.

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