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# GaN Schottky diode on sapphire substrate for THz frequency multiplier applications

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## Abstract

Gallium Nitride, because of its high breakdown field, and peak and saturated electron drift velocity, high chemical stability and high thermal conductivity, is a very promising material as candidate for Schottky varactor diodes for next-generation high-power frequency multipliers. Similarly to the huge interest in the field of HEMT for high frequency and power application, GaN Schottky diodes is of a high interest for the next technological step for frequency multipliers for THz generations, replacing GaAs Schottky diodes. Due to a lack of research focused on GaN Schottky diodes for frequency multiplication, the design and fabrication of GaN frequency multipliers remains a technological challenge. In this paper, we present GaN Schottky diodes fabricated on a heteroepitaxial GaN on sapphire. The barrier height obtained is around 0.53 eV, and it increases up to 0.73 eV after Schottky contact annealing; and the ideality factor is equal to 1.1 before annealing and 1.2 after annealing. The resulting series resistance is very low, 7Ω and 1Ω, before and after annealing, respectively.

Keywords: GaN, Schottky diode, frequency multiplier, THz

## 1. Introduction

In the field of THz frequency generation, the only technology that has proven its potentials relies on the frequency multiplier principle [1]. A GaAs-based frequency multiplier chain delivers state of the art performance with an output power of 18 μW obtained at 2.58 THz [2] and about 1 mW at 1 THz [3]. However, due to the technological limitations of GaAs (intrinsic electric field breakdown limitation and low thermal conductivity), this impressive technology cannot yet reach the requirements for mass-market applications. Gallium Nitride (GaN) was proposed as candidate to substitute GaAs, due to its higher breakdown electric field combined with its high thermal conductivity [4]. These two advantages are expected to yield a power handling capability of a GaN Schottky diode almost one order of magnitude larger than its GaAs counterpart [5].

Though great progress has been made in the last two decades [6–8], obtaining high frequency performances from a vertical device such as a GaN Schottky diodes remains still a great technological challenge [1]; the reason to this may be attributed to the technological difficulties of obtaining defect-free crystalline GaN and to the lack of basic research oriented toward the optimization of GaN Schottky diodes for frequency multiplier circuits.

In this article, we report a quasi-vertical GaN Schottky diode with low series resistance and high breakdown voltage, as well as its electrical characterization.

## 2. Material and device fabrication

The GaN epitaxial layers used in this study (Figure 1) were grown by MOCVD on c-plane sapphire substrate. Given that the optimization of the process is characterized by a high consumption of material, it has been decided to first develop the process with a "low-cost" substrate such as Sapphire. With respect to the application, silicon carbide (SiC) substrate is the substrate of choice for thermal management. Therefore, after the present process development on Sapphire is completed, it is planned to transpose these works on SiC substrate. A 2  $\mu\text{m}$  unintentionally doped GaN was grown first then 1.1  $\mu\text{m}$  thick  $\text{n}^+$  GaN layer highly doped at  $1 \times 10^{19} \cdot \text{cm}^{-3}$  was grown to achieve low specific contact resistance and low series resistance and a 650 nm  $\text{n}^-$  GaN ( $5 \times 10^{16} \cdot \text{cm}^{-3}$ ) acted as active layer. All the lithographic steps in the process were performed through e-beam lithography.

After laser cutting, the sample was thoroughly cleaned with IPA and acetone and ultra-sonication. Then, a  $\text{SiO}_2$  layer was deposited on the GaN surface in order to be used as a hard mask for mesa etch.  $\text{SiO}_2$  is patterned using negative resist; after developing, the mask was transferred to the  $\text{SiO}_2$  layer by  $\text{SF}_6$  dry etch. The remaining resist was subsequently removed by  $\text{O}_2$  plasma. Next, using  $\text{Cl}_2$ -based ICP dry etching, the diode mesa was defined up to the  $\text{n}^+$  GaN layer with a total etch of 750 nm. The ohmic metallization is deposited 100 nm inside of the  $\text{n}^+$  GaN layer doped at  $1 \times 10^{19} \cdot \text{cm}^{-3}$  in order



Figure 1. Schematic view of GaN epitaxy used in this study

to ensure a low specific contact resistance.

The ohmic contact was then fabricated with standard lift-off technique. Before metallization, the sample was treated with an HF solution to remove oxidation and contaminants. Then, a multilayer of Ti/Al/Ni/Au was evaporated onto the sample and lifted-off. Afterwards, the sample was annealed with a rapid thermal annealing (RTA) at 850°C.

Before Schottky contact definition, the remaining  $\text{SiO}_2$  was removed and the interested semiconductor surface was treated with BOE solution and plasma etching. Then, a Pt/Au contact was deposited through e-beam evaporation.

This process allows the fabrication of planar Schottky diodes with diameters ranging from 1400 down to 44  $\mu\text{m}$ .

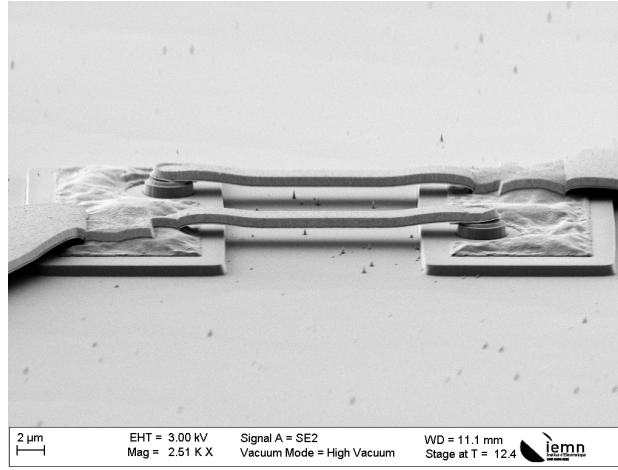


Figure 2. Sub-micronic anti-parallel diodes

Quasi – vertical submicronic diodes are being fabricated under the same process flow layout: after Schottky contact deposition, negative resist is used to define the isolation patterns. After developing, the sample is dry etched ( $\text{Cl}_2$ -based plasma) with about  $1 \mu\text{m}$  down to the undoped GaN layer, resulting in an isolation of the diodes. Subsequently, vias are opened to deposit metal pads. The last step consists in the realization of the air-bridge (Ti/Au, 200/600 nm) that will connect the Schottky and ohmic contacts to their respective metal pads. The choice of the air-bridge is fundamental because this approach allows to minimize parasitic resistances and capacitances.

Two different samples were fabricated and characterized: sample A, with Schottky contact “as deposited”, i.e., with no thermal annealing performed, and sample B, with annealing of the Schottky contact at  $400^\circ\text{C}$  for 5 minutes. On both samples, three diodes with different diameter were characterized (140, 70 and  $44.28 \mu\text{m}$ ).

### 3. Results and discussion

#### 3.1 C-V Characteristics

The capacitance of a metal-semiconductor junction as a function of voltage is described by

$$\frac{A^2}{C^2} = \frac{2 \cdot \left( V_{bi} - V - \frac{k_B T}{q} \right)}{q \cdot \epsilon_s \cdot \epsilon_0 \cdot N_d}$$

where  $A$  is the contact area,  $V_{bi}$  is the built-in voltage,  $V$  is the applied voltage,  $N_d$  is the donor concentration,  $\epsilon_s$  is the dielectric constant of the semiconductor and  $k_B$ ,  $T$ ,  $\epsilon_0$  and  $q$  are Boltzmann constant, the temperature, the dielectric vacuum constant, and the elementary charge, respectively.

A plot of  $C^{-2}$  vs  $V$  should yield a straight line and the carrier concentration can be extracted from its slope. From intercept on the x-axis we can extrapolate the barrier height by:

$$\phi_B = V_x + \frac{k_B T}{q} + \frac{k_B T}{q} \ln \left( \frac{N_c}{N_d} \right)$$

where  $V_x$  is the x-axis intercept, and  $N_c$  is the density of states in the conduction band edge.

The  $C^{-2}$  vs  $V$  plot for both samples can be seen in Figure 3.

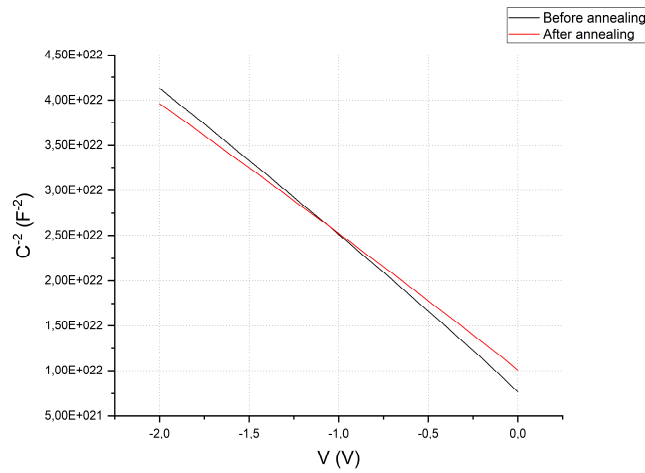


Figure 3.  $C^{-2}$  vs  $V$  plot of a  $140\mu\text{m}$  diameter diode for both samples measured at 1MHz

From our measurements, the barrier height and doping concentration were calculated to be, respectively,  $0.67\text{eV}$  and  $4.15 \cdot 10^{16}\text{cm}^{-3}$  for sample A and  $0.78\text{eV}$  and  $4.42 \cdot 10^{16}\text{cm}^{-3}$  for sample B. The doping density is close to the initial value for both samples, with minor differences that can be attributed to the annealing of the Schottky contact (i.e., better interface conditions). The barrier height is, in both cases, slightly higher than the value extrapolated from DC measurements. This difference originates from the fact that DC measurements are affected by non-idealities effects such as image force lowering, which in turn have little if not zero effect on C-V measurements. In practice, the capacitance-voltage method yields what is called the flatband barrier height, whereas the current-voltage method yields the zero-bias barrier height. In general, the flatband barrier height is a better measure of the barrier height than the zero-bias barrier height

The capacitance-voltage measurements were carried out at 1 MHz in order to avoid interface states and traps contribution to the measurement [9]. When a small voltage is applied to a Schottky diode, various defect energy levels sweep through the quasi-Fermi level, which produce an oscillation in the charge density. If the frequency is higher than the level response time, it cannot respond.

The frequency dependent capacitance measurements are showed in Figure 4.

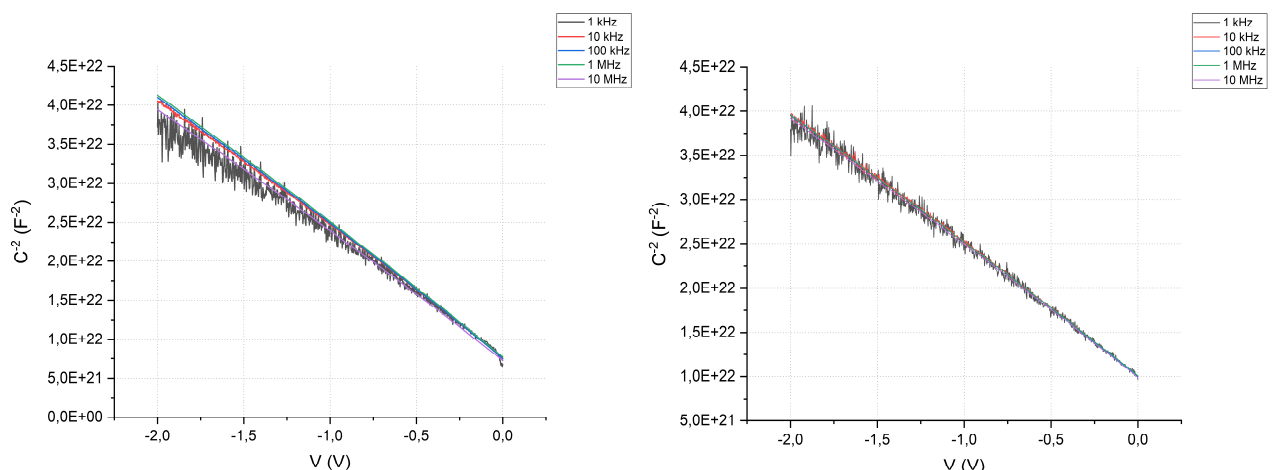


Figure 2. Frequency-dependent capacitance for sample A (left) and sample B (right)

The capacitance measured at virtually all frequencies is the same, meaning that our sample is characterized by a low concentration of trap states, as opposed to some example in the literature [10,11].

A small deviation is observed at 1 kHz, supposedly because at that frequency, the time constant of the ac signal is low enough for the traps to follow.

### 3.2 DC Characteristics

The current-voltage characteristics of the Schottky diode were studied at room temperature, in order to extract first-order parameters to validate the technological process and, in a second time, low and high temperature DC characterization was carried out. The I-V characteristics at room T are shown in Figure 5.

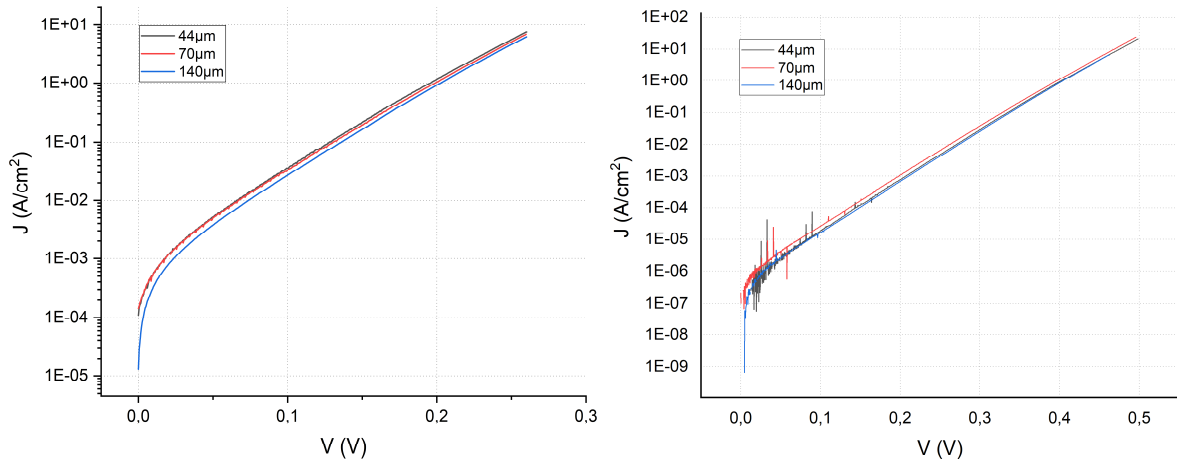


Figure 3. Forward characteristics of measured diodes of sample A (left) and sample B (right)

It is clear from the plot in Figure 5 that both diodes are affected by leakage current at lower voltages. This leakage can be attributed to defect states in the bulk and/or the surface. One of the main technological limitations in GaN electronic devices stems from the epitaxy: since the semiconductor is not lattice matched to the substrate, the material suffers from defect and dislocations that greatly affect its electronic properties [12–16]. Moreover, most Schottky diodes suffer from the presence of a thin insulating layer at the metal-semiconductor interface due to unwanted oxidation and/or contamination, unless it is fabricated in vacuum; in the case of I-V measurements, a thin interfacial layer of a few angstrom can be a major cause of deviation of the electrical diode characteristics from their ideal behavior [9,17]. An annealing of the Schottky contact improves the characteristic, namely by reducing the leakage current [17].

The classic diode model for thermionic emission is given by following equation [18]:

$$I = I_0 \left[ \exp\left(\frac{qV}{nk_B T}\right) - 1 \right] \quad (1)$$

where  $I_0$  is the saturation current, and  $n$  is the ideality factor. The saturation current is (under the assumption that the series resistance of the diode is negligibly small):

$$I_0 = A^* T^2 \exp\left[\frac{-q\phi_b}{nk_B T}\right] \quad (2)$$

where  $A^*$  is the Richardson constant and  $\phi_b$  the barrier height of the diode.

By performing a fit of the linear part of the semi-logarithmic I-V plot, we are able to extract the barrier height and the ideality factor, which for  $T = 300K$  corresponds to  $0.64 eV$  and  $1.16$ , respectively. This value of the ideality factor reflects good agreement with thermionic emission

theory, proving in a first moment, that this is the main conduction mechanism for the diode at that temperature.

The values of the barrier height and ideality factor extracted with this method were compared to the one extracted using Cheung's method [19]:

$$V = R_S A J + n \phi_B + \frac{n}{\beta} \ln \left( \frac{J}{A^* T^2} \right) \quad (3)$$

$$\frac{dV}{d(\ln(J))} = R_S A J + \frac{n}{\beta} \quad (4)$$

where  $n$  is the ideality factor,  $\phi_B$  is the barrier height,  $R_S$  is the series resistance,  $A$  is the electrically active area,  $A^*$  is Richardson constant ( $24.6 \text{ A cm}^{-2} \text{ K}^{-2}$  for GaN) and  $\beta = \left( \frac{k_B T}{q} \right)^{-1}$ .

A plot of  $dV/d(\ln(J))$  vs  $J$  yields a straight line whose slope and intercept with the  $y$ -axis are  $R_S A$  and  $n/\beta$ .

Using an auxiliary function  $H(J)$ , it is possible to evaluate  $\phi_B$  and the series resistance:

$$H(J) = V - \frac{n}{\beta} \ln \left( \frac{J}{A^* T^2} \right) \quad (5)$$

$$H(J) = R_S A J + n \phi_B \quad (6)$$

Using the  $n$  value determined from Eq. 5, a plot of  $H(J)$  vs  $J$  leads to a straight line, with slope  $R_S A$  and intercept with the  $y$ -axis  $n \phi_B$ . The slope of this curve allows a second evaluation of the series resistance that can be used as a consistency check of the approximation with its first value.

The results for both samples are listed in Table 1.

	TE fit [18]		Cheung [19]		
	$\phi_B$ (eV)	$n$	$\phi_B$ (eV)	$n$	$R_S$ ( $\Omega$ )
(A) 44.28	0.54	1.21	0.53	1.28	7.02
(A) 70	0.55	1.18	0.54	1.19	7.91
(A) 140	0.56	1.09	0.56	1.13	5.88
(B) 44.28	0.73	1.16	0.71	1.23	3.08
(B) 70	0.72	1.15	0.72	1.18	3.05
(B) 140	0.75	1.09	0.73	1.16	0.90

Table 1. Extracted valued of barrier height and ideality factor for both samples

The ideality factor for both samples is between 1.1 and 1.2, which confirms that the main electrical conduction mechanism is thermionic emission (an ideality factor of 1 indicates pure thermionic emission in the ideal case), although there is the presence of other, non-ideal, mechanisms, such as tunneling. The barrier height undergoes an improvement with annealing (sample B), by increasing of about 0.20 eV, an improvement due to the fact that the thermal treatment allowed a structural rearrangement of Pt and Ga at the metal/semiconductor interface [20], which possibly eliminated any eventually native oxides present on the semiconductor surface and/or surface roughness induced during the fabrication process [17]. Moreover, the thermal annealing is not detrimental to the ideality factor. The series resistance, as calculated with Cheung's method, is of about 7  $\Omega$  for sample A and between 1 and 3  $\Omega$  for sample B. This reduction in series resistance proves that thermal

annealing of the Schottky contact was effective in promoting a structural reorganization at the metal/semiconductor interface, reordering the lattice structure in its most stable configuration [17].

TLM measurements of the Ohmic contact yielded a contact resistance of  $0.27 \Omega \cdot mm$ , a specific contact resistivity of  $4.3 \cdot 10^{-6} \Omega \cdot cm^2$ , as well as a sheet resistance of  $169.7 \Omega/sq$  for the  $n^+$  GaN layer.

Table 2 presents a comparison of the barrier height and ideality factor for the samples analyzed in this paper with a few of the literature references found on GaN Schottky diodes grown on sapphire substrate.

Epitaxy thickness	$N_d$	$\phi_B$ (eV)	$n$	$R_S$ ( $\Omega$ )	Reference
650 nm (Sample A)	$5 \times 10^{16}$	0.53 – 0.56	1.13 – 1.28	5.8 - 7	This work
650 nm (Sample B)		0.71 – 0.73	1.16 – 1.23	1 - 3	
100-400 $\mu m$	$6.6 \times 10^{16}$	0.84 – 0.94	1.03	NA	[21]
3 $\mu m$	$1 \times 10^{16}$	0.79 – 0.96	1.16 – 1.8	NA	[22]
4 $\mu m$	$1 \times 10^{17}$	0.845	1.18	65	[23]
150 nm	$5-7 \times 10^{16}$	1.10	1.05	120	[24]

Table 2. Comparison of parameters for various GaN Schottky diodes

The lower barrier height of the samples presented in this work as compared to the examples found in the literature (Table 2) can have complex origins, such as the presence of contaminants at the metal-semiconductor interface, or a high density of dislocation defects [15]. Moreover, the barrier height extracted from DC measurements is also affected by image-force lowering and other types of barrier inhomogeneities such as the presence of a thin oxide layer at the metal/semiconductor interface, tunneling currents, generation/recombination currents within the space-charge region [25].

The series resistance, in turn, result to be very low (about  $6 \Omega$  for sample A and between 1 and  $3 \Omega$  for sample B) when compared to the literature [23,24]. This result in particular acquires a new light when thinking that the series resistance of GaN Schottky diodes, which is typically higher than its GaAs counterpart, is a key parameter in the design of GaN Schottky diode frequency multipliers [5,26].

Figure 6 shows the reverse characteristics of the measured diodes, before and after thermal annealing. The breakdown voltage at  $10\mu A$  was measured to be  $-22.4 V$  before annealing, and  $-36 V$  after annealing. The breakdown voltage at the destruction for the diodes before annealing resulted to be between  $60-70 V$ , while the diodes that underwent annealing yielded an improved breakdown voltage between  $75-80 V$ .

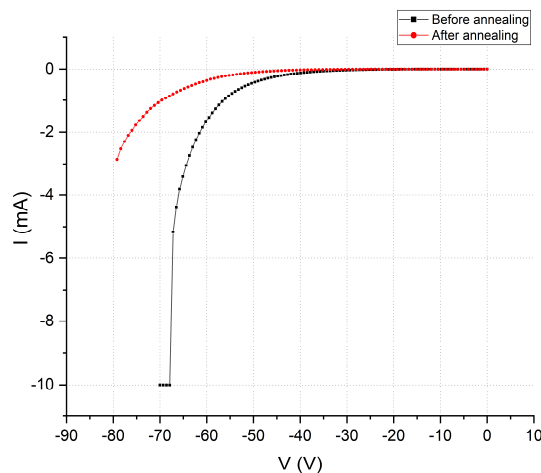


Figure 6. Reverse characteristics of a  $70 \mu m$  diode before and after annealing



The annealed sample shows a reduction in reverse leakage current, which, along with the increased barrier height, can be attributed to a reduction of nonstoichiometric defects in the metal-semiconductor interface [27].

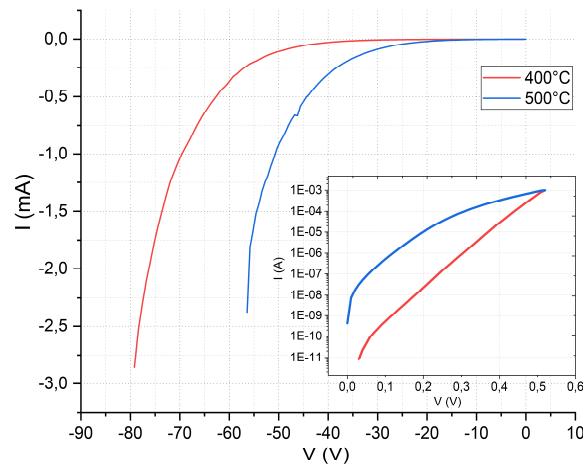


Figure 7. Comparison of different thermal annealings for a 70  $\mu\text{m}$  diode. Inset: forward characteristics

An annealing at 500°C was performed as well (Figure 7): the resulting breakdown voltage was of about -56.4V (as opposed to the corresponding breakdown voltage for the sample annealed at 400°C, which was of about -79.2V). This degradation of the characteristic can be attributed to the formation of intermetallic compounds and to the migration of nitrogen gas to the surface [28]. In the literature is typically reported that Pt degrades as a Schottky contact to GaN in a range of temperatures between 600°C and 800°C, with a fairly dependence on the annealing time [17,28–30].

#### 4. Conclusions

In conclusion, GaN Schottky diodes on sapphire substrate were fabricated in the general optics of realizing varactor-based frequency multipliers for THz generations. Thus, an experimental investigation of the diodes basic parameters was conducted. Two samples (sample A, with no surface treatment and no annealing, and sample B, with no surface treatment and annealing at 400°C for 5 minutes) were studied and analyzed.

The capacitance-voltage characteristics were studied to identify the role of traps and contaminants to the overall performance of the diodes. The extracted barrier height and effective doping density from 1 MHz measurements are 0.67 eV and  $4.15 \cdot 10^{16} \text{cm}^{-3}$  for sample A and 0.78 eV and  $4.42 \cdot 10^{16} \text{cm}^{-3}$  for sample B.

The current-voltage characteristics were studied to extract first order parameters such as the barrier heights, ideality factors and series resistances. The ideality factor for both samples is between 1.1 and 1.2. The barrier height is around 0.55 eV, a value that increase up to 0.72 eV when the diodes undergo annealing at 400°C. The series resistance is of about 7  $\Omega$  for sample A and between 1 and 3  $\Omega$  for sample B; this last result in particular is promising in the optics of GaN Schottky diode frequency multipliers design and realization, since the series resistances obtained in this work are considerably small compared to the literature. The two samples presented a breakdown voltage of about -56.4 V and -79.2 V, respectively for sample A and sample B.

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