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### ► To cite this version:

Florent Albany, François Lecourt, Ewa Walasiak, N. Defrance, Arnaud Curutchet, et al.. Stability of the threshold voltage in fluorine-implanted normally-off AlN/GaN HEMTs co-integrated with commercial normally-on GaN HEMT technology. *Microelectronics Reliability*, 2021, 126, pp.114291. 10.1016/j.microrel.2021.114291 . hal-03539673

**HAL Id: hal-03539673**

**<https://hal.science/hal-03539673>**

Submitted on 25 May 2023

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# Stability of the threshold voltage in fluorine-implanted normally-off AlN/GaN HEMTs co-integrated with commercial normally-on GaN HEMT technology

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## Abstract

Fluorine ion migration in normally-off AlN/GaN HEMTs fabricated by fluorine ion plasma implantation technology is evidenced. Devices under test are co-integrated into the OMMIC commercial D006GH/D01GH MMIC process, providing fluorine-free normally-on HEMTs. Gate reverse bias step-stress experiment at a drain fixed voltage of 0 V, carried out as well on normally-on ones as on normally-off ones, shows a permanent negative shift in the threshold voltage  $V_{th}$  of normally-off devices only.  $V_{th}$  degradation is starting at a  $V_{GS, stress}$  of -8 V, with a negative shift from 0 V to -0.4 V at  $V_{GS, stress} = -30$  V, while the transconductance  $g_m$  and  $g_{m, max}$  remains unchanged prior to breakdown that occurred at  $V_{GS, stress}$  ranging between -26 to -32 V. Since the positive threshold voltage of these devices is induced by F-ions dose and position, the above result suggests a possible drift of F-ions away from the 2DEG channel. A field-assisted migration mechanism of fluorine ions is proposed and supported by the absence of  $V_{th}$  degradation in fluorine-free normally-on devices.

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## 1. Introduction

In the context of the rapid expansion of wireless communications and the emergence of electric vehicles, the increasing demand for more efficient, compact and cheaper devices that can provide higher wideband performances with higher power density, current Si and GaAs based technologies have reached their limits and are no longer able to satisfy market needs. Thanks to GaN outstanding material properties, such as a high critical electric field, high robustness, and high frequency performances, GaN-based HEMTs are considered as the best candidates for the next-generation RF power applications. Meeting the stringent specifications of 5G, GaN multi-functional MMICs have already successfully replaced discrete Si and GaAs circuits in base stations with considerable gains in terms of

circuit density and performances. However, despite the high performances provided, the standard GaN HEMT is normally-on type (in conduction mode at  $V_{GS} = 0$  V) due to the strong spontaneous and piezoelectric polarizations of the material. The lack of GaN technologies that monolithically co-integrate normally-on and normally-off devices is a considerable disadvantage for many applications. As a consequence, current GaN MMICs are exclusively composed of normally-on devices. Since they are not very suitable for digital circuits in reason of the inherent power consumption in quiescent state, conventional Si or GaAs digital control circuits are used, in order to drive GaN high performance power circuits. The co-integration of normally-off and normally-on GaN HEMTs onto the same chip will ultimately allow the replacement of current Si and GaAs technologies, with several benefits in terms of

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efficiency, reliability, integration and circuit simplicity. Normally-off devices will be mainly used in low voltage digital control circuits where no power and high frequency performances is needed (i.e. low  $L_G$  and  $L_{G-S}$ ), while normally-on devices will be used in high frequency power circuits.

The fabrication of co-integrated normally-off devices is still a challenging task as epitaxial structures are usually optimised to enable either operation mode (normally-off or normally-on). The fluorine ion implantation technique used in the devices under test is a promising approach for the fabrication of normally-off GaN HEMTs [1–3]. The unique additional F-ions implantation step required to convert a standard normally-on GaN HEMT to a normally-off one makes this approach particularly attractive for the industry. Unlike conventional published approaches where F-ions are implanted within the barrier layer below the gate, F-ions were here implanted under the 2DEG channel, below the gate region [4,5]. By acting as fixed negative charges, F-ions allow to deplete the overlying 2DEG channel, resulting in a positive shift of the threshold voltage till positive values. Threshold voltage is driven by implantation profile such that the closer F-ions are to the 2DEG channel (and the higher the dose), the higher the threshold voltage is.

In this paper, a reverse gate bias step-stress experiment was performed on both normally-on and normally-off devices in order to evidence fluorine ions drift induced by large vertical electric field and to establish their safe operating area (SOA).

## 2. Description of device and stress procedure

### 2.1. Technology and performances

Fluoride-treated normally-off AlN/GaN HEMTs were co-integrated into the OMMIC commercial D006GH/D01GH (Depletion-mode 60/100 nm GaN HEMT) MMIC processes [6,7]. Processed on GaN/HR-Si substrate, the D006GH/D01GH technologies have been optimized to meet the requirements of millimeter and microwave applications by providing normally-on GaN HEMTs featuring  $L_G = 60$  nm and 100 nm mushroom-shaped gate and in-situ re-growth of ohmic contacts with  $R_C$  contact resistance as low as  $0.06 \Omega\cdot\text{mm}$ . Optimized MOCVD growth of the hetero-structure combined with in-situ growth of SiN protecting layer, were used to reduce memory and fast trap effects. Ultra-thin AlN barrier layer (4 nm) and AlGaIn back-barrier were used to reduce short channel parasitic effects while increasing transconductance and power density. Normally-off HEMTs are co-integrated with nearly

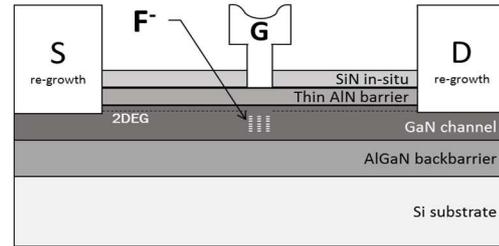


Fig. 1. Schematic cross-section of the normally-off GaN HEMT co-integrated in D006GH/D01GH technologies. F-ions were implanted under the 2DEG channel in the gate region

identical processes as for D006GH/D01GH technologies. Fluorine ion implantation, performed within GaN buffer layer (under the gate) and before gate metal deposition, allows to deplete the overlying 2DEG channel and shifts the threshold voltage to positive values. Additional masking and e-beam lithography steps are added to preserve the fluorine-free normally-on devices performances. A schematic cross-section of the normally-off HEMT structure is shown in Fig. 1. Devices under test feature two gate fingers with  $2 \times 25 \mu\text{m}$  gate width and gate lengths  $L_G$  of 300 nm and 60 nm, respectively for the low frequency normally-off HEMT and for the high frequency normally-on HEMT.

The devices under test are issued from the very first R&D GaN co-integrated OMMIC technology, previously presented in [8,9]. By optimizing the implantation process, a truly positive threshold voltage  $V_{th} = +350$  mV (versus  $-1.4$  V for normally-on devices) was achieved without impacting other parameters. Normally-off HEMTs provide a high current density  $I_{DS,max}$  of  $1 \text{ A}\cdot\text{mm}^{-1}$  (respectively over  $1.5 \text{ A}\cdot\text{mm}^{-1}$  for normally-on ones) and a very good uniformity of the characteristics on the wafer. Thanks to OMMIC's patented ohmic contact re-growth technology (which provides a very low  $R_C$ ) and to the strong piezoelectric polarization (and small thickness) of the AlN barrier layer, a very high extrinsic peak transconductance  $g_{m,max}$  of  $590 \text{ mS}\cdot\text{mm}^{-1}$  (respectively  $1090 \text{ mS}\cdot\text{mm}^{-1}$  for normally-on ones) at  $V_{DS} = 4$  V is achieved. As  $g_{m,max}$  is depending on  $R_S$  source access resistance, the differing in  $g_{m,max}$  can mainly be attributed to the differing in device gate-to-source spacing  $L_{G-S}$ , which is 600 nm in the normally-off device vs. only 250 nm in the normally-on one.

### 2.2. Gate reverse bias step-stress sequence

In order to assess F-ions stability in the hetero-structure, gate reverse bias step-stress experiment was performed at  $23^\circ\text{C}$  room temperature

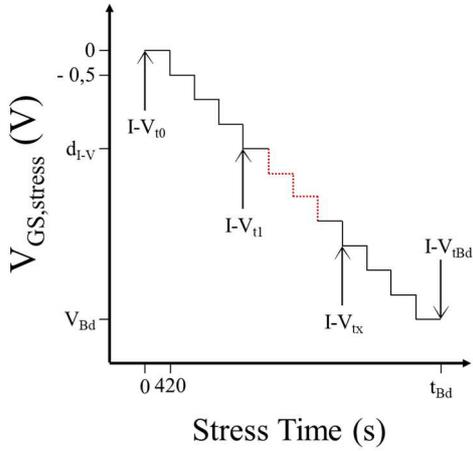


Fig. 2. Illustration of the step-stress sequence using stepped negative gate bias at  $V_{DS} = 0$  V. I-V interim measurements are performed every -5 V or -2 V  $d_{I-V}$  intervals till breakdown.

as well on normally-on as on normally-off devices. In this experiment,  $V_{GS}$  is decreased from 0 V to breakdown in steps of -0.5 V every 420 s at a drain fixed-bias  $V_{DS} = 0$  V. The focus is here made on the effects of the vertical electric field on F-ions. Combined with in-situ continuous monitoring of gate and drain currents, in-situ I-V interim measurements were inserted every  $d_{I-V} = -5$  V or -2 V to accurately monitor the evolution of transistors characteristics. This step-stress sequence is illustrated in Fig. 2. Measurements were carried out on a specifically developed on wafer measurement bench, taking advantage of a HP4142 modular static source analyser to perform all required test (drain and gate polarization, currents monitoring versus time, I-V) with a suitable resolution (within the pA range). This bench is described in [9]. Input, output and transfer I-V characteristics are performed with a 4 ms acquisition time and a 25 mV voltage sampling. Although I-V measurements have been configured to not degrade the under-test devices, transitions between characterization and ageing phases can be the source of large current transients. As they can be destructive for transistors, pre-biasing sequences were added before and after each I-V interim measurements to ensure soft transitions between stressing steps and I-V interim measurements. They consist in 2 s brief 500 mV increments, from previous stress step bias to 0 V before I-V interim measurement, and from 0 V to subsequent stress step bias after I-V interim measurement.

### 3. Results and discussion

Fig. 3 shows the  $I_{GS}$  gate current response to the

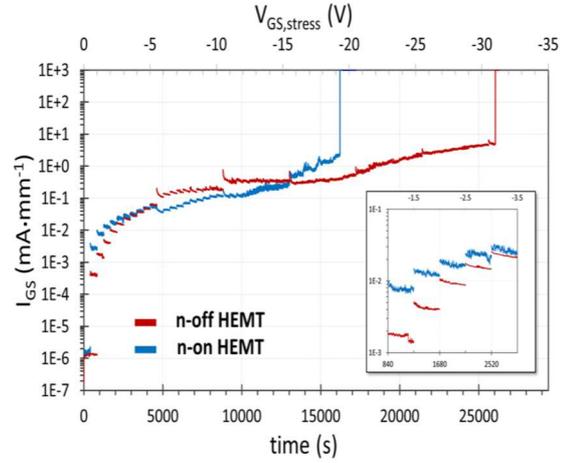


Fig. 3. Gate current monitoring during the gate reverse bias step-stress sequence at  $V_{DS} = 0$  V.  $V_{GS}$  is stepped by -0.5 V from 0 V to devices breakdown.

applied  $V_{GS, stress}$  (and stressing-time, highlighted in the inset of Fig. 3) for representative normally-off and normally-on devices during the complete gate reverse bias step-stress experiment. Both transistors were biased in off-conditions at a drain fixed-bias  $V_{DS} = 0$  V, with few hot electrons generated in order to assess the response of F-ions to vertical electric field stress applied across the GaN channel. Gate current density  $I_{GS}$  is still below  $10 \text{ mA}\cdot\text{mm}^{-1}$  and differ by more than 5 orders of magnitude for  $V_{GS}$  varying from 0 V to breakdown voltages  $V_{Bd}$ , which occurred at -31 V for the normally-off device and -19 V for the normally-on one. The difference in breakdown voltage can be associated with the differing in device gate lengths  $L_G$ , which is 300 nm in the normally-off device vs. only 60 nm in the normally-on one, and with the differing in device gate-to-source spacing  $L_{G-S}$  (respectively 600 nm vs. 250nm). However, as fluorine ions are negatively charged particles, we can assume that they can affect the built-in electric field which, in turn, contribute to the breakdown of the normally-off device as the electric field at breakdown is lower than in the normally-on one ( $E_{Bd, off} = 52 \text{ V}\cdot\mu\text{m}^{-1}$  vs.  $E_{Bd, on} = 76 \text{ V}\cdot\mu\text{m}^{-1}$ ). Further measurements involving several fluorine implantation profiles are still required to support this assumption. The associated total stress durations before breakdown are respectively about  $2.6 \times 10^4 \text{ s}$  (~7h15) and  $1.6 \times 10^4 \text{ s}$  (~4h30).

The corresponding evolution of the  $I_{DS-g_m}(V_{GS})$  transfer and transconductance characteristics and  $I_{DS}(V_{DS})$  output characteristics, throughout the complete step-stress sequence, for a normally-off device is shown in Fig. 4. The transfer characteristics consist in an increase of gate bias  $V_{GS}$  from -1.5 V to 2 V by 25 mV steps at a drain bias  $V_{DS}$  of -4 V. The

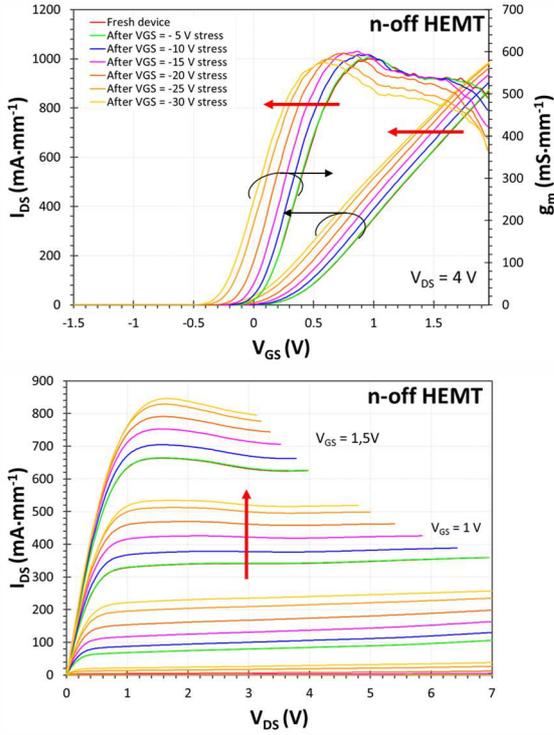


Fig. 4. Evolution of  $I_{DS}$ - $g_m(V_{GS})$  transfer characteristic and  $I_{DS}(V_{DS})$  output characteristic in a normally-off HEMT throughout the step-stress experiment with  $d_{I-V} = -5V$  intervals.

output characteristics consists in an increase of drain bias  $V_{DS}$  from 0 V to 7 V by 25 mV steps, while increasing the gate bias  $V_{GS}$  from -1 V to 1.5 V by 0.5 V steps. These DC I-V interim measurements were carried out with  $d_{I-V} = -5V$  intervals from  $V_{GS, stress} = 0V$  to breakdown, occurred at  $V_{Bd} = -31V$ . A negative shift in  $g_m(V_{GS})$  and  $I_{DS}(V_{GS})$  characteristics is observed from  $V_{GS, stress} = -10V$  to breakdown. This results in a negative shift of the threshold voltage  $V_{th}$  from 381 mV to -48 mV (deduced by the linear extrapolation of the transfer characteristics) of the normally-off device. However, the extrinsic  $g_m$  transconductance and  $g_{m, max}$  extrinsic peak transconductance remain unchanged. As a result, it can be assumed that the positive shift in  $I_{DS}$  drain current density seen in the corresponding  $I_{DS}(V_{DS})$  output characteristics is induced by the negative shift in  $V_{th}$ . A -429 mV shift of  $V_{th}$  leading to a  $\sim 200 \text{ mA}\cdot\text{mm}^{-1}$  shift in  $I_{DS}$  (at  $V_{DS} = 2V$  and  $V_{GS} = 1V$ ) is observed after the stress at  $V_{GS} = -30V$ . Similar degradation signature was identified in a previous study on this technology in the case of a step-stress experiment carried out in semi-on-state operation [9].

Fig. 5 shows the evolution of the  $I_{DS}$ - $g_m(V_{GS})$  transfer and transconductance characteristics and  $I_{DS}(V_{DS})$  output characteristics, throughout the

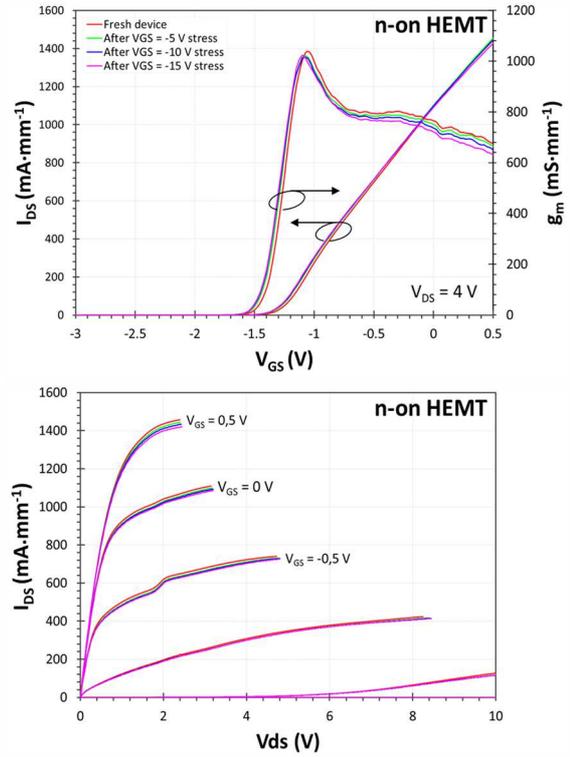


Fig. 5. Evolution of  $I_{DS}$ - $g_m(V_{GS})$  transfer characteristic and  $I_{DS}(V_{DS})$  output characteristic in a normally-on HEMT throughout the step-stress experiment with  $d_{I-V} = -5V$ .

complete step-stress sequence ( $d_{I-V} = -5V$ ), for a normally-on device. The transfer characteristics consist in an increase of gate bias  $V_{GS}$  from -3 V to 0.5 V by 25 mV steps at a drain bias  $V_{DS}$  of -4 V. The output characteristics consist in an increase of drain bias  $V_{DS}$  from 0 V to 10 V by 25 mV steps, while increasing the gate bias  $V_{GS}$  from -2 V to 0.5 V by 0.5 V steps. In contrast, the fluorine-free co-integrated normally-on GaN HEMT showed no significant degradation in transfer and output characteristics, prior to breakdown, occurred at  $V_{Bd} = -19V$ .

It can be assumed that the vertical electric field induced by the gate reverse bias step-stress experiment provides enough Coulomb force for a possible drift of the negatively-charged F-ions. In this way, the magnitude of the vertical electric field induced by the gate bias - and therefore the magnitude of the Coulomb force - can drive F-ions towards or away from the gate metallisation, according to the electric field orientation. Specifically, fluorine ions are expected to drift away from the gate metallisation in reverse gate bias and towards the gate metallisation in forward gate bias. While F-ions are located within the GaN channel and under the 2DEG, the gate reverse-bias step-stress experiment is expected to drive F-ions away from the 2DEG then deeper into the GaN channel. As a result, the ability of fluorine ions

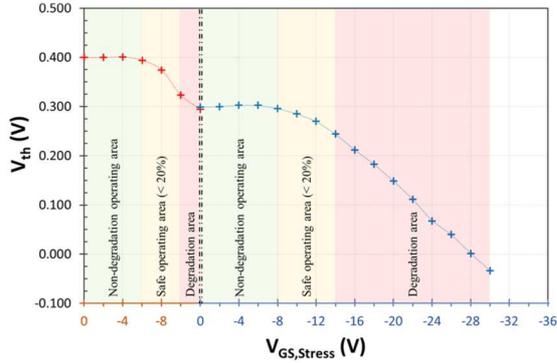


Fig. 6. Degradation of the extrapolated  $V_{th}$  threshold voltage in a normally-off HEMT throughout a specific two-stage step-stress experiment with  $d_{I-V} = -2$  V intervals.

to deplete the 2DEG is reduced, which leads to the negative shift in  $V_{th}$  observed for the normally-off device. As expected, this phenomenon only occurs in normally-off devices since normally-on ones are fluorine-free, which supports the assumption of a field-assisted fluorine ions migration mechanism. A similar degradation mechanism was identified by Ling Yang et al in off-state stress conditions in the case of several fluorine ion plasma implantation powers [10].

Furthermore, it is interesting to notice that  $V_{th}$ , and thus  $I_{DS}$ , are the only static parameters degraded throughout the reverse gate bias step-stress experiment. This behaviour is the result of the non-conventional fluorine ions implantation approach used. By implanting fluorine ions under the 2DEG channel (instead of within the barrier layer), fluorine ions are scattered away from the 2DEG, allowing it to maintain its outstanding properties.

Fig. 6 shows the evolution of the threshold voltage  $V_{th}$  for a normally-off HEMT throughout a specific two-stage reverse gate bias step-stress experiment. For this latter,  $V_{GS,Stress}$  is firstly decreased from 0 V to -12 V in steps of -0.5 V. After about 24 hours in storage conditions (floating potentials and 23°C room temperature), the step-stress is finally re-started from 0 V to breakdown, occurring at  $V_{Bd} = -31$  V. Interim DC I-V measurements are carried out with  $d_{I-V} = -2$  V intervals to provide a more accurate monitoring of  $V_{th}$  degradations. In response to the applied stresses,  $V_{th}$  is decreased from 400 mV to 295 mV during the first step-stress stage and from 299 mV to -34 mV during the second. The similitude between the ending and starting  $V_{th}$  values of the first and the second step-stress stages, respectively, indicates that there is no recovery and confirms that the degradation of  $V_{th}$  is permanent.  $V_{th}$  remains very stable down to a  $V_{GS,Stress}$  of about -6 V in the first step-stress stage and about -8 V in the second, assuming a 2%  $V_{th}$  dispersion criterion. This behavior indicates that there

is no degradation in the 0 to -6 V range (for a fresh device) and defines the non-degradation operating area. In turn, the rather linear decrease in  $V_{th}$  observed beyond  $V_{GS,Stress} = -6$  V in the first step-stress stage (resp. -8 V for the second) indicates that  $V_{th}$  is degrading. The degradation of  $V_{th}$  is still below 20% close to a  $V_{GS,Stress}$  of about -10 V (first stage). As  $V_{th}$  (and thus  $I_{DS}$ ) is the only parameter that degrades, this criterion define the safe operating area under reverse gate bias conditions at  $V_{DS} = 0$  V. Non-degradation and safe operating areas are highlighted in green and yellow, respectively, in Fig. 6. Even if  $I_{DS}$  and  $I_{GS}$  currents appear to be stable during stressful steps, making  $V_{th}$  degradation time-independent, it is important to keep in mind that this SOA is determined with steps of only 420 s (see inset of Fig. 3). Extensive robustness assessment of these devices is beyond the scope of this paper. Nevertheless, Yi et al have reported a moderate permanent negative shift (-25 mV) in  $V_{th}$  under long-term (until 288 hours) high-electric-field stress in a fluorine-treated AlGaIn/GaN HEMT [11].

During the subsequent step-stress experiment (second stage), and considering that the device under test is already degraded, the defined 20% degradation criterion is this time reached close to a  $V_{GS,Stress}$  of -14 V. The differing in degradation rate between the first and the second stage of the step-stress experiment (and also the differing in  $V_{th}$  degradation starting  $V_{GS,Stress}$  bias) can be explained by the above-mentioned field-assisted ions migration mechanism. During the first stage of the step-stress experiment, fluorine ions are expected to drift away from the 2DEG and deeper into the GaN channel as a consequence of the resulting vertical electric field stress. Since its magnitude (at fluorine ions depth) depends both on fluorine ions depth and  $V_{GS,Stress}$  bias, the further they are from the gate, the harder it will be to drive them away. In this way, the energy - and therefore the  $V_{GS,Stress}$  - required to drive away the fluorine ions (and decrease the  $V_{th}$ ), is more important in the case of the already degraded device in the second step-stress stage.

#### 4. Conclusion

Reverse gate bias step-stress experiments were carried out both on normally-on and normally-off devices, which are co-integrated to the commercial D006GH/D01GH MMIC processes. Identified degradation mode of the normally-off device is a negative shift in  $V_{th}$ , leading to a positive shift in  $I_{DS}$  as  $g_m$  and  $g_{m,max}$  remain unchanged. The lack of degradation in normally-on devices has revealed that a fluorine ion drift mechanism induced by vertical

electric field occurs in normally-off devices only, from  $V_{GS, stress}$  around -8 V. Nevertheless, this constitutes a good result for this OMMIC R&D technology, as normally-off HEMTs will be only used in digital control blocks for core chip application, with  $V_{GS}$  ranging from -3 V to sub +1 V.

### Acknowledgements

This work was supported by the French National Research Agency (ANR) through the PRCE project EDGaN and the LABEX GANEX.

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