



**HAL**  
open science

## Exploring the analytical boundaries of capacitive feedback transimpedance amplifiers

Quentin Schmidt, Adrien Morel, Yasser Moursy, Houssein Elmi Dawale,  
Gerard Billiot, Franck Badets

► **To cite this version:**

Quentin Schmidt, Adrien Morel, Yasser Moursy, Houssein Elmi Dawale, Gerard Billiot, et al.. Exploring the analytical boundaries of capacitive feedback transimpedance amplifiers. ICECS 2021 - 28th IEEE International Conference on Electronics, Circuits, and Systems, Nov 2021, Dubai, United Arab Emirates. 10.1109/ICECS53924.2021.9665553 . hal-03527154

**HAL Id: hal-03527154**

**<https://hal.science/hal-03527154v1>**

Submitted on 10 Jun 2024

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# Exploring the analytical boundaries of capacitive feedback transimpedance amplifiers

Quentin Schmidt, Adrien Morel, Yasser Moursy, Houssein Elmi Dawale, Gérard Billiot, Franck Badets  
 Univ. Grenoble Alpes, CEA, LETI, F-38000 Grenoble, France  
 Email: quentin.schmidt@cea.fr

**Abstract**—This paper proposes a comprehensive model of capacitive feedback transimpedance amplifiers, based on an analysis of the parasitics and non-idealities of the system. The proposed model is in good agreement with circuit simulations (less than 2% error on the gain and 18% on the bandwidth for large set of parameters), and allows to compute the analytical boundaries of the capacitive topology. Finally, a comparative assessment between capacitive and resistive topologies in terms of performance is proposed and highlights the salient performances of capacitive feedback transimpedance amplifiers.

**Index Terms**—Transimpedance amplifier, Capacitive TIA, Analytical model, Pareto frontier, Topology boundaries, R-TIA, C-TIA.

## I. INTRODUCTION

Transimpedance amplifiers (TIA) are key building blocks of various readout architectures, as they combine impedance adaptation with relatively high gain. Depending on targeted application, a high gain and bandwidth might both be required while the noise and power consumption need to be minimized [1], [2]. A vast number of TIA structures were introduced [2]. Among literature, one of the simplest TIA is the resistive feedback TIA (R-TIA) that has been thoroughly analyzed and optimized in previous works. The trade-offs of R-TIA as well as their limitations in term of gain-bandwidth are relatively well-understood [3].

However, specific applications such as nanomechanical mass sensing (i.e. for the detection of viruses, bacteria, proteins, DNA fragments, etc. ) require particularly aggressive design goals which are out-of reach for R-TIA implementations [4], [5]. Indeed, for this kind of application, TIA must both combine high bandwidth (up to 300 MHz), high gain (above  $1\text{M}\Omega$  to amplify the nA-level currents), low noise and low power consumption ( $< 1\text{mW/TIA}$  for massive readout of sensors arrays) .

In 2000, Razavi introduced the capacitive feedback TIA (C-TIA) topology for optical fiber receivers applications [1]. Compared to R-TIA, C-TIA allows to relax the trade-off between bandwidth and gain, while decreasing the TIA noise. In [1], was presented a simplified model of such C-TIA in order to evaluate its gain and bandwidth under stringent assumptions on the components used, on the sensor, on the biasing circuit, and on the TIA load. Further analysis have been realized by Shadoost et al. in [6] and in [7] in order to analytically optimize the noise of the C-TIA. Finally, in 2020, Romanova et al. questioned the accuracy of the Razavi's model for modern technologies and applications, and

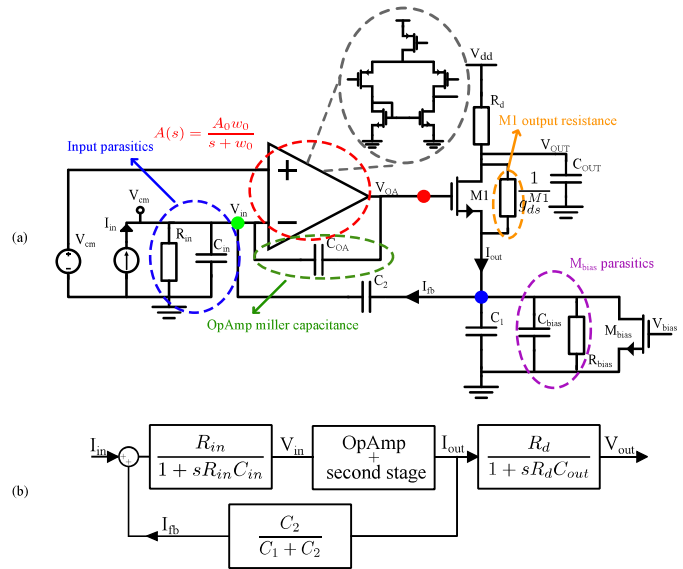


Fig. 1. (a) C-TIA schematic and (b) its associated block diagram.

proposed a new model to predict the gain of the C-TIA [8]. Unfortunately, the key characteristics of C-TIA are currently not totally known and literature equations are not accurate enough to define the limits of the topology and to compare them realistically to the R-TIA.

This paper focuses on the development of an accurate analytical model of the C-TIA key parameters (gain, bandwidth). The details of this analytical model as well as its verification against circuit simulations are described in section II of this paper. Based on this model, we propose in section III an analysis of the C-TIA performances, and the exploration of its performances boundaries. Finally, in section IV, we compare the C-TIA with the R-TIA architecture. This comparison allows the verification and quantification of the initial intuition that the C-TIA presents a better gain/bandwidth trade-off than the R-TIA topology.

## II. C-TIA ANALYTICAL MODELING

The schematic of a standard C-TIA is shown in Fig. 1.a. The input current flowing from the sensor  $I_{in}$ , is added to the feedback current  $I_{fb}$  flowing through the parallel capacitor  $C_2$ . These two currents flow through the input impedance of the

TABLE I  
PARAMETERS OF THE C-TIA MODEL AND THE EQUATIONS NUMBER

Parameters	Variables	Typical values	Influences on eq. (x)
Input current	$I_{in}$	$1nA$	(1-12)
Input capacitance	$C_{in}$	$100fF - 1pF$	(1-12)
Input resistance	$R_{in}$	$100k\Omega$	(1,2)
Feedback capacitance 1	$C_1$	$20fF - 1pF$	(2-12)
Feedback capacitance 2	$C_2$	$20fF - 1pF$	(2-12)
Output resistance	$R_d$	$30k\Omega$	(10,12)
OpAmp static gain	$A_0$	$40dB$	(1-12)
OpAmp bandwidth	$\omega_0$	$68 \times 10^6 rad.s^{-1}$	(4-12)
OpAmp miller cap.	$C_{OA}$	$10fF$	(4-12)
OpAmp input cap.	$C_{gs}$	(added to $C_{in}$ )	(4-12)
$M_1$ transcond.	$g_{m1}$	$300\mu S$	(1-12)
$M_1$ output admittance	$g_{ds1}$	$4\mu S$	(4-12)
$M_1$ bulk transcond.	$g_{mb1}$	$49.6\mu S$	(1)
$M_{bias}$ output resistance	$R_{bias}$	$10\mu S$	(3)
$M_{bias}$ parasitic cap.	$C_{bias}$	(added to $C_1$ )	(2-12)
Output capacitance	$C_{out}$	$1fF - 10pF$	(10,12)

system, composed of the input parasitic capacitance  $C_{in}$  and the input parasitic resistance  $R_{in}$ , to generate the input voltage  $V_{in}$ . This voltage is amplified by the operational amplifier (OpAmp), and fed in a second stage made of a transistor  $M_1$  which generates the output current,  $I_{out}$ . Part of  $I_{out}$  is sent back in the input node (as a feedback current  $I_{fb}$ ), depending on the capacitive ratio  $C_1/(C_1 + C_2)$  and also generates the output voltage when it flows in the output pole  $C_{out}/R_d$ . The operation of the C-TIA is depicted schematically by the block diagram in Fig. 1.b.

The various parameters, parasitics and non-idealities that can be taken into account are shown in Fig.1.a, and listed in Table I. Taking into account all of these parasitics leads to a fifth order transfer function (TF) that hardly favors an intuitive and comprehensive design. Nevertheless, it is possible to simplify the analysis by separating the influences of each parasitics (e.g.  $R_{bias}$  is only taken into account in the derivation of the zero of the TF,  $\omega_{z,1}$  in (3), and disregarded in all the other equations). Table. I lists all parasitics and shows in which equation they are taken into account.

Thanks to a DC analysis, we derive the static gain  $G_{DC}$  whose expression is given by (1). Here, the bulk transconductance of  $M_1$  ( $g_{mb1}$ ) is the only non-negligible parasitic.

$$G_{DC} = \frac{A_0 R_{in} g_{m1} R_d}{1 + R_{bias} g_{m1} + g_{mb1} R_{bias}} \quad (1)$$

The pole  $\omega_{p,1}$  associated with the input parasitics ( $C_{in}$  and  $R_{in}$ ) is represented by a green dot in Fig. 1.a. This constitutes the first pole of the TF  $I_{out}/I_{in}$ . It is possible to derive its expression by writing  $I_{out}/I_{in}$  considering ideal components ( $M_1$ ,  $M_{bias}$  and the OpAmp) while only taking into account the input parasitics. The expression of  $\omega_{p,1}$  is given by (2), under the assumption that  $A_0 \gg 1$ .

$$\omega_{p,1} = \left[ \frac{C_1 + C_2}{g_{m1}} + R_{in}(A_0 C_2 + C_{in}) \right]^{-1} \quad (2)$$

The biasing zero  $\omega_{z,1}$  associated with the biasing transistor  $M_{bias}$  parasitics ( $C_{bias}$  and  $R_{bias}$ ) is represented by a blue

dot in Fig. 1.a. The expression of this zero can be found by writing  $I_{out}/I_{in}$  while only taking into account the biasing parasitics ( $R_{bias}$ ), and is given by (3).

$$\omega_{z,1} = [R_{bias}(C_1 + C_2) + \frac{C_2 R_{bias}}{A_0}]^{-1} \quad (3)$$

The OpAmp and its non-ideal TF, given by  $A(s) = (A_0 \omega_0)/(s + \omega_0)$ , are responsible for the double-pole  $\omega_{p,2}$  represented by the red dot on Fig. 1.a. The analytical expression of  $\omega_{p,2}$  can be found from the TF  $I_{out}/I_{in}$  with no biasing parasitics and no  $R_{in}$ . This TF is given by (4).

$$H_{p,2} = \frac{I_{out}}{I_{in}} = \frac{G_0 \omega_{p,2}^2}{s^2 + 2 m \omega_{p,2} s + \omega_{p,2}^2} \quad (4)$$

Where  $G_0$  and  $m$  represent the static gain of the TF and its damping factor, respectively. The expressions of  $G_0$ ,  $m$  and  $\omega_{p,2}$  are given by (5), (6) and (7).

$$\omega_{p,2} = \sqrt{\frac{g_{m1} \omega_0 (C_{in} + A_0 C_2 + C_m)}{C_T^2 \gamma}} \quad (5)$$

$$m = \omega_{p,2} \frac{(C_T^2 + C_m(C_1 + C_2))\gamma + \frac{g_{m1}}{\omega_0}(C_{in} + C_2)}{2g_{m1}(C_{in} + A_0 C_2 + C_m)} \quad (6)$$

$$G_0 = \frac{(C_1 + C_2)A_0 + C_2}{C_{in} + (C_2 + C_{OA})A_0 + C_2} \quad (7)$$

With  $C_m = A_0 C_{OA}$  the equivalent Miller capacitance,  $C_T^2 = C_{in}C_1 + C_2C_{in} + C_1C_2$  and  $\gamma = 1 + R_d g_{ds1}$ . The transfer function  $I_{out}/I_{in}$  of the C-TIA is obtained by combining the poles and zeros that have been previously derived in (1)-(7).

$$H_{model} = \frac{I_{out}}{I_{in}} = \frac{\frac{G_{DC}}{R_d} \left(1 + \frac{s}{\omega_{z,1}}\right)}{1 + \frac{s}{\omega_{p,1}}} H_{p,2} \quad (8)$$

As shown in Fig.2, we consider that the frequency band of interest of our TIA goes from the first zero to the second pole of the system. The 3-dB bandwidth of  $H_{model}$ ,  $\Delta\omega_{p,2}$ , is calculated from the gain in this frequency band of interest and not from the DC gain. This 3-dB bandwidth depends on the second pole of the C-TIA, thus it can be deduced from (5) and (6), and is expressed by (9).

$$\Delta\omega_{p,2} = \omega_{p,2} \sqrt{-(2m^2 - 1) + \sqrt{(2m^2 - 1)^2 + 1}} \quad (9)$$

A good approximation of the complete C-TIA TF can be obtained by considering that the output pole is independent from the TF given by (8). In this case, the complete C-TIA TF  $H_{C-TIA}$  is given by (10).

$$H_{C-TIA} = \frac{V_{out}}{I_{in}} = H_{model} \frac{R_d}{s + R_d C_{out}} \quad (10)$$

From (10), the bandwidth of the C-TIA (in the frequency band of interest) depends on the dominant pole (either  $\omega_{p,2}$  or  $(R_d C_{out})^{-1}$ ) and can thus be expressed by (11). The C-TIA

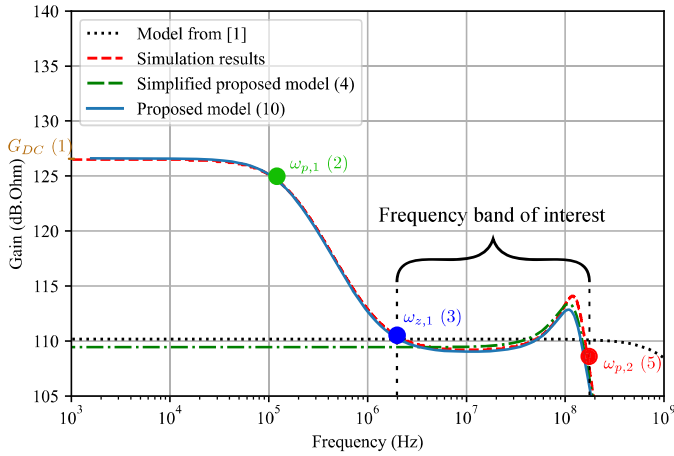


Fig. 2. Bode plots  $V_{out}/V_{in}$  with the model from [1] (black), from circuit simulations (red), with the proposed model (blue) and with the simplified model given by (4) multiplied by  $R_d$  ( $C_1 = 1pF$ ,  $C_2 = 100fF$ ).

gain in the frequency band of interest ( $\forall \omega \in [\omega_{z,1}, \omega_{p,2}]$ ) can be approximated by (12).

$$G_{TIA} = R_d G_0 \quad (11)$$

$$\Delta\omega_{BW} = \min(\Delta\omega_{p,2}, (R_d C_{out})^{-1}) \quad (12)$$

### III. C-TIA ANALYSIS AND TOPOLOGY BOUNDARIES

In this section, we compare our model predictions with circuit simulations. We will first assume that the output pole of the C-TIA does not limit the frequency bandwidth (i.e.  $(R_d C_{out})^{-1} \gg \Delta\omega_{p,2}$ ), in order to focus our analysis on the intrinsic boundaries of the C-TIA topology. Unless otherwise specified, the set of parameters used in this section is given by Table I.

Figure 2 depicts the bode plots of the proposed model (10) (blue solid line), the proposed simplified model (4) multiplied by  $R_d$  (green dashed line), the Razavi model [1] (black dotted line) and the bode plot obtained from circuit simulations (red dashed line). The zero  $\omega_{z,1}$  (3), and the two dominant poles  $\omega_{p,1}$  (2) and  $\omega_{p,2}$  (5) are indicated on the red line by a blue, a green and a red dot, respectively. We can notice that the proposed model (10) is in good agreement with circuit simulations in the whole range of frequencies while the simplified model (4) is only correct for high frequencies ( $\omega > \omega_{z,1}$ ). Hence the proposed simplified model allows to accurately predict the bandwidth and gain in the frequency range of interest. The differences between the circuit simulations and [1] can be explained by the fact that [1] considers an ideal OpAmp TF.

Figure 3 presents the bandwidth and gain that can be obtained with our C-TIA simplified model, in the  $(C_1, C_2)$  plane, as well as the relative error of our model. The capacitors  $C_1$  and  $C_2$  being integrated, their values are chosen between  $20fF$  and  $1pF$ . Figure 3 shows that our simplified model is in good agreement with the circuit simulations, with a relative error on the bandwidth up to 18% and a relative error on

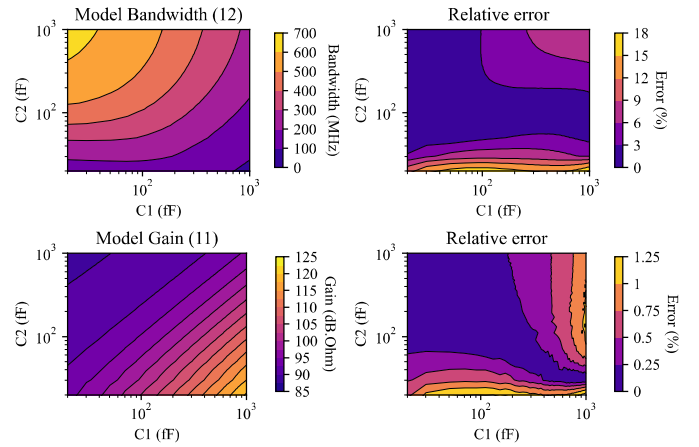


Fig. 3. C-TIA bandwidth and gain obtained with our model (11) and (12) and their relative error in the  $(C_1, C_2)$  plane.

the gain up to 1.25% compared to simulation results. We can observe that both errors grow with smaller  $C_2$  and that the bandwidth error grows with larger capacitances  $C_1$  and  $C_2$  while the gain error grows with larger  $C_1$ . Indeed, when  $C_2$  gets smaller, some parasitic capacitances that have not been taken into account in our model become non-negligible. On the other hand the parasitic capacitances of  $M_1$ ,  $C_{gd1}$  and  $C_{gs1}$ , are responsible for the appearance of a complex pole at the output of the OpAmp. This pole depends on the values of  $C_1$  and  $C_2$  and its influence becomes significant when  $C_1$  and  $C_2$  get large. Nevertheless, Figure 3 shows that the C-TIA exhibits promising performances in term of bandwidth and gain. E.g., with a gain of  $100dB/Ohm$ , it is possible to reach a bandwidth larger than  $400MHz$ . Note that these results have been obtained under a total current consumption of  $140\mu A$  (fixing the values of  $A_0$ ,  $\omega_0$  and  $g_{m1}$ ).

Figure 4 shows the reachable gain/bandwidth for every value of  $C_1$  and  $C_2$  (with  $C_i \in [20fF, 1pF]$ ) for a fixed power consumption. The color of the surface indicates the ratio  $C_1/C_2$  (with purplish tones corresponding to low ratio values, and yellowish tones corresponding to high ratio values). We can verify that a higher  $C_1/C_2$  ratio leads to a larger bandwidth while a lower  $C_1/C_2$  ratio leads to a larger gain. The optimal Pareto frontier of the C-TIA is shown by the black dashed line in Fig.4, and defines the performance boundaries of the C-TIA for a particular power consumption. If the power consumption of the C-TIA is increased, the Pareto frontier will rise almost vertically (due to the increase of  $A_0$ ,  $\omega_0$  and  $g_{m1}$ ). In the other hand, an increase of the output resistor  $R_d$  leads to an horizontal shift of the Pareto frontier, leading to higher transimpedance gains.

Finally, Fig. 4 shows two Bode plots corresponding to high (red) and low (blue)  $C_1/C_2$  ratios. These Bode plots show that a resonance peak is associated with low  $C_1/C_2$  ratios but not with high  $C_1/C_2$  ratios. This suggests that a too low  $C_1/C_2$  ratio might lead to stability issues. This observation can be confirmed analytically by the analysis of the damping factor

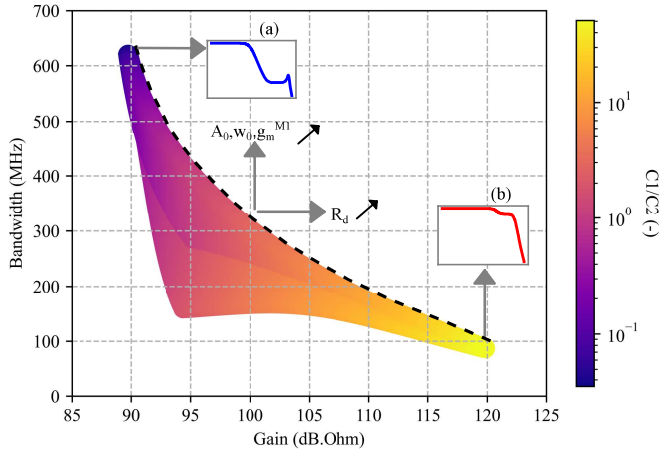


Fig. 4. C-TIA reachable bandwidth and gain.

in equation (6) with various values of  $C_1/C_2$ .

As mentioned previously, we assumed in Fig.2, 3 and 4 that the output pole of the C-TIA does not limit the frequency bandwidth ( $(R_d C_{out})^{-1} \gg \Delta\omega_{p,2}$ ). However, if the output capacitor gets too large (important  $C_{out}$ ) or if the C-TIA gain has to be large (important  $R_d$ ), the output pole might become the dominant pole of the system, limiting the C-TIA bandwidth. Thus, as shown in Fig.5.a (red dashed line), the output pole acts as a bandwidth limit depending on the value of  $R_d$  and  $C_{out}$ .

#### IV. COMPARISON C-TIA VERSUS R-TIA

Equation (13) allows us to compute the reachable performances that can be obtained with a R-TIA and to compare them with our C-TIA model [3].

$$\frac{V_{out}}{I_{in}} = \frac{-R_F}{\frac{R_F(C_{OA}+C_{in})}{\omega_0 A_0} s^2 + \frac{1+\omega_0 R_F(C_{in}+A_0 C_{OA})}{\omega_0 A_0} s + 1} \quad (13)$$

With  $R_F$  the R-TIA feedback resistance. The output capacitor  $C_{out}$  does not appear explicitly in (13), but has a direct influence on the OpAmp bandwidth  $\omega_0$  [3].

Figure 5.a shows the aforementioned Pareto frontier of the C-TIA (black dashed line) compared to the Pareto frontier of the R-TIA (orange solid line). We can observe that the Pareto frontier of the C-TIA is always greater than the Pareto frontier of the R-TIA, in the case where the output pole's influence remains negligible. Figure 5.b shows the bandwidths of both topologies against an increasing  $C_{out}$  for a gain of  $120dB.Ohm$ . We can observe that the performances of C-TIA are always greater than those of the R-TIA (four to five times greater for low  $C_{out}$  values). However, the increase of performance brought by the C-TIA topology becomes smaller as the output capacitance  $C_{out}$  is increased. In order to fully exploit the C-TIA topology and its improved performances, it is thus necessary to minimize  $C_{out}$  (e.g. by connecting its output to a buffer).

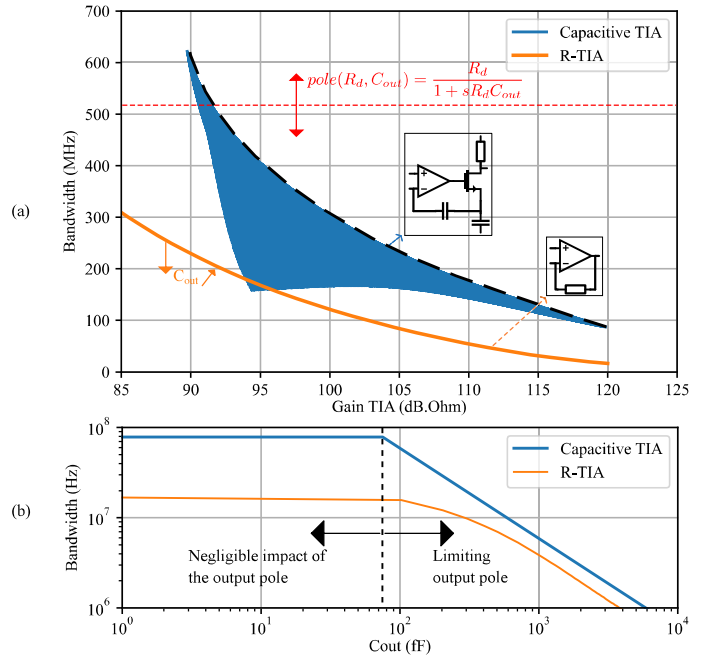


Fig. 5. (a) C-TIA (blue) and R-TIA (orange) reachable bandwidth and gain and (b) R-TIA and C-TIA bandwidth as a function of  $C_{out}$  with a fixed gain of  $120dB.Ohm$ ,  $C_1 = 1pF$ ,  $C_2 = 15fF$ ,  $R_d = 27k\Omega$ ,  $R_F = 1M\Omega$ .

#### V. CONCLUSION

In this paper, we propose a model for capacitive feedback transimpedance amplifiers, thanks to a thorough analysis of the various system parasitics and non-idealities. Our model allows to accurately predict the bandwidth and gain of the C-TIA with various set of parameters, and to compute its performance boundaries. These boundaries allowed us to quantify the gain and bandwidth improvement brought by the C-TIA topology, compared to the more traditional R-TIA topology. Further works will explore how the C-TIA boundaries could be improved, depending on the OpAmp topology for instance.

#### REFERENCES

- [1] B. Razavi, "A 622 Mb/s 4.5 pA/spl radic/Hz CMOS transimpedance amplifier [for optical receiver front-end]," 2000 IEEE ISSCC, pp. 162-163, 2000.
- [2] A. Romanova and V. Barzdenas, "A Review of Modern CMOS Transimpedance Amplifiers for OTDR Applications," Electronics, vol. 8, no. 10, p. 1073, 2019.
- [3] E. Säckinger, "The Transimpedance Limit," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 8, pp. 1848-1856, Aug. 2010.
- [4] Gil-Santos, E., Ruz, J.J., Malvar, O. et al., "Optomechanical detection of vibration modes of a single bacterium," Nat. Nanotechnol. 15, 469-474 (2020).
- [5] H. E. Dawale, L. Sibeud et al., "Compact Modeling and Behavioral Simulation of an Optomechanical Sensor in Verilog A.," IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4677-4681, Nov. 2020.
- [6] S. Shahdoost, A. Medi and N. Saniei, "A 1.93 pA/spl Hz transimpedance amplifier for 2.5 Gb/s optical communications," 2011 IEEE ISCAS, pp. 2889-2892, 2011.
- [7] S. Shahdoost, A. Medi, B. Bozorgzadeh and N. Saniei, "A novel design methodology for low-noise and high-gain transimpedance amplifiers," 2014 EAMTA, pp. 77-82, 2014.
- [8] A. Romanova and V. Barzdenas, "Programmable-Gain Capacitive Feedback TIA for Low-Noise Applications in CMOS," pp. 1-6, 2020.