



HAL
open science

Memristor models optimization for large-scale 1T1R memory arrays

Basma Hajri, Mohammad M Mansour, Ali Chehab, Hassen Aziza

► To cite this version:

Basma Hajri, Mohammad M Mansour, Ali Chehab, Hassen Aziza. Memristor models optimization for large-scale 1T1R memory arrays. 2018 International Conference on IC Design & Technology (ICICDT), Jun 2018, Otranto, France. pp.109-112, <10.1109/ICICDT.2018.8399768>. <hal-03526089>

HAL Id: hal-03526089

<https://hal.science/hal-03526089v1>

Submitted on 14 Jan 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire HAL, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

Memristor Models Optimization for Large-Scale 1T1R Memory Arrays

Basma Hajri, Mohammad M. Mansour and Ali Chehab

¹Department of Electrical and Computer Engineering
American University of Beirut
Beirut 1107 2020, Lebanon
E-mail: {bh24, mmansour, chehab}@aub.edu.lb

Abstract— Recently, memristive devices have been shown to possess unique and intriguing properties such as small size, high density, non-volatility, state-dependent behavior, good scalability, very low leakage current, and compatibility with CMOS technology. A critical requirement for using memristive devices at the circuit level is the availability of a simple, accurate and efficient model that adequately characterizes circuit performance. Most existing models for memristive devices presented in the literature suffer from high complexity and computational inefficiency. In this paper, we propose a new scheme to reduce the complexity of existing models and improve simulation time while maintaining circuit designer requirements in terms of accuracy. Using this technique, the simulation time can be improved by around 20% while maintaining a good accuracy.

Keywords—Memristor, models, complexity reduction, Resistive Random Access Memory (RRAM), simulation time, model optimization.

I. INTRODUCTION

Recently, Resistive Random Access Memory (RRAM) devices received considerable attention in light of their fast programming and high scalability characteristics. In its simplest form, a resistive memory element relies on a Metal/Insulator/Metal (MIM) stack that acts as a resistive switch. This concept of resistive switching is at the core of the behavior of the so-called memristor device discovered by Chua [1]. A critical requirement for using memristors at a circuit level is the availability of a predictive model for device behavior that can be used in simulations, as well as a guide to assist designers. An accurate physical model of a memristive device will not only lead to a better understanding of the memory cell behavior but will also result in a better exploitation of its unique properties in novel systems and architectures combining data storage and processing in the same physical location. However, typically, such a model is complicated and computationally inefficient.

A model with simpler expressions rather than the complex equations is therefore desired. Yet, the accuracy of the simple model must be adequate. Large scale memristor crossbar simulations are typically done using simulation tools such as *LTspice* and *PSpice*. These simulations can only handle 3,000 memristors before simulation time becomes unreasonable [2]. Using these tools for simulating large-scale memristor crossbars takes more than 3 days to train as they are non-parallel simulators that utilize only a single-core processor [3].

Hassen Aziza

IM2NP, UMR CNRS 7334, Aix-Marseille Université
38 rue Joliot Curie, F-13451
Marseille Cedex 20, France
E-mail: hassen.aziza@univ-amu.fr

This paper presents a general technique used to reduce model's simulation time at the circuit level. This technique can be applied to all complex existing memristor models. A selection of actual memristor models is presented in Section II. In Section III, a technique for improving the computational efficiency and simulation runtime of the existing models is discussed. Simulation results are presented in Section IV. Concluding remarks are developed in Section V.

II. OVERVIEW OF MEMRISTOR COMPLEX MODELS

Recently, research on memristors has increased rapidly due to their promising potential in a wide range of applications, backed by the maturity of memristor manufacturing process. A typical memristor device consists of two electrodes (typically metal electrodes), and the resistance of the device depends on the polarity and magnitude of the voltage applied across the electrodes. The first memristor device was fabricated in 2008 by R. Stanley Williams in HP labs [4]. It was based on a MIM structure using Platinum for the electrodes and Titanium dioxide as insulator. Figure 1 shows a cross-section of the first HP TiO₂-memristor consisting of a high conductive (doped) part and a low conductive (un-doped) part placed in between two platinum electrodes (Pt). R_{off} and R_{on} are the high resistance and low resistance, w the length of the doper region and D the structure length. The boundary between the two parts is dynamic and is moved back and forth by the passing charge carriers. The parameter w is a mathematical variable that describes the position of the boundary [4].

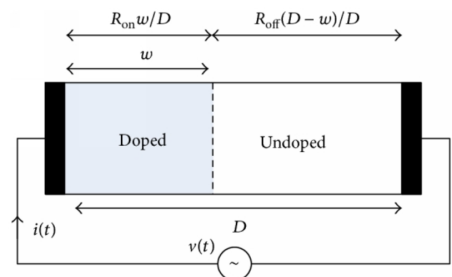


Fig. 1. Cross-section of the first HP TiO₂-memristor [4]

When the voltage is switched off, the resistance remains at its previous level. Thus, we can say that a memristor “remembers” its history; this is the non-volatility property that gives it the name of “memory resistor”.

Currently, research is in full swing to use memristors in analog circuits, digital or programmable logic controllers, computers and sensors [5]. Thus, new models of memristors

need to be developed for design engineers to use as circuit elements throughout design exploration. Physics-based device models are generally adopted to accurately capture device characteristics for simulations. However, the use of physics-based compact models is still infeasible for simulations of large arrays due to the enormous amount of required computing resources as presented in Fig. 2; it takes approximately a year to simulate a 400 Mb array [6].

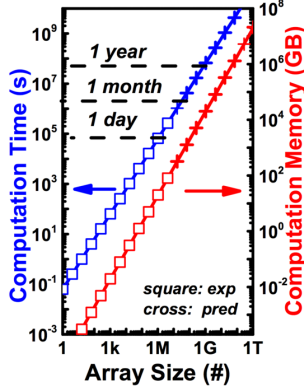


Fig. 2. Computation time and memory vs. array size [6]

A model is considered complex if the equations use hyperbolic functions and exponentials rather than polynomials [7]. At the expense of computational efficiency, hyperbolic sine and exponential functions have been used in many memristor models in the literature [9-17]. Hyperbolic sine function is widely used in physics-based device models since it represents very well the hysteresis of the memristor MIM structure. Exponential functions define accurately the Schottky barrier between the oxide layer and the bottom electrode [8]. The three models considered in this study are the non-Linear Ion Drift Model [9], the Simmons Tunnel Barrier Model [10] and the Stanford model [11]. These models are considered complex and cover all different types of physics based I-V equations. These models are listed below and detailed in this section.

A. Non-Linear Ion Drift Model

The non-linear ion drift model presented in Fig. 1, is an improvement of the linear ion drift model presented in [9]. Studies and experiments have proved that the behavior of the implemented memristors is quite nonlinear and the linear ion drift model is not accurate enough. The non-linearity of the device is voltage dependent; a nonlinear dependence between the voltage and the internal state derivative is assumed. By using physically reasonable parameters, this model properly captures both the static electric conduction as well as the switching dynamic behaviors and provides a good fit to the experimental data. The major application of this memristor model is in logic gates. In this model, the relationship between the current and voltage given by:

$$i(t) = \omega(t)^n \beta \sinh(\alpha v(t)) + \chi [\exp(\gamma v(t)) - 1] \quad (1)$$

where β , χ and γ are experimental fitting parameters, and n is a parameter that determines the influence of the state variable, ω , on the current. ω is a normalized parameter within the interval $[0,1]$. In this model, an asymmetric switching behavior is assumed. When the device is in the ON state, ω is close to 1 and the current is dominated by the first expression in (1) (i.e. $\beta \sinh(\alpha v(t))$), which describes a tunneling phenomenon. When the device is in the OFF state, ω is close to 0 and the current is dominated by the second expression

(i.e. $\chi[\exp(\gamma v(t)) - 1]$), which is similar to an ideal diode equation. This model assumes also a nonlinear dependence on voltage in the state variable differential equation:

$$\frac{d\omega}{dt} = a \cdot f(\omega) \cdot v(t)^m \quad (2)$$

where a and m are constants, m is an odd integer, and $f(\omega)$ is a window function.

B. Simmons Tunnel Barrier Model

Pickett et al. presented a more accurate physical model of a memristors [10]. Instead of two resistors in series, as in HP's model, a resistor is used in series with an electron tunnel barrier as shown in Fig. 3. The model exhibits nonlinear and asymmetric switching characteristics. The relationship between the current and voltage is shown as an implicit equation (3):

$$i(t) = \tilde{A}(x, Vg) e^{-\beta(Vg, x)} \times \left[\Phi(Vg, x)^{3/2} - \sqrt{\Phi(Vg, x) + eVg} (\Phi(Vg, x) + e|Vg|) \right] \quad (3)$$

$$V_g = v - i(t) R_s \quad (4)$$

$$\frac{dx(t)}{dt} = \begin{cases} c_{\text{off}} \sinh\left(\frac{i}{i_{\text{off}}}\right) e^{\left(-\exp\left(\frac{x-a_{\text{off}}}{w_c} - \frac{|i|}{b}\right) - \frac{x}{w_c}\right)} & i \geq 0 \\ c_{\text{on}} \sinh\left(\frac{i}{i_{\text{on}}}\right) e^{\left(-\exp\left(\frac{x-a_{\text{on}}}{w_c} - \frac{|i|}{b}\right) - \frac{x}{w_c}\right)} & i < 0 \end{cases} \quad (5)$$

The state variable x is the Simmons tunnel barrier width, so its derivative can be interpreted as the oxygen vacancy drift velocity given in equation (5); where c_{off} , c_{on} , i_{off} , i_{on} , a_{off} , a_{on} , w_c and b and are fitting parameters. R_s is the channel resistance, v is the internal voltage of the device and V_g is the voltage in the oxide region.

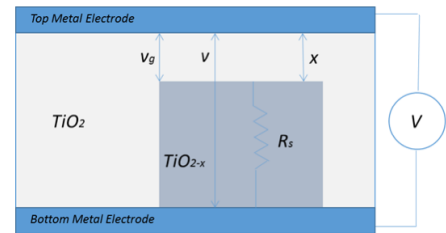


Fig. 3. Physical memristor structure based on Simmons model [10]

C. Stanford Model

The Stanford RRAM model is a SPICE-compatible compact model that describes the switching performance for bipolar metal oxide RRAM [11]. In principle, this model has no limitations on the RRAM cell size. The complex process of ion and vacancy migration is simplified into the growth of a single dominant filament that preserved the essential switching physics as presented in Fig. 4. The size of the tunneling gap, g , which is the distance between the tip of the filament and the opposite electrode, is the primary variable determining the device resistance. The current conduction is exponentially dependent on the tunneling gap distance. This distance is found by calculating the growth of the gap, taking into consideration the electric field, temperature-enhanced oxygen ion migration, and local temperature due to Joule heating. Included also is the stochastic and temperature-dependent filament movement (δg).

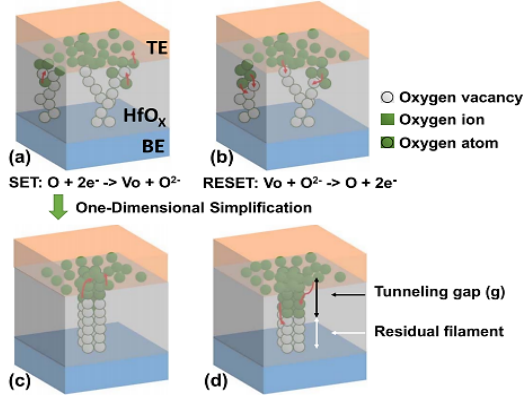


Fig. 4. Stanford-PKU RRAM model illustration. (a) and (c) Schematic of the SET and RESET switching processes and conductive filament configuration. (b) and (d) Simplified model of the conductive filament at the SET and RESET states. LRS has shorter (b) tunneling gap distance while HRS has (d) longer tunneling gap distance [11].

The current flowing through the cell is defined as:

$$I = I_0 \exp\left(-\frac{g}{g_0}\right) \sinh\left(\frac{V}{V_0}\right) \quad (6)$$

where g is the gap distance, V is the applied voltage across the cell; the prefactor I_0 , the gap coefficient g_0 , and the voltage coefficient V_0 are the parameters that are obtained from the experimental results.

The evolution rate of the gap distance g due to filament growth/rupture is given in (7):

$$\frac{d\langle g \rangle}{dt} = -v_0 \exp\left(-\frac{E_A}{KT}\right) \sinh\left(\gamma \frac{a_0}{t_{ox}} \frac{qV}{KT}\right) \quad (7)$$

where $\langle g \rangle$ reflects the average gap distance, v_0 is the velocity dependent on the attempt-to-escape frequency, E_A is the effective activation energy (migration barrier) for vacancy generation (oxygen migration), t_{ox} is the thickness of the switching material, a_0 is the hopping site distance, γ is the field local enhancement factor that accounts for the polarizability of the material.

III. MODEL COMPLEXITY REDUCTION

In order to reduce the complexity, the hyperbolic and exponential functions used in the models listed in section II, are replaced by polynomials using Taylor series, with a finite number of terms. Taylor's theorem gives quantitative estimates on the error introduced by the use of such an approximation. The polynomial formed by taking some initial terms of the Taylor series is called a Taylor polynomial [21]. Taylor's theorem leads to the following polynomial approximation of the exponential function within the interval $[-1,1]$ while ensuring an error less than 0.1% as presented in (8).

$$e^x = 1 + x + \frac{x^2}{2!} + \dots + \frac{x^6}{6!} + R_6(x); \quad R_6(x) \leq 10^{-3} \quad (8)$$

Given the properties of the exponential function:

$$e^0 = 1; \quad \frac{d}{dx} e^x = e^x; \quad e^x > 0; \quad x \in \mathbb{R} \quad (9)$$

It follows that $f_k(x) = e^x$ for all k , and in particular, $f_k(0) = 1$. Hence the k -th order Taylor polynomial of the function f at 0 and its remainder terms in the Lagrange form are given by (10):

$$P_k(x) = 1 + x + \frac{x^2}{2!} + \dots + \frac{x^k}{k!}; \quad R_k(x) = \frac{e^\xi}{(k+1)!} x^{k+1} \quad (10)$$

where ξ is some number between 0 and x . Since e^x is a monotonically increasing function by (8), we can simply use $e^x \leq 1$ for $x \in [-1, 0]$ to estimate the remainder on the sub-interval $[-1, 0]$. To obtain an upper bound for the remainder on $[0,1]$, we use the property $e^\zeta < e^x$ for $0 < \zeta < x$ to estimate e^x using the second-order Taylor expansion:

$$e^x = 1 + x + \frac{e^\xi}{2} x^2 < 1 + x + \frac{e^x}{2} x^2; \quad 0 < x \leq 1 \quad (11)$$

Then, we solve for e^x to deduce that:

$$e^x \approx \frac{1+x}{1-\frac{x^2}{2}} = 2 \frac{1+x}{2-x^2} \leq 4; \quad 0 \leq x \leq 1 \quad (12)$$

simply by maximizing the numerator and minimizing the denominator. Combining these estimates for e^x we see that:

$$|R_k(x)| \leq \frac{4x^{k+1}}{(k+1)!} \leq \frac{4}{(k+1)!}; \quad -1 \leq x \leq 1 \quad (13)$$

so, the required precision is certainly reached, when:

$$\frac{4}{(k+1)!} \leq 10^{-3} \Leftrightarrow 4 \cdot 10^3 \leq (k+1)! \Leftrightarrow k \geq 6 \quad (14)$$

For instance, as shown in Fig. 5, this approximation provides a decimal value for $e \approx 2.718$, which is correct up to three decimal places.

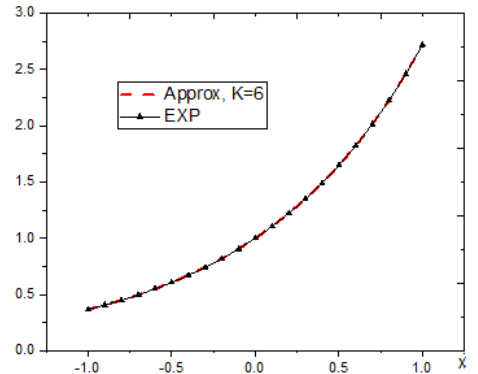


Fig. 5 Approximation of exponential (blue) by its Taylor polynomials P_k of order $k=6$ centered at $x=0$ (red).

IV. SIMULATION RESULTS

To demonstrate the effectiveness of the model reduction technique presented in section III, the three models listed in section II are considered. The exponential functions used in the models equations are replaced by their 6th order Taylor series and all hyperbolic sine functions are replaced by polynomials (15) while maintaining a precision of 10^{-3} .

$$\sinh(x) = x + \frac{x^3}{3!} + \frac{x^5}{5!} + \frac{x^7}{7!} \quad (15)$$

which follows from:

$$\sinh(x) = \frac{e^x - e^{-x}}{2} \quad (16)$$

The circuit used for simulation to perform this comparison is shown in Fig. 6, a 1T1R (one transistor one resistor) cell in series with an AC source $V(t)$ (sine of 1.8V amplitude and 2MHz frequency). The total simulation time is 1.5us.

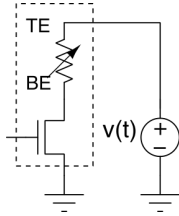


Fig. 6. Circuit used in simulation setup

As can be verified in Fig. 7 (a, b and c), the I-V characteristics remain almost the same before and after applying the complexity reduction technique which means that a precision of 10^{-3} is enough when using the models in memory applications.

Different 1T1R memory array sizes are then simulated (128b, 256b and 1Kb) and the optimization is evaluated.

Table I shows a simulation time improvement of around 7%, which might appear low for just a single cell. However, as presented in Fig. 8, the improvement becomes considerable for bigger memory array sizes. According to [6], a 1 Mb RRAM 1T1R array simulation takes more than 24 hours of CPU time using a main memory of 20 GB for a 64-core Intel(R) Xeon(R) (@2.67 GHz) server. Hence, by extrapolating the simulation results, the applied technique presents a simulation time improvement of around 18% for a 1Mb memory array.

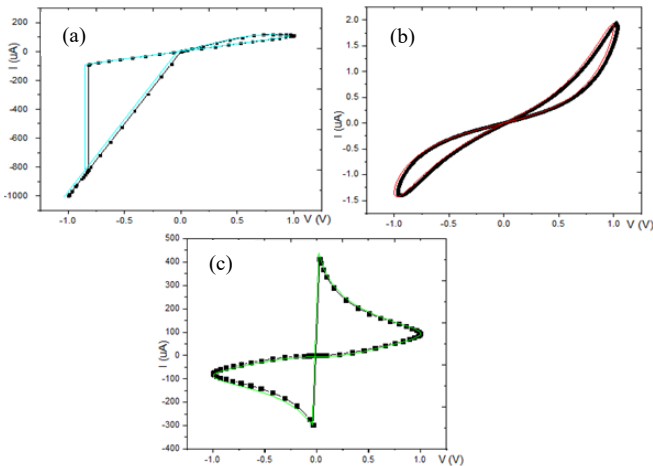


Fig. 7. (a) I-V characteristic of Simmons model before (black) and after optimization (blue), (b) I-V characteristic of Non-linear model before (black) and after optimization (red) and (c) I-V characteristic of Stanford model before (black) and after optimization (green)

TABLE I. SIMULATION TIME IMPROVEMENT AT CELL LEVEL

Model	Sim. time (ms) original	Sim. time (ms) modified	Improvement at cell level (%)
Nonlinear model	188.34	173.95	7.64
Simmons model	234.56	215.96	7.93
Stanford model	166.97	154.97	7.18

V. CONCLUSION

In this paper, various memristor models have been surveyed—nonlinear ion drift, Simmons tunnel barrier, Stanford model—and a new technique that reduces complexity and improves simulation time compared to existing models has been presented. By applying this technique, the simulation time can be reduced by around 20% while maintaining good accuracy of the model.

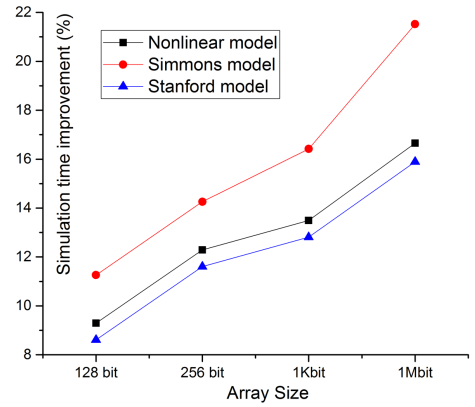


Fig. 8. Simulation time improvement for different 1T1R memory array sizes

REFERENCES

- [1] L. O. Chua, "Memristor—The missing circuit element", *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep. 1971.
- [2] C. Yakopcic, R. Hasan, and T. Taha, "Tolerance to defective memristors in a neuromorphic learning circuit," in *Proc. IEEE National Aerospace and Electronics Conference (NAECON)*, Dayton, OH, USA, June 2014, pp. 243–249.
- [3] R. Uppala, C. Yakopcic and T. M. Taha, "Methods for reducing memristor crossbar simulation time," in *Proc. IEEE National Aerospace and Electronics Conference (NAECON)*, Dayton, OH, July 2015, pp. 312–319. J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R.
- [4] S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," in *Nature Nanotechnology*, vol. 3, pp. 429–433, Jul. 2008.
- [5] Mohanty, Saraju P. "Memristor: from basics to deployment." *IEEE Potentials* 32.3 (2013): 34-39.
- [6] Z. Jiang et al. "Performance prediction of large-scale 1S1R resistive memory array using machine learning", in *Proc. IEEE Int. Memory Workshop (IMW)*, Monterey, CA, May 2015.
- [7] Defez, Emilio, et al. "Computing Hyperbolic Matrix Functions Using Orthogonal Matrix Polynomials." *Progress in Industrial Mathematics at ECMI 2012*. Springer, Cham, 2014. 403-407.
- [8] J. G. Simmons, "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film," in *J. Appl. Phys.*, vol. 34, no. 6, p. 1793, Jun. 1963.
- [9] D.B. Strukov, G. S. Snider, D. R. Stewart and R. S. Williams, "The missing memristor found," *Letter in Nature* 453, 80–83, May 2008
- [10] D. Pickett, et al. "Switching dynamics in titanium dioxide memristive devices" in *J. Appl. Phys.*, vol. 106, no. 7, pp. 1–6, Oct. 2009.
- [11] Z. Jiang and H. P. Wong, "Resistive-switching random access memory (RRAM) Verilog-A model," in *nanoHUB*, Oct. 2014.
- [12] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R.S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nat. Nanotechnol.*, vol. 3, pp. 429–433, Jun. 2008.
- [13] M. Laiho, E. Lehtonen, A. Russel, and P. Dudek, "Memristive synapses are becoming a reality," *Neuromorphic Eng.*, pp. 1–3, Nov. 2010.
- [14] C. Yakopcic, T. M. Taha, G. Subramanyam, R. E. Pino, and S. Rogers, "A memristor device model," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1436–1438, Oct. 2011.
- [15] E. Lehtonen and M. Laiho, "CNN using memristors for neighborhood connections," Feb. 2010, pp. 1–4.
- [16] T. Chang, S. H. Jo, K. H. Kim, P. Sheridan, S. Gaba, and W. Lu, "Synaptic behaviors and modeling of a metal oxide memristor device," *Appl. Phys. A*, vol. 102, no. 4, pp. 857–863, Feb. 2011.
- [17] Y. Shang, W. Fei, and H. Yu, "Analysis and modeling of internal state variables for dynamic effects of nonvolatile memory devices," in *Proc. IEEE TCAS*, vol. 59, no. 9, Sep. 2012, pp. 1906–1918.
- [18] I. S. Vourkas, "Memristor modelling," in *Memristor based Nanoelctronic Computing Circuits and Architectures*, 2006, pp. 9-28.
- [19] Radwan, Ahmed G., and Mohammed E. Fouda. On the mathematical modeling of memristor, memcapacitor, and meminductor. Vol. 26. New York: Springer, 2015.
- [20] B. Hajri, M. M. Mansour, A. Chehab and H. Aziza, "Oxide-based RRAM models for circuit designers: A comparative analysis," *2017 12th International Conference on Design & Technology of Integrated Systems In Nanoscale Era (DTIS)*, Palma de Mallorca, 2017, pp. 1-6.
- [21] N. S. Nedialkov, V. Kreinovich, and S. A. Starks, "Interval arithmetic, affine arithmetic, Taylor series methods: Why, what next?" in *Numerical Algorithms*, vol. 37, no. 1–4, pp. 325–336, 2004.