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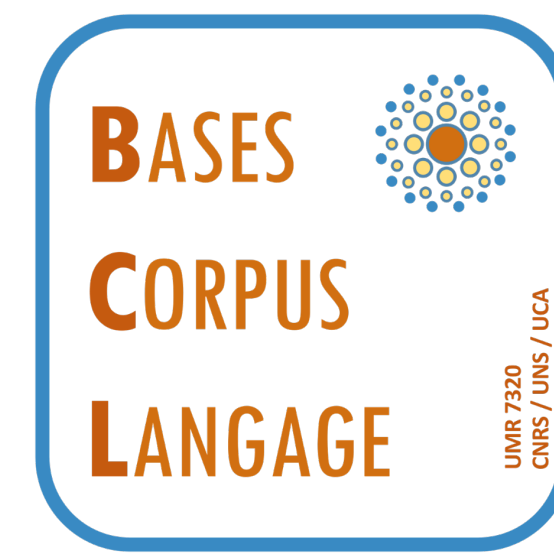
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Switching costs in verbal working memory complex span task performance



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#2301

Introduction

Switching between tasks induces a toll on the cognitive system (Monsell, 2003). Following the idea that complex span tasks require to switch between storage and processing activities and vice-versa, we examined in tasks of various level of difficulty if subtle variations of task structure could reveal switching costs associated to working memory (WM) performance.

Experimental manipulations

Task difficulty

- Task difficulty was manipulated by varying the cognitive load (CL) of the task at hand.
- CL is defined as the proportion of time during which a given task occupies attention preventing thus the maintenance of memory traces (Barrouillet et al., 2004).

Task structure

- Task structure was manipulated by varying the processing schedule of a complex span task.

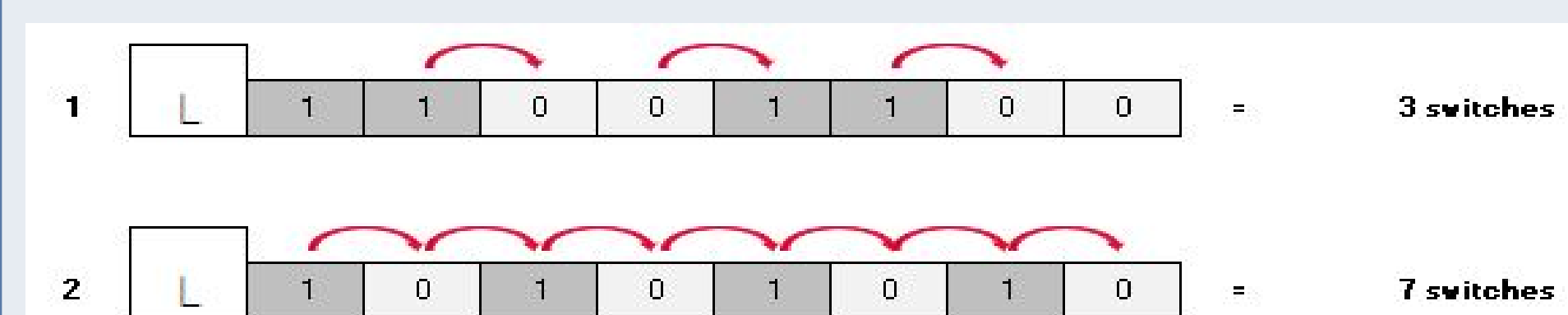


Figure 1: Processing schedules produced three vs. seven switches between storage and processing steps. Note: L stands for the storage item (letter), 1 for a processing step (digit) and 0 for a delay of free time allowing storage-maintenance activities to take place.

References

Barrouillet, P., Bernardin, S., & Camos, V. (2004). Time constraints and resource sharing in adults' working memory spans. *Journal of Experimental Psychology: General*, 133, 83–100.

Monsell, S. (2003). Task switching. *Trends in Cognitive Sciences*, 7, 134–140.

Experiment 1

Hypothesis - We expected to find reduced WM performance as a result of a high number of to-be-executed switches between storage and processing steps.

Participants & Method - 130 students performed a parity judgment span task requiring keyboard responses. Four levels of CL were created by varying the pace and the attentional capture of the task. Within each CL level, the processing schedule of the task was composed of either three or seven switches between storage and processing steps.

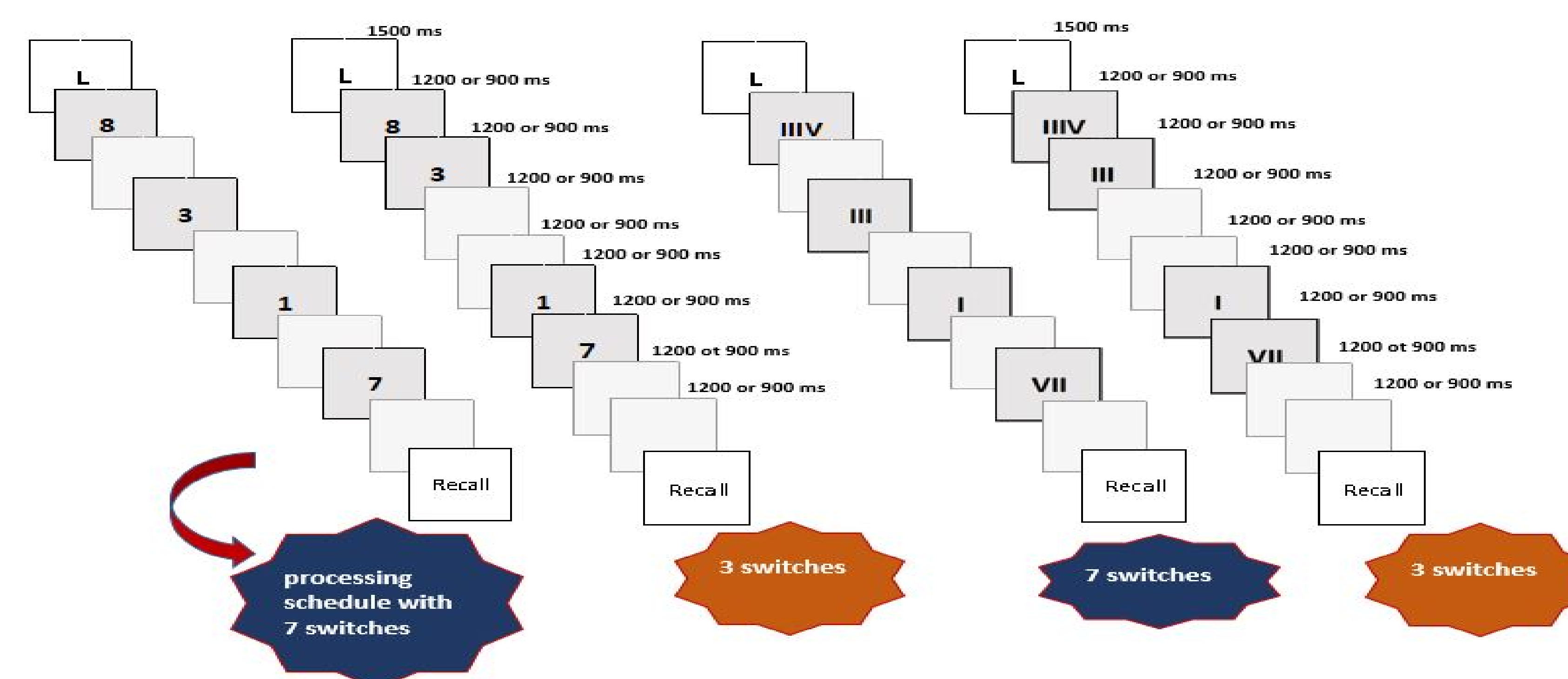


Figure 2: Parity judgment span task in Exp. 1 & 2. The pace of the task was either at 1200 ms or 900 ms (i.e slow or fast CL) for every distractor (digit) or free delay (blank screen). The attentional capture was manipulated by presenting digits in their Arabic or Roman form (i.e low or high CL). Experimental trials involved by construction three vs. seven switches between storage and processing steps. Note : Pace was a between-subject manipulation; attentional capture and number of switches were within-subject manipulations.

Results Exp. 1 & 2 (Recall)

In Exp. 1 when no verbalization was required, results showed no evidence in favor of switching costs in memory performance regardless of cognitive load of the task at hand. In contrast, in Exp. 2 when the concurrent task involved verbalization, a main effect of the number of switches on recall was found ($M_{3sw} = 0.67$, $ET = .33$; $M_{7sw} = 0.63$, $ET = .34$; $F(1, 4761) = 18.86$, $p < .001$). Akin to previous studies, both experiments found a main effect of CL on memory performance.

Experiment 2

Hypothesis - As in Experiment 1, we investigated the effect of switching between storage and processing activities on WM with different processing schedules.

Participants & Method - 134 students completed a parity judgment span task requiring oral responses. The material and procedure was identical to Experiment 1, except for the response types of the concurrent task (verbalization vs. no verbalization).

Figures Exp. 1 & 2

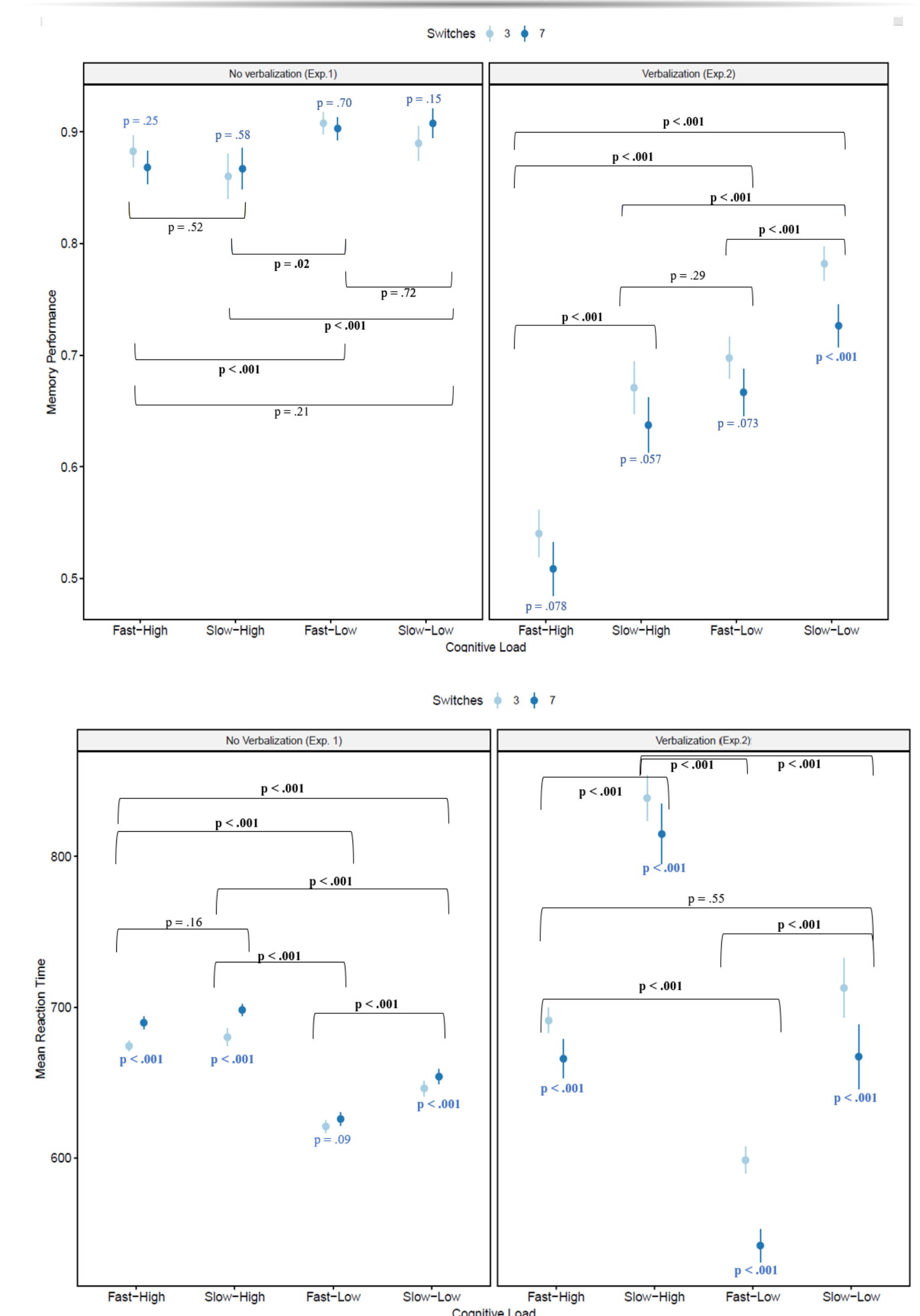


Figure 3: Mean memory performance (top figure) and mean RT of the concurrent task (bottom figure) as a function of CL and number of switches in Exp. 1 & 2. Note: CL= Fast-High: Roman numerals showed at 900 ms; Slow-High: Roman numerals at 1200 ms; Fast-Low: Arabic digits at 900 ms; Slow-Low: Arabic digits at 1200 ms.

Results Exp. 1 & 2 (RT)

In Exp. 1 requiring no verbal responses, concurrent task results showed slower (but more accurate) performance when the task involved a high number of switches to execute ($M_{RT3sw} = 655$ ms, $ET = 44$ ms; $M_{RT7sw} = 667$ ms, $ET = 45$ ms; $F(1, 5010) = 62.77$, $p < .001$). Exp. 2 indicated increased processing speed as a function of the number of the switches ($M_{RT3sw} = 708$ ms, $ET = 150$ ms; $M_{RT7sw} = 672$ ms, $ET = 173$ ms; $F(1, 4758) = 279.94$, $p < .001$).

Conclusion

Variations of the structure of the complex span task can induce slight variations of WM performance. However, the phenomenon appears to be sensitive to specific task designs. The finding of impaired memory performance as a function of our manipulation of switches in Exp. 2 could suggest that switch costs can occur (at least in some cases) independently of the attentional capture generated by the concurrent task.