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Experimental study of an EMI reduction gate-driver technique for turn-off transition of 1.7 kV SiC MOSFET

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Keywords

«EMC», «Gate-driver», «SiC MOSFET», «Soft-switching», «Converter»

Abstract

This paper proposes a novel self-controlled SiC MOSFET gate driver circuit. This new gate driver (GD) proposes a dynamic gate-bias modification thanks to a passive feedback of the drain or source current to control the EMI during turn-off switching transition. A Rogowski coil integrated into the terminals of the SiC MOSFET provides the feedback to modify the gate voltage profile. During turn-off, this circuit increases the voltage level of gate and consequently the gate current. This approach has a positive effect on the EMI behavior of converters without harmful effect on converter efficiency compared to the conventional method which consists in increasing the gate resistance. Moreover, with this approach, the gate driver design remains without modification (except the connection to the Rogowski coil) and there is no effect on turn-on transition of the SiC MOSFET. The proposed method is designed and developed for a 1.7kV SiC MOSFET and has been validated experimentally in an inductive double-pulse test platform. The proposed gate driver moderates the switching speed and is validated experimentally up to 1.2 kV 200A with the 1.7kV SiC MOSFET by reducing the common-mode current of turn-off transition.

1. Introduction

Wide bandgap devices require less gate charge to switch on or off and have overall better figures of merit than conventional Si devices [2]. They can be then used to improve the efficiency or density of power converters and power transistors based on GaN or SiC technologies are expected to represent a growing market in the next few years considering their decreasing price and excellent characteristics [1]. Therefore, research in these new technologies is of a great interest in the power electronic domain.

The lower level of gate charge of GaN and SiC devices leads to faster turn on/off transition which reduces switching losses but faster switching transition (di/dt and dv/dt) results in bigger electromagnetic interferences (EMI) which can disturb the operation of the converter itself and even the devices close by [2]. Several factors such as stray inductances in the layout, gate resistance (R_g) and parasitic capacitors of semiconductors have effect on EMI [3]. One of the solutions that can be applied

to mitigate the EMI is an individual switching transition modification which acts on di/dt and dv/dt . That can be done at the gate driver level, ie by acting on the gate voltage shape.

The most common way to overcome the EMI issue nowadays in power converters by means of switching modification is decreasing the switching slope by increasing the gate resistance. Therefore, to mitigate EMI, during switching, increasing the external R_g in gate drivers can change the driving signal and reduces the generated EMI by changing the current and voltage slopes across the switches. However, it increases the losses and decreases the efficiency. Finding the trade-off between EMI and power losses by new optimized driving techniques is the main motivation of research on gate driver designs nowadays.

Most of the times, switches are arranged as a pair of devices in a half-bridge configuration. In a half-bridge configuration of SiC MOSFETs (see Figure 1), during turn on/off transition of high-side switch, there is a voltage variation across the low-side switch which affects the C_{dg} parasitic capacitance of the device and creates a parasitic current [4] [5]. This current creates a gate-voltage perturbation due the parasitic impedance of the gate circuit. This parasitic voltage can lead to an unexpected switching of the low-side switch or device failure due to gate voltage perturbation. Therefore, a high value for the gate impedance during the off state is not an attractive solution. This adds some constraints to control the EMI by means of gate drivers and this should be considered in the design of gate drivers. Although it is possible to act on the level of EMI at turn-off by increasing the off-state gate resistance, it is not possible to increase it without also decreasing the switching speed for turn-on transition of the complementary switch in half-bridge devices (increasing R_g for turn-on) [5]. This shows another important aspect of controlling EMI during turn-off transition.

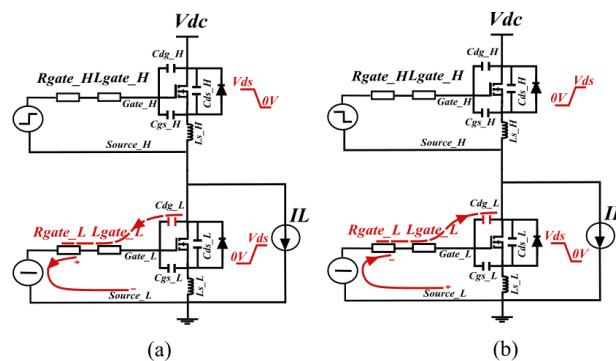


Figure 1: Complementary switching effect in half-bridge configuration (a) Turn-on (high-side) (b) Turn-off (high-side)

Active gate drivers (AGD) have been introduced recently to control the switching transition (di/dt and dv/dt) mostly for Si IGBTs [2]. AGD may be adapted to control the switching transition of SiC MOSFETs by driving the gate circuit in a feedback loop. The principle is to change the profile of the gate-source voltage when the current/voltage overshoot across the switch occurs. Reported research on AGDs for SiC MOSFET noticed a considerable delay in switching transitions using this technique which increases the switching losses [6]. For instance, an open loop AGD is presented in [3]. It acts on current rising/falling and voltage rising/falling subdivisions of the switching transition without any dynamic feedback to the controller of the gate driver. The switch-able gate resistances for controlling the gate current are implemented on a SiC MOSFET chip. The main drawback of this method is the considerable delay in turn-on transition which rises the losses level. A closed loop feedback gate driver is proposed for SiC MOSFETs in [7]. By means of two independent comparators, the gate-source voltage is compared to four reference voltages. Due to the fast switching of the SiC MOSFET, a delay compensator is implemented in the circuit. The complexity of the circuit lies in the current sensor, the generation of four references and the control of switching of different gate resistances. This gate driver results in a good trade-off between losses and EMI, but it has not been tested using a high voltage / high current power module. The current level required to turn-on the SiC MOSFET power module could be problematic with this gate driver. Another closed-loop gate driver for SiC MOSFET is presented in [7].

This gate driver successfully regulates the turn-on voltage and current slopes thanks to a voltage reference generator. Like in [3] this closed loop also suffers from the added delay to switching transition which is partially solved using a compensator circuit. It is stated in [7] that applying this control for both turn-on and turn-off imposes a considerable delay.

In [8] the concept of coupling between switching loop and power loop is used in the gate driver design to boost the gate current and modify the switching behavior. In this gate driver, only a current transformer is added to the circuit of the buck converter to transfer energy between the power path to the gate path while the design of the gate driver remains without modification. The proposed gate driver benefits from simpler design compared to the gate drivers described in [2] and [7]. This method has not been used to reduce the EMI and the implemented idea has not been tested for power modules. However, the proposed feedback in this work did not impose any delay to switching transition. A parametric study in [9] also has shown the effect of the mutual inductance between the switching loop and power loop. This work described experimentally that a negative coupling (which creates some negative voltage to be added to the gate-source voltage during turn-on to decrease the gate bias level) leads to a reasonable trade-off between losses and EMI because it decreases the current and voltage overshoot. These characteristics made it as a good choice to be studied for fast switching SiC MOSFET gate driver.

Another method which can help to deal with the EMI of the SiC MOSFET based converters is soft switching. These methods allow to reduce switching losses and can reduce the EMI issues as well [10]. Soft switching techniques that can be used in only certain applications. It can be in the form of zero-voltage switching (ZVS) and zero-current switching (ZCS) methods [11]. According to the application and soft switching method, the soft switching technique restricts the di/dt and dv/dt of switching transitions. However, in certain applications to achieve the soft switching, there is a need of extra components such as capacitance in parallel with the SiC MOSFET. Turn-on soft switching (ZVS) helps to reduce the EMI while turn-off transition is still a question in SiC MOSFET based converters [12]. Achieving soft switching for turn-off transition is not easy in SiC MOSFET based converters. It needs a considerable capacitance in parallel to the device while the effect of this capacitance on losses has not been investigated profoundly so as most of the soft switching conditions are applied only to the turn-on transition of the SiC MOSFETs.

Based on above introduction, the conventional method as increasing gate resistance during turn-off is not attractive to decrease the EMI of the converter since it increases the gate-source perturbation. Moreover, having soft switching without adding extra component is not achievable easily for turn-off transition of the SiC MOSFET. Therefore, this paper deals with reducing EMI created by SiC MOSFETs at turn-off transition. The current research work intends to present a gate driver able to reduce the EMI without changing the turn-on switching speed while proposing a better trade-off than conventional method with losses for a 1.7 kV SiC MOSFET power module (CAS300M17BM2 package). This gate driver can be used for SiC MOSFET based converters operating in ZVS conditions. The goal is to keep the conventional circuit of the gate driver and to integrate only a simple feedback to the gate driver circuit which makes a dynamic modification during fast switching. This feedback should be simple and easy to implement for different applications apart from the characteristics of the semiconductors. In addition, this method should not add any delay to the switching of SiC MOSFETs.

After the introduction, this work presents an inductive feedback gate driver concept at first. Then the expected results and the hardware implementation constraints are described. The platform for the tests and the experimental results are presented and discussed respectively. The paper ends with conclusion and perspectives.

2. Inductive feedback gate driver

2.1. Operation principles and Circuit configuration

The method presented in [8] is a current transformer which creates a voltage based on current variation to increase the gate current level and to increase the switching speed. Here, based on the study presented in [9] and to reduce the EMI due to hard-switching turn-off transition, the transformer is used to create

a voltage in series with the gate in a specific period and to smooth the gate current level (see Figure 2.a). This circuit using a current transformer with a feedback to the gate is called *inductive feedback gate driver*. So, during turn-off transition, an inductive feedback generates a voltage proportional to switching current variation (di/dt). This voltage is in series with the output stage of the gate driver (see Figure 2.b). The secondary of the current transformer is connected in the circuit with an orientation allowing to increase the gate voltage during turn-off transition. This gate voltage is regulated between +20 V (on state) and -6 V (off state). Thanks to the modified gate voltage profile, the drain-source voltage slope is smoothly slowed down. It is expected to have the modification presented in Figure 2.b to moderate the level of the voltage and current oscillations and that is how it allows to decrease the generated EMI. To apply this method, there should be a gate driver feature able to sense the current variation across the switch and change the gate voltage. This can be done by an embedded Rogowski coil to the gate driver (see Figure 2.a). The current transformer is implemented in this form (see Figure 2) to optimize its integration to the system.

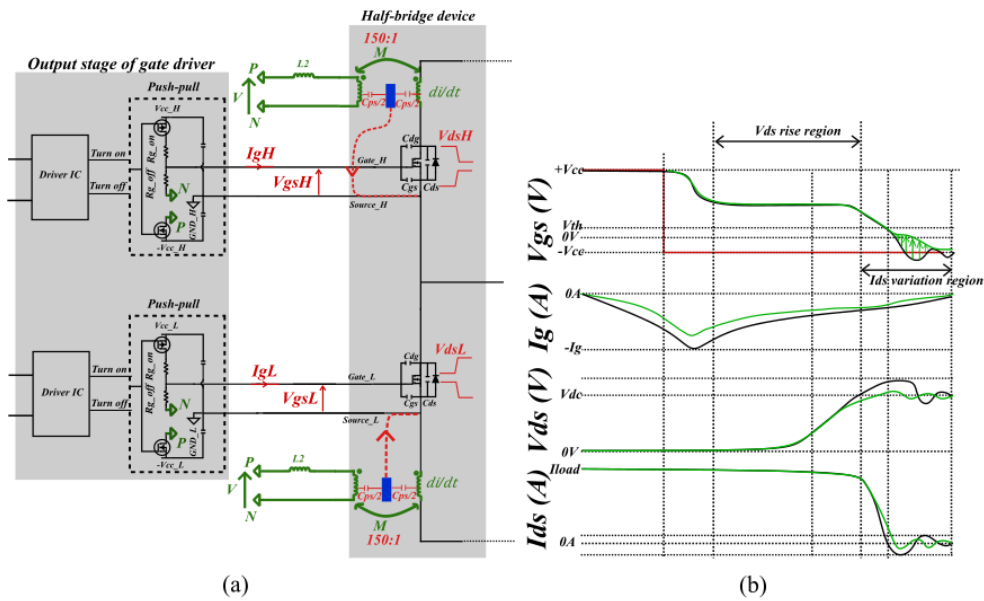


Figure 2: Proposed gate driver (a) Schematic of the proposed method implemented for half-bridge SiC MOSFET and half-bridge gate driver (b) Operation of gate driver in switching characteristics during turn-off transition (the effects of the inductive feedback are in green)

2.2. Hardware implementation

To design the Rogowski coil, the challenges are the physical integration and the minimization of parasitic elements, especially the parasitic inductance due to the installation of the coil into the gate circuit and its parasitic capacitor to use the Rogowski coil below its resonant frequency. A classical equivalent circuit model of the Rogowski coil (see Figure 3.a) consists of two inductors $L1$ and $L2$. The primary side $L1$ corresponds to the terminal of the device under test (see Figure 3.b). Since it is planned to integrate the coil on the top of the device, for the primary side $L1$, only the value of the terminal inductance is considered. Moreover, like this, there is no added parasitic component to the power loop due to the integration of the Rogowski coil to the power circuit. Compared to the power loop circuit parasitic inductance (physical connection of the device into layout of the converter), the impedance of the terminal of the device is very small (about 10nH). The critical points in integrating the Rogowski coil to gate circuit are the added parasitic inductance which should be as low as possible (The secondary side $L2$ will be placed in the gate path (see Figure 2)) and the mutual inductance which should have a high enough value (to provide the expect effect). It can be optimized by proper design of the Rogowski coil and a proper type of winding. To do so, based on previous research on core-less Rogowski coils [13] and [14] where the current is not completely perpendicular to the Rogowski coil (as the case here) a “return wire compensated winding” type has been selected (see Figure 3.c) [13]. This winding has been chosen due to its lower impedance and better immunity to noise. To achieve the proper mutual inductance, the number of turns in the secondary should be high enough compared to that of the primary. Therefore, a single turn to sense the current and maximum possible turns in secondary leads to increase

the mutual inductance (see Figure 3.c). To increase the number of turns in the secondary, the smallest via size and PCB track with the width of 0.2mm have been chosen. With the 6-layer PCB, a Rogowski coil with 150 turns on the secondary has been manufactured to be implemented on the top of the device. The design integrates two Rogowski coils into a half-bridge power module to sense the current of low-side and high-side switch. Then the coils are implemented in a half-bridge power module gate driver. The coil is implemented on the terminals of the power module, where the voltage is changing at 30 kV/ μ s in this work ($R_g=0.2\Omega$). The parasitic capacitance between the primary inductor and secondary winding (C_{ps} in Figure 3.a) of the coil provides a coupling path for this voltage variation across the switch ($C_P \frac{dv}{dt}$). To overcome this problem, the PCB Rogowski coil has been shielded by two PCB layers on top and bottom layers of the coils (see Figure 3.d). The shield layers have been connected to the source of each switch in the half-bridge device (see Figure 2.a).

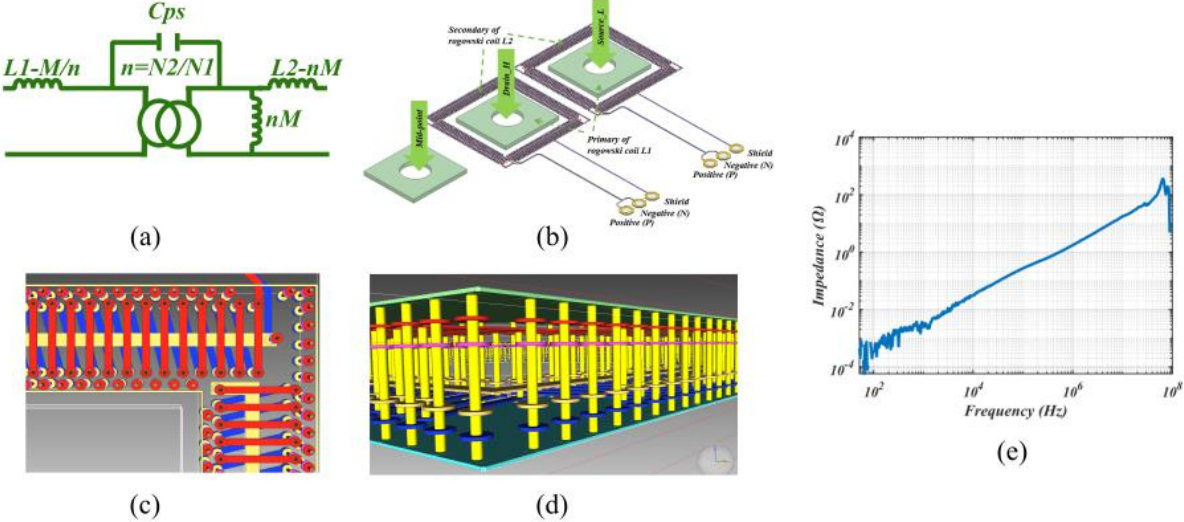


Figure 3: Embedded Rogowski coil (a) Equivalent circuit (b) Implementation of the Rogowski coil on the top of the power module (c) side cross section of the PCB Rogowski (d) front cross section of the PCB Rogowski (e) Impedance measurement of the PCB Rogowski

The impedance of the manufactured PCB (see Figure 3.e) was measured by impedance meter (The measurement between N and P in Figure 3.b). The maximum rise/fall time of the SiC MOSFET current is expected to be 40ns (corresponds to the frequency range up to 9 MHz). It means that the Rogowski coil should presents an inductive behavior in this frequency range to creates a voltage. Moreover, it can be seen in Figure 3.e that the main components of the current signal are then at frequencies lower than the frequency of the first resonance (64MHz) of the manufactured coil which assures the performance of the coil.

2.3.Gate driver with integrated Rogowski coil

The implemented coil integrated to the circuit of the gate driver is shown in Figure 4 on the top of the 1.7kV SiC MOSFET. The proposed gate driver has been evaluated experimentally in double pulse test platform in different current levels.

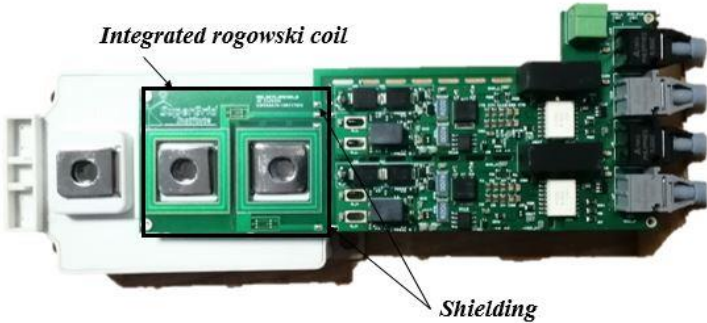


Figure 4: Gate driver prototype with embedded Rogowski coil

3. Experimental validation

3.1. Test bench

To investigate the performance of the gate driver and switching characteristics, the experimental study has been carried out on a full-bridge double-pulse test bench (see Figure 5.a where only the half-bridge under test is represented). In this test bench, it is possible to control the direction of the current through the inductor which enables to characterize the high-side and low-side switches of the half-bridge device under test (DUT) in soft switching and hard switching conditions.

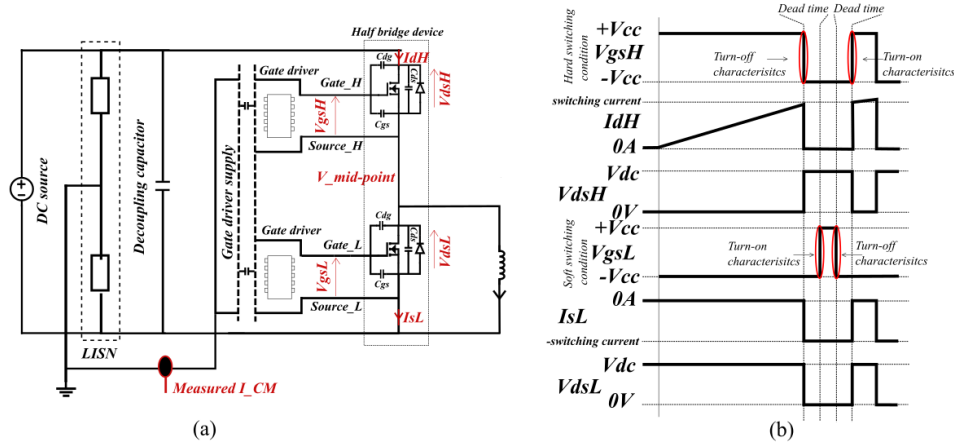


Figure 5: Double-pulse method (a) Circuit (b) Switching waveform

This study is focused on the hard switching of the high-side switch while the low-side switch commutates in soft switching condition (see Figure 5.b). All the design characteristics are the same for the low-side switch. In a double pulse test, by turning-on the high side switch, the inductance is charged until a certain level of the current, then the first pulse highlights the turn-off behavior of high-side switch in hard switching condition. Then, the second pulse is the turn-on transition of the MOSFET in a specific voltage and current (see Figure 5.b).

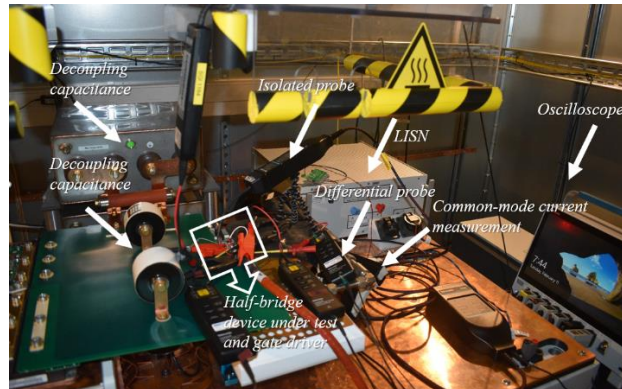


Figure 6: Double pulse test platform

Characterizing the performance of the high-side switch in half-bridge configuration is challenging because of the variation of mid-point voltage (see Figure 5.a) [15]. In this experimental work, high frequency oscilloscope and optical voltage probe were used.

3.2. Rogowski coil

The PCB Rogowski coil has been tested in different current levels in double pulse test (see Figure 7). It is shown that during turn-off, the current slope (di/dt) is changing based on the current level, therefore, the voltage at the output of the coil is changing also ($V_{(N-P)}$ in Figure 2.a). This assures that the coil can inject the voltage and change the gate bias in different current levels and modify the switching transition of the device.

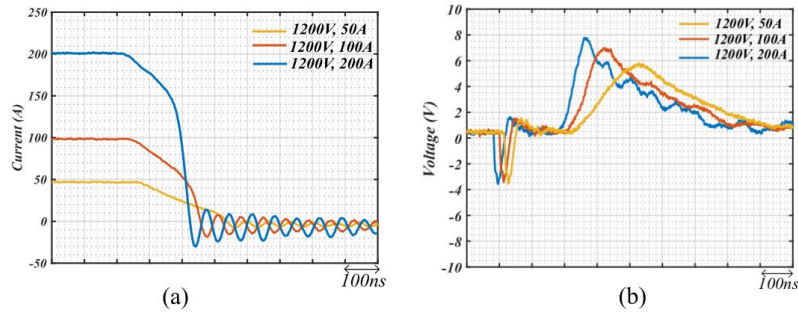


Figure 7: Performance of the Rogowski coil in different current levels during turn-off transition (a) Experimental drain current measurement (b) Voltage at the output of the Rogowski coil when it is not connected to the gate circuit

3.3. Gate driver performance

Figure 8 shows a comparison of V_{gs} waveforms with and without integrated Rogowski coil. As it is shown in Figure 5.b, during switching transition of high-side switch, the first pulse shows the hard-switching turn-off. In Figure 8, it is shown that when the switch current is decreasing, the generated voltage at the output of the Rogowski coil is added to the negative bias of the gate-source voltage and the Rogowski coil feedback is acting. Moreover, it is shown, that the added coil does not change the turn-on transition.

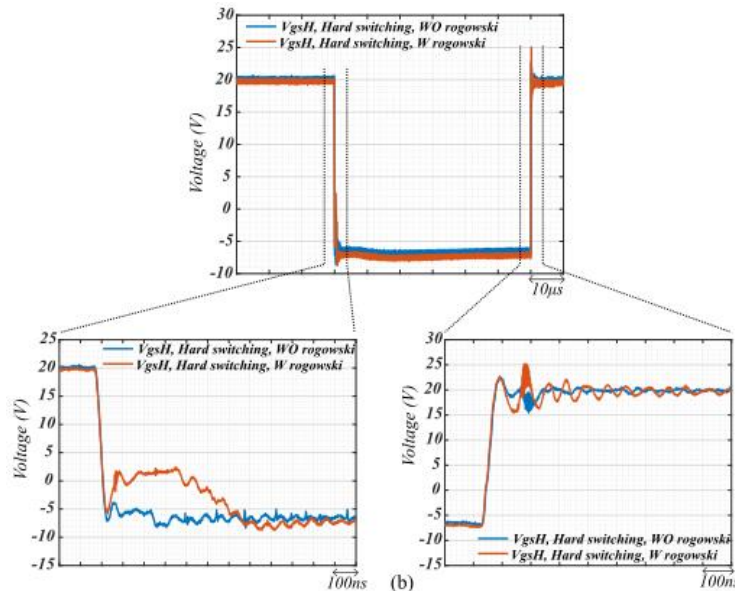


Figure 8: Experimental gate driver performance with (W) and without (WO) integrated Rogowski coil at 200A, 1200V, gate-source voltage comparison W and WO Rogowski coil

Following the gate-source voltage modification in hard switching condition, the waveforms of the switch (see Figure 9) depict a moderate slope of the current and voltage. The reduction in the amplitude of the oscillations is due to the added inductor in push-pull path which slightly changes the waveforms (see Figure 2.a). The switching waveforms of the uncontrolled switch (low-side switch) are the projections of the high-side switch since it is not controlled. Therefore, the same waveforms will be applied to the low-side switch as well. Thanks to these moderate switching slopes, the generated CM current passing through the gate driver (see the measurement point in Figure 5.a) is reduced by 40% in peak-to-peak value (see Figure 10). The implemented coil has not significantly changed the turn-on transition which can be seen in Figure 9.b. The oscillation has been changed due to the changes in the resonance circuit elements.

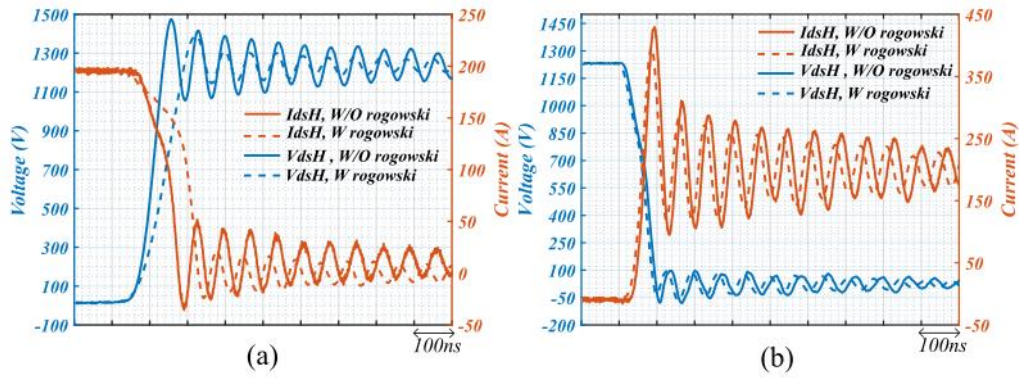


Figure 9: Experimental gate driver performance with (W) and without (WO) integrated Rogowski coil at 200A, 1200V (a) V_{dsH} and I_{dsH} during Turn-off transition (b) V_{dsH} and I_{dsH} during Turn-on transition

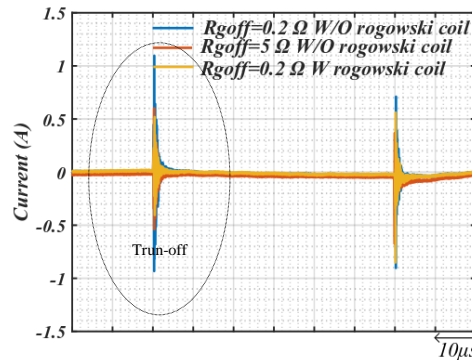


Figure 10: Experimental common-mode current comparison With (W) and Without (WO) integrated coil at 200A, 1200V and different R_{goff}

4. Trade-off comparison between the proposed method and classical increasing gate resistance

To evaluate the proposed method in terms of losses compared to conventional increasing gate resistance method, the gate resistance has been increased such that the input CM current reduction is the same as with the Rogowski coil (Figure 10). This was achieved by increasing the gate resistance (for turn-off) from 0.2Ω to 5Ω .

Experimental comparison between the current and voltage switching waveforms shown in Figure 11, illustrates that by increasing the gate resistance to achieve the same amount of CM current reduction, the switching slope is more reduced than with the Rogowski coil method. It results in increasing switching losses compared to proposed method in this work.

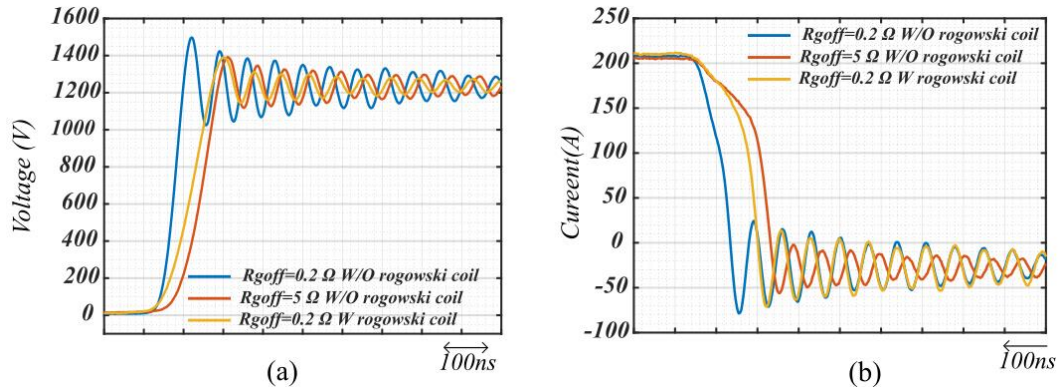


Figure 11: Experimental comparison of the performance of the gate driver with (W) Rogowski coil and conventional method Without (WO) Rogowski coil by increasing R_g at 200A, 1200V (a) V_{dsH} (b) I_{dsH}

The gate driver prototype has been tested in different levels of current where the Rogowski coil creates different voltages in the gate path. A comparison of switching losses during turn-off transition with two methods has been done. In *Figure 12* the difference between losses during turn-off is depicted in different levels of the current. The proposed gate driver outperforms the conventional approach by reducing losses up to 20% with a similar EMI reduction. Another important point that must be considered is the complementary switching effect in half bridge configuration explained in introduction section (see *Figure 1*). As it has been explained, during these measurements, only R_{goff} has been increased while keeping R_{gon} equal to 0.2Ω , the turn-on switching speed has not been changed. Looking into experimental results shown in *Figure 13*, it can be seen that, by increasing R_{goff} , the disturbance on low-side gate voltage is exacerbated when the high-side switch turns-on [5].

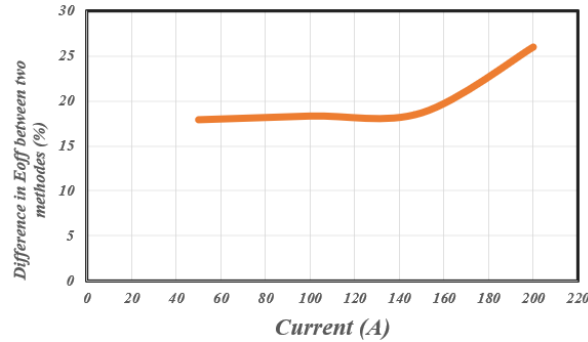


Figure 12: Experimental comparison of the performance of the gate driver with (W) Rogowski coil and conventional method Without (WO) Rogowski coil at 1200V and different current levels

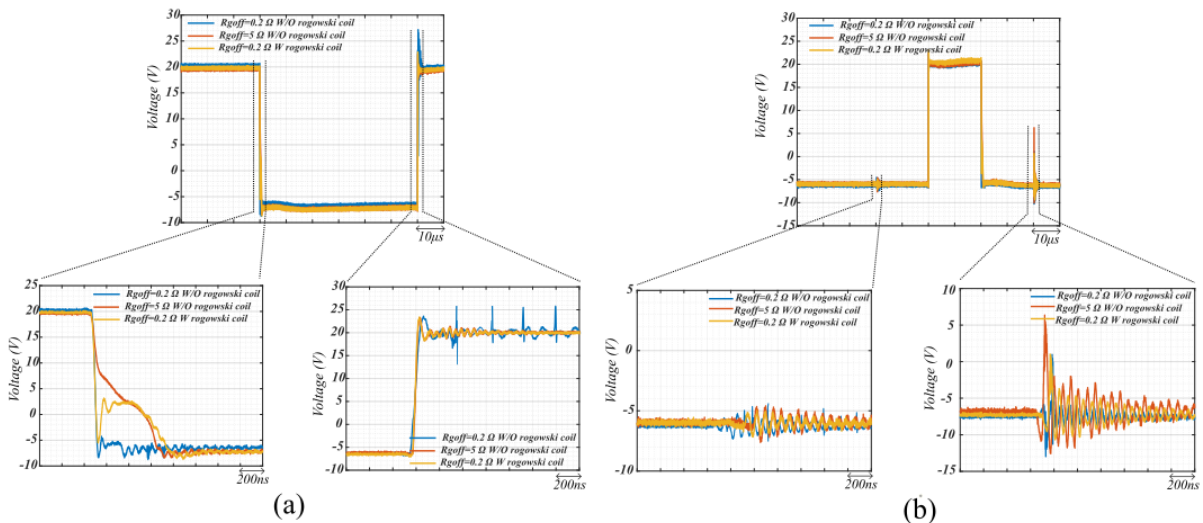


Figure 13: Experimental comparison of the Vgs waveform with (W) Rogowski coil and conventional method Without (WO) Rogowski coil at 200A, 1200V (a) VgsH (hard-switching) (b) VgsL(soft-switching)

5. Conclusion

This work presents a new method to control turn-off switching process of 1.7 kV SiC MOSFET gate driver. The inductive feedback gate-driver, thanks to a simple feedback from drain/source current to the gate, induces a positive voltage during turn-off, thereby reduces the gate current during a short period. This gate current reduction moderates the switching slope and voltage/current switching oscillations. This is validated experimentally up to 1.2kV and 200A. The new method reduces the input CM current of the gate driver. Decreasing the input CM current decreases the risk of self-disturbance in the operation of the converter. Thanks to this new technique, achieving better efficiency is feasible compared to the conventional method and there is a lower risk of gate perturbation. In comparison with reviewed approaches for active SiC MOSFET gate driver, the proposed feedback has not imposed any delay in

switching transition of the SiC MOSFET. This makes the proposed gate driver a relevant choice for ZVS SiC MOSFET based converters where hard-switching turn-off is happening.

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