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Keywords

«Power flow control», «HVDC», «Multi-terminal HVDC», «DC-DC power converter», «Design»

Abstract

Power flow controllers (PFC) or current flow controllers (CFC) are expected to be required in future HVDC grids to control the current flows and avoid congestions. This work proposes a methodology to obtain the specifications, select the most suitable converter structure and perform the sizing of an interline PFC. Then, the methodology is applied to a real HVDC grid case study, obtaining the specifications, the selected converter structure and the sizing of the power electronic elements and the passive components. The results show that the PFC is a medium voltage converter with high current rating requiring some switches in series and interleaved branches. With such a series/parallel association, the main elements of the converter are available on the market except for the inductances which can be manufactured on-demand without major technical locks.

Introduction

Meshed HVDC grids can facilitate the integration of distant renewable power sources and increase the flexibility of the grid, but they also pose several challenges regarding their operation and control [1]. A major concern is the power flow control within the grid, since the HVDC converters at the nodes cannot control independently the currents circulating inside the mesh (they depend on the line resistance relation). This can lead to overloads in certain lines, restricting the overall power transmission [2].

In order to face this challenge, additional devices must be introduced in the meshed HVDC grid to provide additional degrees of freedom to control the current flows [2]. These devices are based on power electronics and are named power flow controllers (PFC) or current flow controllers (CFC), which are the equivalent of flexible AC transmission systems (FACTS) but applied to DC grids. Several different proposals of these devices can be found in the literature: series switching resistors [3], full power converters connected between poles [3] and variable voltage sources inserted in series with one line or with several lines [4]. In the literature, those PFCs are introduced with electric diagrams illustrating their control and operation. They are validated through simulations or in scaled-down prototypes tested in laboratory [5]. However, to the best knowledge of the authors, there is no work where the specifications of such a device are obtained and then no example for the sizing of such a converter is given. The feasibility of the PFCs is then questionable.

This paper presents the methodology to obtain the specifications of a PFC, select the most convenient converter structure and perform the sizing of the converter, considering the passive components

(inductors and capacitors), IGBTs and diodes. The sizing process is based on selecting, as much as possible, existing devices from manufacture datasheets to investigate the PFC feasibility. It is applied to a case study in Zhangbei HVDC grid, where a PFC is introduced to avoid the overloads caused by an hypothetical converter station upgrade. The considered PFC is the interline topology proposed in [6], which inserts series voltages between two different lines. It has the advantages of a simple structure and at the same time it applies filtered voltages in series with both lines to control the current.

Methodology

This section presents the methodology to obtain the specifications of the PFC, the selection of the most convenient converter structure and the sizing of the selected PFC converter.

Specifications of the power flow controller

In this work, it is assumed that a power upgrade is needed in a converter station of a meshed HVDC grid, while maintaining the existing lines (they are not upgraded, keeping the same current rating than in the initial case). Due to the power upgrade, new current flows will circulate through the HVDC grid, which can exceed the current rating of the lines. Those lines with lower resistance may be susceptible to be overloaded in this new situation since the voltage source converter (VSC) stations cannot control independently the currents within the mesh. Instead of upgrading the overloaded lines, this work considers the installation of a PFC in one node of the HVDC grid in order to add an additional degree of freedom to regulate the current flows. By inserting voltages in series with the lines, the PFC can redirect the current of the overloaded line into an underused line ensuring the nominal power transmission. Fig. 1 illustrates a generic meshed HVDC grid after a power upgrade of one of the converter stations (S_I) and the installation of a PFC (S_N).

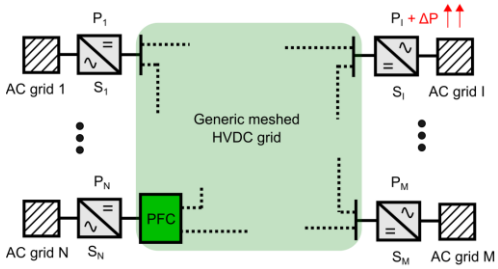

Fig. 1. HVDC grid after a power upgrade in a converter station and the installation of a PFC in a generic node.

In order to obtain the voltages that the PFC must apply and its current constraints, the system is modelled as an Optimal Power Flow (OPF) problem [7], where the objective function consists in minimizing the losses. The PFC is modelled as two equivalent voltage sources [5] that can be placed at any node. Fig. 2 shows different PFC models depending on how the voltage sources are placed on the corresponding node. A constraint to guarantee the PFC power balance must be introduced in order to ensure that the power extracted by one of the voltage sources of the PFC is injected by the other voltage source. The previous equation is also illustrated in Fig. 2 for each PFC model.

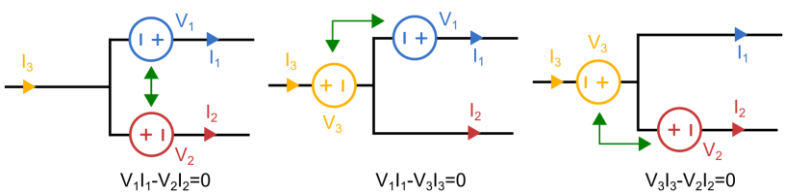

Fig. 2. PFC models based on the topology in [6] and used in the OPF problem formulation. Note that a node with three possible connections is shown here as an example.

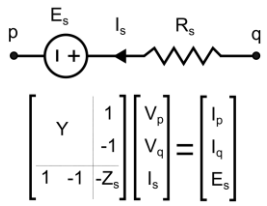

Fig. 3. Generic voltage source model and implementation of the MNA load flow.

A Modified Nodal Analysis (MNA) load flow method [8] is used to generically integrate PFC voltage sources into the mathematical formulation of the OPF problem irrespectively of the number of network nodes. Fig. 3 presents a generic voltage source and the mathematical implementation of the MNA load flow method between two generic nodes p and q. By implementing two of these voltage sources and the power balance equation, the PFC can effectively be included in the OPF problem.

The implemented approach performs a power sweep of the converter stations (from $-P_1$ to P_1 with a given power step) starting for converter station S_1 and doing it for all the converter stations up to S_M. Then, for each possible operating point, the OPF problem is solved and if one of the lines of the HVDC grid exceeds the maximum current, one of the PFC models in Fig. 2 is included. In those cases, the output of the OPF problem provides the voltages V_1, V_2, V_3 (gathered in pairs) that the PFC must apply to prevent the overload in the corresponding line considering the different models in Fig. 2. The currents that circulate through the PFC (I_1, I_2 and I_3) are also obtained. It is important to notice that a vector of values for each magnitude (V_1, V_2, V_3, I_1, I_2 and I_3) is obtained for each PFC model, in which each value of the vector corresponds to an operating point where the PFC is required. The previous procedure is repeated assuming the models in Fig. 2 are implemented in any node of the HVDC grid in order to find the PFC specifications for different locations (this will allow to find the optimum location where to install the converter). With those values for each PFC model and node, it is possible to proceed to the next step, the selection of the most convenient PFC structure.

Selection of the most convenient PFC structure

Step 1: Comparing the PFC structures at node level and selecting one

In order to translate the previous voltages (V_1, V_2, V_3) and currents (I_1, I_2 and I_3) obtained in the OPF problem into requirements for switches and passive components, a PFC topology compatible with the previous representation of the device (see Fig. 2) must be selected. The base PFC topology introduced in [6] has been chosen for this work. However, depending on the polarity of the voltage sources and the direction of the DC currents, different converter structures of the chosen PFC topology are needed to implement the device and their elements will require to withstand/conduct different voltages and currents. In Fig. 4, three possible PFC models and their corresponding converter structures are shown. It is important to notice that if the voltage sources are located in the lines where the two currents are circulating in the same direction (see Fig. 4(a)), the PFC structure becomes simpler.

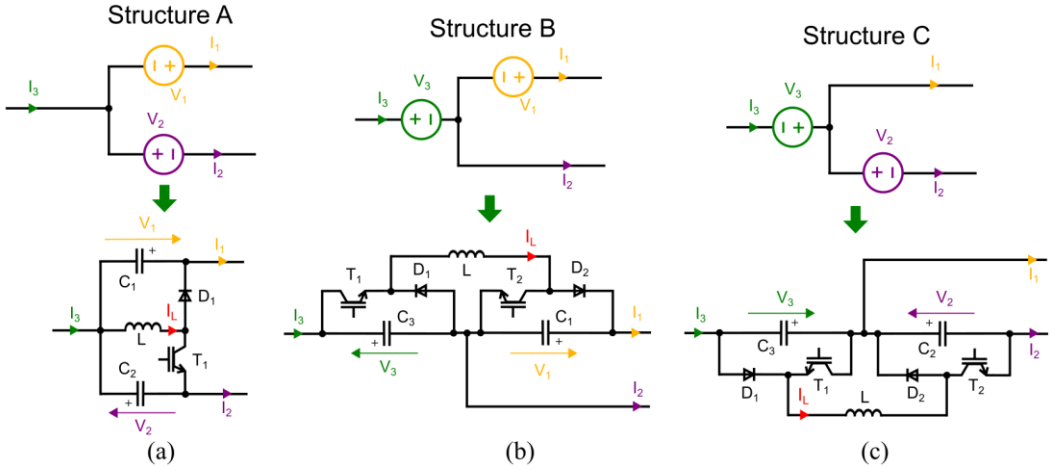

Fig. 4. Three possible PFC models with their corresponding converter structures.

This section illustrates the methodology for the three structures in Fig. 4 (with the same current directions). However, in case of having different current directions, which would be the case when the PFC is installed in another node, the orientation of the IGBTs and diodes may change and thus, the expressions to obtain the voltage and current of the PFC elements.

The PFC converter structures shown in Fig. 4 are unidirectional in terms of current and voltage, meaning that the capacitors cannot change their polarity and the currents cannot reverse. They are controlled by sending pulses to the IGBT (the same pulses for both IGBTs in Fig. 4(b) and Fig. 4(c)) with a certain duty cycle α_{igbt}. This duty cycle α_{igbt} corresponds to the time that the IGBT (or IGBTs) is in conduction mode, equal to t_{igbt}, divided by the total period T. The duty cycle of the diode (or diodes) can be defined as $\alpha_d=(1-\alpha_{igbt})$ and is illustrated in (1) for the PFC structure A; in (2) for the PFC structure B; and in (3) for the PFC structure C:

$$\alpha_d^A = (1 - \alpha_{igbt}^A) = \frac{t_{diode\_A}}{T} = \frac{V_2}{V_1+V_2} \quad (1)$$

$$\alpha_d^B = (1 - \alpha_{igbt}^B) = \frac{t_{diode\_B}}{T} = \frac{V_3}{V_1+V_3} \quad (2)$$

$$\alpha_d^C = (1 - \alpha_{igbt}^C) = \frac{t_{diode\_C}}{T} = \frac{V_2}{V_2+V_3} \quad (3)$$

The previous expressions are obtained after imposing that the average voltage in the inductor must be equal to 0. Knowing the duty cycle of each structure, it is possible to obtain the maximum value of current and voltage waveforms in each element of the PFC (without considering the ripple due to the passive components), whose expressions are illustrated in Table I.

Table I. Voltage and current constraints for the PFC structures A, B and C

	Structure A		Structure B		Structure C	
	Voltage	Current	Voltage	Current	Voltage	Current
Inductor L	$max(V_1,V_2)$	I_3	$max(V_1,V_3)$	I_1/α_d^B	$max(V_2,V_3)$	I_3/α_d^C
Capacitor C_1	V_1	$max(I_1,I_2)$	V_1	$max(I_1,I_1/\alpha_d^B-I_1)$	-	-
Capacitor C_2	V_2	$max(I_1,I_2)$	-	-	V_2	$max(I_2,I_3/\alpha_d^C-I_2)$
Capacitor C_3	-	-	V_3	$max(I_3,I_1/\alpha_d^B-I_3)$	V_3	$max(I_3,I_3/\alpha_d^C-I_3)$
IGBT T_1	V_1+V_2	I_3	V_3	I_1/α_d^B	V_3	I_3/α_d^C
Diode D_1	V_1+V_2	I_3	V_3	I_1/α_d^B	V_3	I_3/α_d^C
IGBT T_2	-	-	V_1	I_1/α_d^B	V_2	I_3/α_d^C
Diode D_2	-	-	V_1	I_1/α_d^B	V_2	I_3/α_d^C

Then, the expressions in Table I allow to calculate the voltage and current of each PFC element (IGBTs, diodes, capacitors and inductor) for each operating point. After, the maximum current and voltage of each element are used for the comparison between PFC structures A, B and C (in Fig. 4). In this first step, the PFC structure with the lowest values of voltage and current among the structures A, B and C is selected. The previous process is repeated for the number of nodes M of the HVDC grid (nodes where the PFC can be installed, in which different PFC structures are possible). Fig. 5 presents the different steps for the selection of the most convenient PFC structure and location.

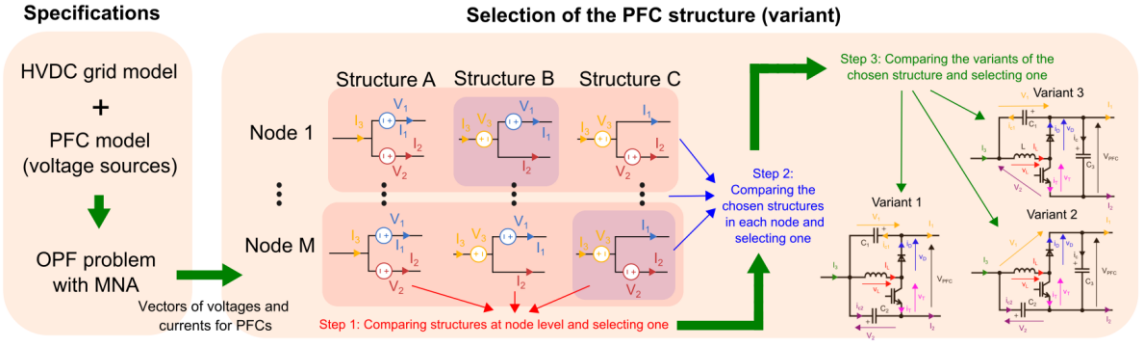

Fig. 5. Procedure describing the obtention of the specifications of the PFC, the selection of its location and the structure/variant to be used in the sizing.

Step 2: Comparing the selected PFC structures for each node and choosing one

A number M of PFC structures are compared at step 2. The calculation of the energy of the capacitors and the inductors is included in the analysis to aid in the selection since the voltage and current ratings of the PFC elements may not be enough to take a decision. Also, the energy in passive components is highly related to their size and these components are expected to represent a significant part of the PFC volume. The capacitances and inductance are calculated based on the maximum allowed voltage ripple in the capacitors and maximum allowed current ripple in the inductor, respectively. Then, the structure in the node that has a lower value of energy (sum of capacitors' and inductor's energy) is selected. Structure A in Fig. 4 is used as an example to explain the methodology and show the used expressions.

The maximum allowed current ripple in the inductor (ΔI_L^{max}) is defined as a percentage (ΔI_L^{pu}) of the maximum inductor current in all the operating points (I_L^{max}). For structure A, the current through the

inductor corresponds to I_3 as shown in Table I. With the previous current ripple, the inductance of the PFC structure A can be calculated as follows:

$$L = \frac{\alpha_d(1-\alpha_d)(V_1+V_2)}{f\,\Delta I_L^{max}} = \frac{\alpha_d(1-\alpha_d)(V_1+V_2)}{f\,\Delta I_L^{pu} I_L^{max}} \quad (4)$$

where, f is the switching frequency of the PFC structure.
A value of L is obtained for each operating point and then the maximum of all of them is selected (L^{max}). With L^{max} and I_L^{max}, the maximum energy of the inductor is calculated as follows:

$$E_L^{max} = \frac{1}{2} L^{max} (I_L^{max})^2 \quad (5)$$

The process to calculate the energy of the capacitors C_1 and C_2 is analogous and the expressions for C_1 are shown in (6)-(7) (the process for C_2 is the same as for C_1). The maximum allowed voltage ripples in the capacitors (ΔV_{C1}^{max}, ΔV_{C2}^{max}) are defined as a percentage (ΔV_{C1}^{pu}, ΔV_{C2}^{pu}) of the maximum voltages in the capacitors (V_{C1}^{max}, V_{C2}^{max}), which correspond to the maximum voltages V_1 and V_2 from all the operating points, respectively.

$$C_1 = \frac{\alpha_d(1-\alpha_d)I_3}{f\,\Delta V_{C1}^{max}} = \frac{\alpha_d(1-\alpha_d)I_3}{f\,\Delta V_{C1}^{pu} V_{C1}^{max}} \quad (6)$$

$$E_{C1}^{max} = \frac{1}{2} C_1^{max} (V_{C1}^{max})^2 \quad (7)$$

After that, the PFC structure with the lowest value of energy of the passive components is selected.

Step 3: Comparing variants of the same PFC structure and selecting one

A single PFC structure has been selected and a node has been identified where to install the PFC. However, the chosen topology allows a certain flexibility in terms of the location of the capacitors (three possible arrangements can be considered). The word variant is used to identify the different arrangements of capacitors for a certain PFC structure, which are shown in Fig. 6 for PFC structure A.

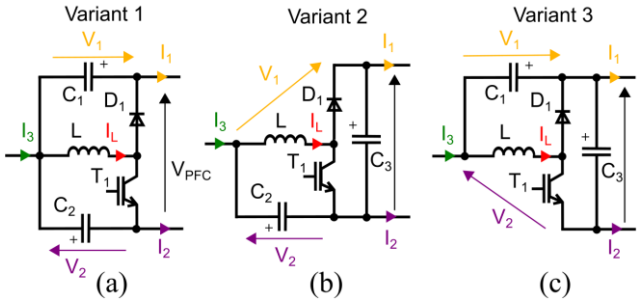

Fig. 6. Three possible variants for the PFC structure A.

Table II. Expressions to calculate the required capacitance for each variant

	Variant 1	Variant 2	Variant 3
C_1	$\frac{\alpha_d(1-\alpha_d)I_3}{f\,\Delta V_{C1}^{max}}$	-	$\frac{\Delta I_L}{8\,f\,\Delta V_{C1}^{max}}$
C_2	$\frac{\alpha_d(1-\alpha_d)I_3}{f\,\Delta V_{C2}^{max}}$	$\frac{\Delta I_L}{8\,f\,\Delta V_{C2}^{max}}$	-
C_3	-	$\frac{\alpha_d(1-\alpha_d)I_3}{f\,\Delta V_{C3}^{max}}$	$\frac{\alpha_d(1-\alpha_d)I_3}{f\,\Delta V_{C3}^{max}}$

The variants are operated in the same way than the original structure. However, the current and voltage waveforms, that the capacitors see, are different for each variant, leading to different requirements for the capacitors. Since the ratings of the inductor, IGBTs and diodes are not modified within variants, the selection of the most convenient variant is based on the energy of the capacitors. Table II depicts the expressions to calculate the capacitance according to the same voltage requirement explained in Step 2. It can be noticed that the expressions for C_2 in variant 2 and C_1 for variant 3 are different from the previous ones and they depend on the current ripple in the inductor (ΔI_L). This work selects the variant with the lowest value of energy in the capacitors. Other possible criteria could be selecting the variant with the minimum capacitor RMS current, minimum capacitor RMS current/capacitance, etc.

Sizing of the selected PFC structure/variant

Once the PFC structure and variant is selected, the sizing of the power electronic components of the PFC (IGBTs, diodes, inductor and capacitors) is performed for normal operation. The additional components as bypass switches, protection equipment, cooling system and control systems are not analyzed here, but their technical feasibility has been discussed in [9]. Fig. 7 presents the inputs and main outputs of the sizing process. For the sake of simplicity, only the expressions for the PFC structure A Variant 3 are presented in the following sections.

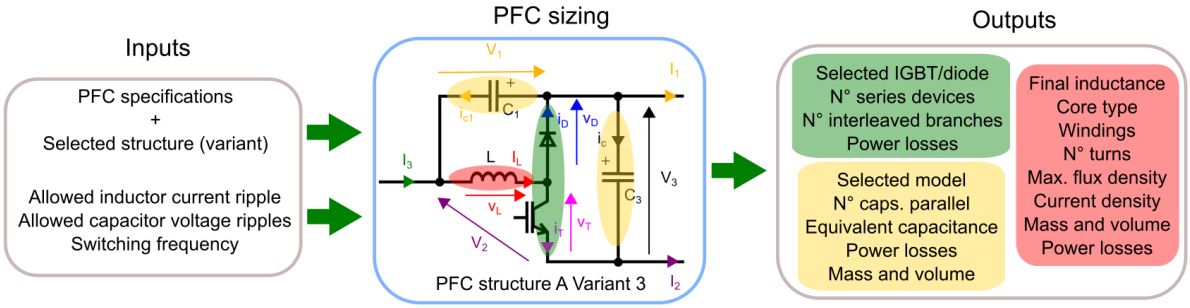

Fig. 7. Diagram of the sizing process, illustrating the required inputs and the main outputs.

Diodes+IGBTs/IGCTs

Regarding the switches, a database of several press pack IGBTs and IGCTs are considered as candidates to implement the self-commutating devices, according to the current and voltage specifications. A database of diodes is also used, where each diode is associated to a certain IGBT or IGCT with similar ratings, meaning that selecting the latter implies the selection of the corresponding diode. Table III depicts the IGBTs, IGCTs and the associated diodes (in the same row) considered in the database.
In case of requiring a higher blocking voltage than the available devices in the database, the series connection of devices is considered. Similarly, if the current specification is higher than the current rating of the available devices, interleaved branches will be added into the converter to deal with the required current. The IGBT or IGCT to be used in the PFC is selected based on the following criteria:

1. Minimum number of devices in series
2. Minimum number of interleaved branches (in case of the same number of devices in series)
3. Lower index in Table III (in case of the same number of interleaved branches)

For the IGCTs, the additional circuit to limit the di/dt when turning ON is not included in the sizing. Also, for the IGCT, the switching frequency is not defined as an input but an internal variable. It is obtained as the maximum switching frequency at which the IGCT is able to interrupt the current of the PFC specifications (max. turn-off current based on the data of the datasheet).

Table III. IGBTs, IGCTs and diodes considered in the database

IGBTs	4.5 kV 2 kA (5SNA 2000K452300)	Diodes	4.5 kV 2.1 kA (5SDF 20L4521)
	4.5 kV 3 kA (5SNA 3000K452300)		4.5 kV 2.6 kA (5SDF 28L4521)
IGCTs	4.5 kV 1.9 kA (5SHY 55L4500)		4.5 kV 2 kA (5SDF 20L4520)
	5.5 kV 1.3 kA (5SHY 50L5500)		6.5 kV 1.1 kA (D1131SH)

In order to calculate the number of devices in series, the following expression is employed, which rounds to the next integer the content inside the parenthesis:

$$n_{series} = ceil\left(\frac{V_{\max\_peak}}{V_{100\text{FIT}}}\right) \tag{8}$$

where, V_{max_peak} is the maximum peak voltage that the transistor must withstand ($V_{C3}^{max}+\Delta V_{C3}^{max}/2$); $V_{100\text{FIT}}$ is the voltage of the IGBT/IGCT to have 100 failures within 10^9 hours of operation.
To calculate the number of interleaved branches in the PFC, the expressions in (9) are used. The variables in the numerator come from the PFC specifications, whereas the denominators correspond to the parameters from the datasheets.

$$n_1 = ceil\left(\frac{I_{\max\_peak}}{I_{peak\_sw}}\right), \quad n_2 = ceil\left(\frac{I_{T\_av}}{I_{dc\_sw}}\right), \quad n_3 = ceil\left(\frac{I_{D\_av}}{I_{av\_diode}}\right) \tag{9}$$

where, I_{max_peak} is the maximum peak current circulating through the transistor ($I_L^{max}+\Delta I_L^{max}$); I_{peak_sw} is the peak current of the IGBT (two times the DC current) or the maximum turn-off current of the IGCT; I_{T_av} is the maximum average current circulating through the transistor (among all the operating points); I_{dc_sw} is the DC current of the IGBT or the average current of the IGCT; I_{D_av} is the maximum average current circulating through the diode (among all the operating points); I_{av_diode} is the average current of the diode in the datasheet.

Then, the required number of interleaved branches is calculated as the maximum of the values in (9) and the total number of each type of device is defined in (11).

$$n_{inter} = max\ (n_1, n_2, n_3) \tag{10}$$

$$n_{total} = n_{series}\ n_{inter} \tag{11}$$

Once the number of interleaved branches and devices in series are identified, the average current and RMS current through the individual devices can be computed (I_{av_dev}) and (I_{rms_dev}), respectively (for the IGBT/IGCT and diodes). Then, the conduction (P_{cond}) and switching losses (P_{sw}) of the PFC are:

$$P_{cond} = n_{total}\left(V_0 I_{av\_dev} + r I_{rms\_dev}^2\right) \tag{12}$$

$$P_{sw} = n_{total}\frac{V_3/n_{series}}{V_{cc}}\left(E_{on} + E_{off}\right)f \tag{13}$$

$$P_{total} = P_{cond} + P_{sw} \tag{14}$$

where, V_0 and r are the on-state zero current voltage drop and the on-state resistance of a single device, respectively; V_3 is the voltage seen by the stack of series connected devices; E_{on} and E_{off} are the turn on and turn off energy of the device, respectively (which are a function on the current circulating through the device); V_{CC} is the voltage where the energy losses are measured; f is the switching frequency.
The previous formulas are used for IGBTs, IGCTs and diodes. Note that for the diodes the E_{on} is assumed to be zero and E_{off} corresponds to the loss of energy during the reverse recovery.
The losses estimation is done assuming that the devices are operated at the maximum allowed temperature for each type of device. They are calculated for all the operating points and then the maximum values are selected.

Inductor

Regarding the inductor, its inductance is calculated to keep the current ripple of the inductor below a certain value (in case of interleaved inductors, it is the sum of their current ripple that must be lower than a certain threshold). Due to the possible presence of interleaved branches (that will imply more than one inductor) the previous formula to calculate the ripple from the inductor (4) is updated into (15).

$$L = \frac{n_{inter}\,\alpha_{eq}(1/n_{inter} - \alpha_{eq})(V_1+V_2)}{f\,\Delta I_{L\_sum}^{max}} = \frac{n_{inter}\,\alpha_{eq}(1/n_{inter} - \alpha_{eq})(V_1+V_2)}{f\,\Delta I_L^{pu} I_{L\_sum}^{max}} \tag{15}$$

where, $\Delta I_{L\_sum}{}^{max}$ is the maximum allowed sum of the ripples of the inductors; $I_{L\_sum}{}^{max}$ is the maximum value of the sum of the different inductors' currents (maximum value of I_3); α_{eq} corresponds to an equivalent duty cycle for the interleaved structures ($\alpha_{eq}=mod(\alpha_d, 1/n_{inter})$).
Then, the previous formula is applied to all the operating points and the maximum value of L is selected. The voltage and current waveforms in the inductor at the operating point where the peak current is the highest have been used as the worst-case scenario to design the inductor. The design is done using the tool to size magnetic components developed in [10].

Capacitors

The capacitance of the capacitors is chosen to have a voltage ripple in the capacitors below a certain threshold. Increasing the number of interleaved branches allows to reduce the capacitance requirements for the same voltage ripple. The expressions in Table II are also modified to consider this effect:

$$C_3 = \frac{\alpha_{eq}(1/n_{inter} - \alpha_{eq})I_3}{f\,\Delta V_{C3}^{max}} = \frac{\alpha_{eq}(1/n_{inter} - \alpha_{eq})I_3}{f\,\Delta V_{C3}^{pu} V_{C3}^{max}} \tag{16}$$

$$C_1 = \frac{\Delta I_{L\_sum}^{max}}{8\,n_{inter}\,f\,\Delta V_{C1}^{max}} = \frac{\Delta I_{L\_sum}^{max}}{8\,n_{inter}\,f\,\Delta V_{C1}^{pu} V_{C1}^{max}} \tag{17}$$

The previous expressions are used in each operating point and then, the maximum value of C_1 and C_3 are then selected. Along with the maximum peak voltage ($V_{C3}{}^{max}+\Delta V_{C3}{}^{max}/2$ and $V_{C1}{}^{max}+\Delta V_{C1}{}^{max}/2$) and the maximum RMS current through each capacitor, they are used to implement the capacitors based on the catalog TRAFIM PRODUCTS 1950-6000 V (polypropylene film capacitors) from the manufacturer AVX [11]. In order to reach the required RMS current rating and capacitance, the paralleling of the capacitor models in [11] is considered. For the required voltage level (based on the maximum peak voltage), several capacitor models are available, which leads to different possible realizations. The capacitor model is chosen considering the minimum number of parallel capacitors being connected, the

minimum value of mass and the minimum volume (in this order). Once the capacitor model is selected, the equivalent capacitance, total mass, total volume and estimated power losses can be calculated.

Case study

Zhangbei grid in China (see Fig. 8) has been chosen as case study. It is a 4-terminal bipolar HVDC grid considering overhead lines and based on half-bridge Modular Multilevel Converters (MMC) [12].

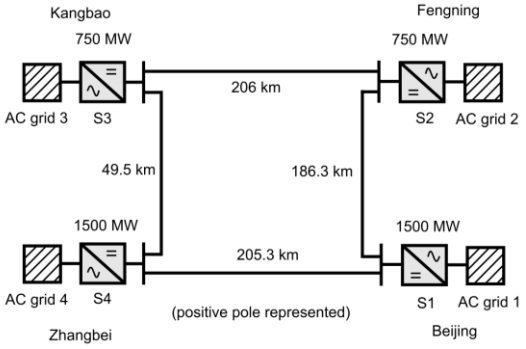

Fig. 8. Schematic representation of the Zhangbei 4-terminal HVDC grid (positive pole).

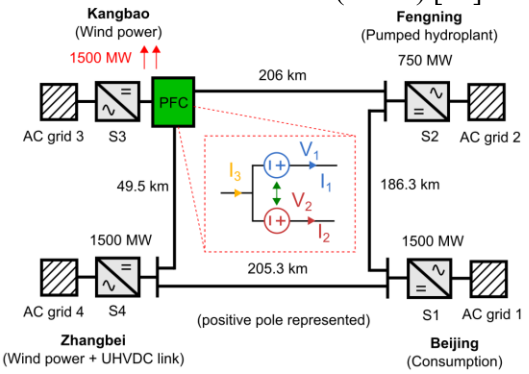

Fig. 9. Schematic representation of the Zhangbei grid after the power upgrade in S3 and the installation of a PFC at the same station.

The power ratings of each station and the lengths of each line can be seen also in Fig. 8. In order to apply the previous methodology, it is assumed that the total generation in S3 is increased from 1.5 GW to 3 GW, thus, a PFC is required in certain operating points to prevent the overload of the line between S4 and S1 (limit of 3 kA). Fig. 9 presents the Zhangbei grid scheme with the power upgrade and an example of a PFC installed in S3 (represented in the OPF formulation as two voltage sources).

After solving the OPF problem the voltages and currents through the device are obtained for the different operating points where the PFC is required while considering different PFC structures and the device installed in different nodes. The previous vectors of voltages and currents allow to obtain the maximum required voltage and current in each element of the PFC. Table IV presents those voltages and currents for the elements of the PFC, taking into account the structures of Fig. 4 installed in node 3. Structure A (in bold) is selected for this node since it is simpler and has the lowest requirements (step 1).

Table IV. Voltage and currents of the PFC structures in node 3

	Structure A		Structure B		Structure C	
	Voltage [kV]	**Current [kA]**	Voltage [kV]	Current [kA]	Voltage [kV]	Current [kA]
L	**5.78**	**2.96**	5.86	5.85	5.86	4.77
C_1	**1.08**	**2.90**	5.86	2.96	-	-
C_2	**5.78**	**2.90**	-	-	5.86	2.96
C_3	**-**	**-**	5.78	2.96	1.08	2.96
T_1	**5.86**	**2.96**	5.78	5.85	1.08	4.77
D_1	**5.86**	**2.96**	5.78	5.85	1.08	4.77
T_2	**-**	**-**	5.86	5.85	5.86	4.77
D_2	**-**	**-**	5.86	5.85	5.86	4.77

This step is repeated for the other nodes of the HVDC grid, and one structure in each node is selected and then compared with the ones in the other nodes (step 2). The PFC structure A in node 3 is found to have lower requirements than the other structures in the rest of nodes, thus the PFC structure A is selected to be installed in node 3 (this comparison is not shown here for due to space limitations). For this structure A in node 3, three possible variants can be considered (see Fig. 6). Then, the requirements of their capacitors are compared in Table V, selecting the variant 3 as the one with lower requirements.

Therefore, the sizing is done for PFC structure A Variant 3 in node 3. The allowed inductor ripple (ΔI_L^{pu}) is set at 10%, the allowed voltage ripples (ΔV_{C3}^{pu}, ΔV_{C1}^{pu}) are set at the maximum value according to the manufacturer constraints [11] (4.7% for C_3 and 20% for C_1). The switching frequency is set at 1 kHz.

The final PFC structure requires the use of two interleaved branches (see Fig. 11) due to the current requirements. Table VI, Table VII, and Table VIII illustrate the main outcomes of the sizing for the IGBTs/diodes, capacitors and inductors, respectively, according to the previously explained methodology. Table IX presents the losses estimation of the different PFC elements.

Table V. Comparison of the variants of PFC structure A in node 3

	Variant 1		Variant 2		**Variant 3**	
	C_1	C_2	C_3	C_2	$\boldsymbol{C_3}$	$\boldsymbol{C_1}$
Max. average voltage [kV]	1.08	5.78	5.86	5.78	**5.86**	**1.08**
Max. current peak [kA]	2.90	2.90	2.90	0.148	**2.90**	**0.148**
Max. capacitance [mF]	6.90	1.3	1.3	0.064	**1.3**	**0.34**
Max. energy [kJ]	3.98	21.35	21.64	1.07	**21.64**	**0.2**
Total max energy [kJ]	25.33		22.71		**21.84**	

Table VI. Sizing results of the IGBTs and diodes

	Model	n_{series} [-]	n_{inter} [-]	n_{total} [-]
IGBT T_a, T_b	4.5 kV 2 kA	3	2	6
Diode D_a, D_b	4.5 kV 2.1 kA	3	2	6

Table VII. Sizing results of the capacitors. Final value from catalog (required value)

	N° caps. in parallel	Equivalent Capacitance [mF]	I rms current [A]	DC voltage [V]	Total mass [kg]	Total volume [dm^3]
Capacitor C_1	1	1.34 (0.05)	185 (85)	1950 (1204)	14	8.6
Capacitor C_3	3	1.40 (0.66)	765 (739)	6000 (5875)	120	84.1

Table VIII. Sizing results of the inductor

L_a, L_b [mH]	1.77
N° inductors [-]	2
Type	FeSi grain-oriented core, CTC winding, no cooling
N° turns [-]	20
Current density [A/mm^2]	0.93
Max. flux density [T]	0.686
Mass [kg]	9080 (2x4540)
Volume [dm^3]	1626 (2x813)

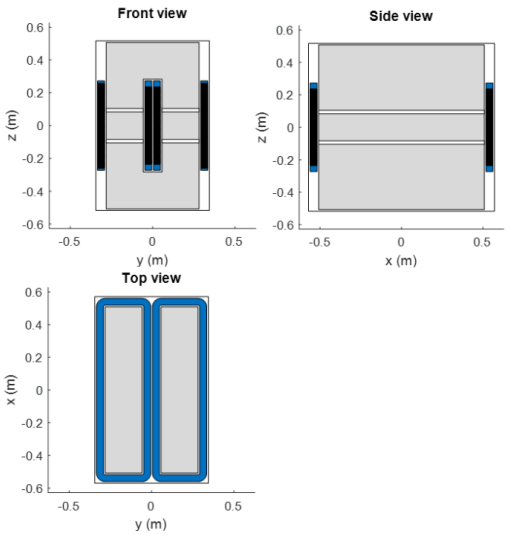

Fig. 10. Front, side and top view of the inductors (L_a and L_b)

Table IX. Power losses estimation of the PFC elements

	Max. conduction losses [kW]	Max. switching losses [kW]	Max. total losses [kW]
IGBTs/diodes	26.93 (3.98 per dev.)	71.90 (7.82 per dev.)	95.93 (8.1 per dev.)
Capacitor C_1	-	-	0.005
Capacitor C_3	-	-	0.084
Inductors	-	-	6.12
Total*	-	-	102.14

*Note, that they are not happening at the same operating point. The losses in a 200 km line at half the current capacity (1.5 kA) in Zhangbei grid are in the order of 5 MW, much higher than the total losses of the PFC.

It can be noticed that 3 devices are needed in series for each IGBT and diode in Fig. 11, making a total of 12 devices for the PFC. C_3 requires 3 capacitors in parallel due to the current rating and the inductors

present a significant footprint and weight compared to the other elements. The power losses, though being more than 100 kW, are much lower than the expected losses in the lines (in the range of several MW). Fig. 12 shows a preliminary 3D design to illustrate the size of the elements without considering insulation distances or providing a definitive arrangement or connections.

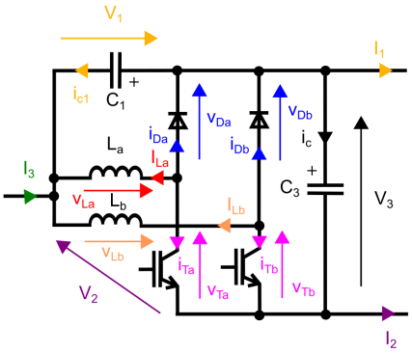

Fig. 11. Selected PFC for the sizing (PFC structure A in node 3 Variant 3).

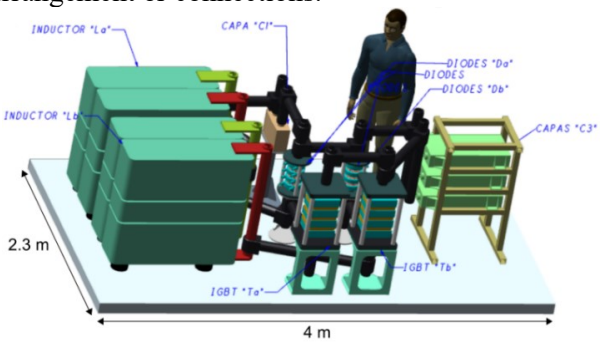

Fig. 12. 3D preliminary design of the power electronic devices and passive components of the PFC in Fig. 11 (C_1 and C_3 on the shelves).

Conclusion

The methodology to obtain the specifications, select the most convenient converter structure and perform the sizing of an interline PFC have been introduced and applied to a case study considering a real HVDC grid. The results show that the PFC is a feasible medium voltage converter with a high current rating, requiring series connection of IGBTs/diodes and interleaved branches to deal with the voltage and current requirements. The inductors represent a significant footprint and weight of the PFC. The power losses of the device, in the order of hundreds of kW, should be managed thanks to a well-designed cooling system but are much lower than the power losses in the lines of the HVDC grid. Additional work is required to size the additional elements, such as bypass switches, protection equipment and cooling systems.

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