Modelling and control of an MMC-HVDC submodule with energy storage for fast frequency response

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Keywords

«HVDC», «Modular Multilevel Converter (MMC)», «Energy Storage System», «Converter control»

Abstract

Recent works have shown that energy storage systems (ESSs) can be distributed in a modular multilevel converter (MMC) for the enhancement of high voltage direct current (HVDC) converter stations in order to provide ancillary services. In this case, DC-DC converters are compulsory to interface energy storage elements to submodule (SM) capacitors. However, the choice of the converter topology and its control is not straightforward due to the complex working principle of an MMC. This paper proposes a suitable interface converter with a control strategy to address these issues. Special emphasis is put on the modelling of the converter to highlight all the interactions inside a SM and ease the design of the controllers. To conclude, a downscaled prototype validates the effectiveness of the proposed solution.

Introduction

The increasing penetration of power electronics in power transmission systems to favor the introduction of renewable energy sources, the decommissioning of classical power plants with direct connection of synchronous generators to the grid and the interconnection of large power systems, have introduced significant challenges to grid operators to ensure a secure supply of the electrical energy [1]. One noticeable consequence is the reduction of system inertia since these new generation units are physically decoupled from conventional synchronous generators [2]. However, synchronous machines play a crucial role in the dynamics of system frequency, through inertial response, which depends on the kinetic energy stored. As a result of the decreased level of inertia in power system, grid frequency reacts more abruptly and nervously in case of fault. This is particularly critical for the stability of power systems. Therefore, there is an increasing need of innovative solutions and short-term ancillary services, such as fast frequency response (FFR) or power oscillation damping (POD) [3].

Energy storage systems (ESSs) have raised a clear attractiveness for such applications in both academia and industry. They are expected to offer the necessary flexibility and dynamics to comply with new grid requirements, and be an alternative solution for ancillary services. Because these new services require a fast response during a short period of time, low energy content (i.e. 50 MW from 5 to 30s [4]) is needed compared to traditional significant grid scale energy storage systems. Thus, storage technologies such as supercapacitors have received a growing interest to meet these specifications. In addition, the requested power is relatively low in comparison to the bulk power that flows through transmissions lines. Therefore, recent works have been dedicated to the integration of ESSs inside modular power converters used for high power and high voltage applications such as modular multilevel converter

(MMC). The goal is to extend the set of services the converter can provide with an energy storage function, in addition to its AC/DC power conversion capability, without requesting significant changes or lowering its performances [5]–[7].

A key advantage of modular converters, compared to classical voltage source converters, is that ESSs can be distributed within their sub-modules (SMs). The configuration of a three phase MMC is reminded in Figure 1(a). Each phase i ($i \in \{a, b, c\}$) is divided into an upper and lower arm (superscript $\{u, l\}$) that consists in an arm inductor in series with a set of SMs. Most of the time, half-bridge SMs that comprise two IGBTs with anti-parallel diodes are used. In order to make an energy storage submodule (ES-SM), as shown in Figure 1(c) [7], an energy storage element is connected to the SM capacitor.

A crucial aspect is the way the energy storage element, here supercapacitors, is connected to the SM capacitor. Although in theory, an energy storage element can be directly connected to an SM capacitor, significant part of the high frequency components in $i_{sm}^{u,l}$ would circulate through the energy storage element. This leads to an accelerated aging of this device, making this solution irrelevant [8]–[10]. Passive filters can be considered [10], [11] but during operation the SM capacitor and the energy storage element voltages are not able to evolve independently. The use of the energy storage element is not optimal. So, an interface converter is compulsory to provide a controllable energy decoupling between the two entities as seen in Figure 1(c). In this work, the SM capacitor voltage is controlled by the global control of the MMC (as for an MMC without ESSs). In addition to its design, one of the main challenges relies on the control of the interface converter to ensure that the ESS provides the correct amount of power.
This paper proposes a straightforward model of an ES-SM based on a convenient interface converter [7], [12]. The small signal modelling of the converter and its linear state-space model are depicted. This model details the additional dynamics of the converter and can be used for stability analysis. Then, a control strategy is described to manage the ESS of an ES-SM to achieve the expected performances.

The content of the paper is organized as follows. The modelling of an ES-SM is presented in the following section. Afterwards, the approach for developing the model of the interface converter and its linearization, using the small signal approximation, are explained. In the third section, the overall control strategy of the ES-SM is introduced. After that, the model is validated through a downscaled prototype. Finally, the last section concludes and highlights the advantages of the proposed solution.

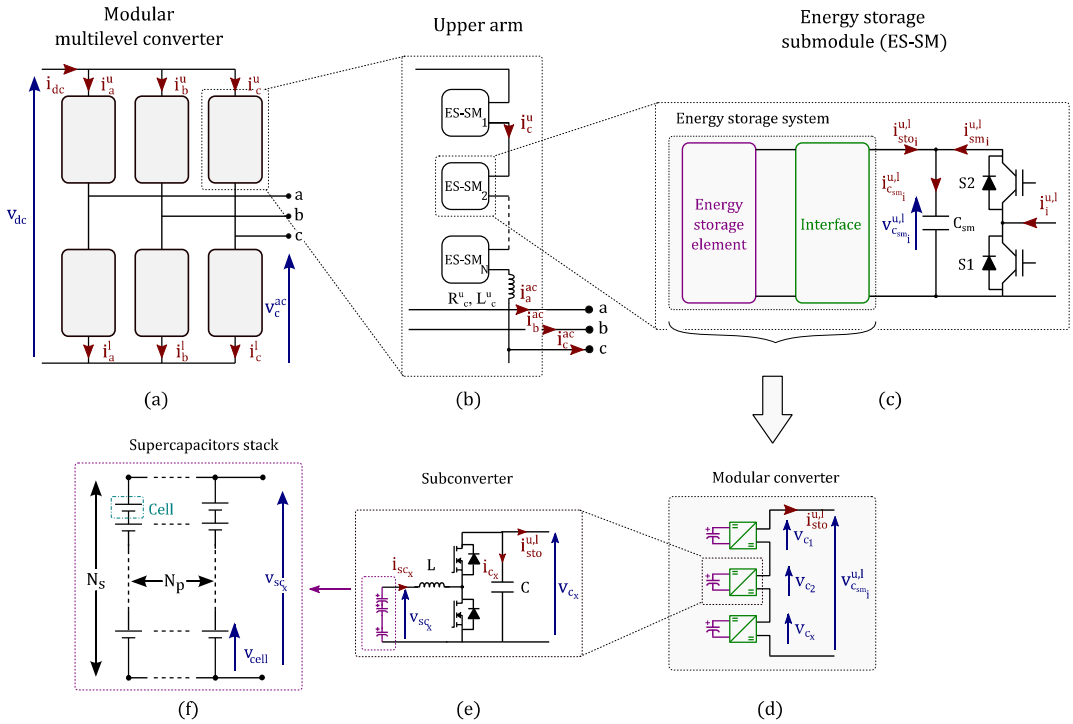

Figure 1 Topology of a modular multilevel converter with integrated energy storage systems

Energy storage submodule modelling

In this section, the topology and the modeling of the proposed ES-SM are presented. The proposed interface converter is a modular converter that consists of a number N_{mod} of series connected subconverters as depicted in Figure 1(d) and (e). Each of these subconverters consists of a bidirectional DC-DC converter that works as an interface between the ES-SM capacitor and a supercapacitor stack. As this modular interface converter allows to reduce the voltage constraint on each subconverter, the bidirectional DC-DC converters can include MOSFETs as switching elements (different from the IGBT power modules in the main switches of the half-bridge of a SM). This topology allows the use of affordable switches working at high switching frequency to make an ES-SM with a better power density. By switching at high frequency and using affordable components, the size of the passive components and the cost of the ES-SM are thus significantly decreased [12]. This topology is especially relevant when the maximum power of the ESS is low in comparison to the power rating of the MMC.

Mathematical description

In order to facilitate the analysis of the converter, average type modelling can be used. By using the switching function concept of a bidirectional DC-DC converter, the equivalent model of the proposed ES-SM can be drawn as shown in Figure 2. Each subconverter can be modelled as a controllable current source from the ES-SM DC bus point of view, through a modulation index α'_x (with $x \in \{1, \dots, N_{mod}\}$) such as $\alpha'_x = 1 - \alpha_x$, with α_x the duty cycle of one subconverter (i.e. the fraction of time the lower switch of a subconverter is closed). Note that in this model, switching losses are not considered. All the subconverters of the proposed topology are similar and operate in continuous conduction mode through a complementary control of the switches.

As it can be clearly seen, the SM capacitor and the N_{mod} subconverters are coupled through the branch current $i_{sto}^{u,l}$ that comes from the ESS. Note also that the sum of the output voltage of all the subconverters v_{c_x} equals at any time the SM capacitor voltage $v_{c_{sm}}^{u,l}$. Due to this strong coupling, one subconverter cannot be independently modelled with a classical average model of a bidirectional DC-DC converter like in [13]. Therefore, in this paper, a mathematical model, that considers these interactions, is proposed.

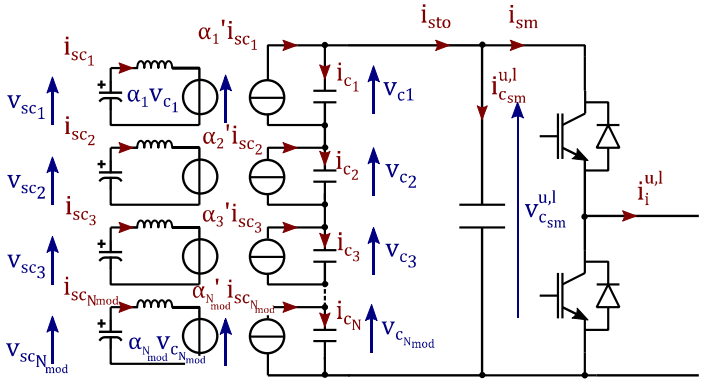

Figure 2 Equivalent model of an ES-SM

First, the dynamics of the SM capacitor (C_{sm}) and the subconverter capacitors (C) of an ES-SM can be described by the following set of equations:

$$i_{c_{sm}}^{u,l} = C_{sm} \frac{dv_{csm}^{ul}}{dt} \quad (1) \qquad i_{c_x} = C \frac{dv_{c_x}}{dt}. \quad (2)$$

Then, the currents $i_{c_{sm}}^{u,l}$ and i_{c_x} that flows respectively through each capacitor are defined as:

$$i_{c_{sm}}^{u,l} = -i_{sm}^{u,l} + i_{sto}^{u,l} \quad (3) \qquad i_{c_x} = \alpha'_x i_{sc_x} - i_{sto}^{u,l}. \quad (4)$$

where i_{sc_x} is the current across the supercapacitor stack of one subconverter, v_{sc_x} the corresponding voltage at its terminal and $i_{sm}^{u,l}$ a switched current that goes out of an ES-SM (cf. Figure 2). By applying

Kirchoff's voltage law in an ES-SM and using Eq.(1), it is noticed that the current through the SM capacitor is linked to the sum of the output voltage of all the subconverters (cf. Eq.(5)). So, the currents of the SM capacitor and the subconverter capacitors are closely related as shown in Eq.(6), assuming that the subconverter capacitors C are similar.

$$i_{c_{sm}}^{u,l} = C_{sm} \frac{d\sum_{x=1}^{N_{mod}} v_{c_x}}{dt} \quad (5) \qquad i_{c_{sm}}^{u,l} = \frac{C_{sm}}{C} \sum_{x=1}^{N_{mod}} i_{c_x}. \quad (6)$$

At this stage, each subconverter is characterized by two state variables: the output voltage of a subconverter v_{c_x} and the supercapacitor stack current i_{sc_x}. Similarly, the input variables correspond to the duty cycles of all the subconverters $\alpha_{N_{mod}}$ and the switched current that flows towards the MMC arm $i_{sm}^{u,l}$. In order to derive the equivalent circuit of the proposed ES-SM, considering the coupling among the subconverters, the superimposing principle can be used in combination with in Eq.(1)-(6). The goal is to study the influence of all the input variables on the state variables of the system. Note also that the superposition principle is only applied to deduce the linear part of the model, since the average model described in Figure 2 is nonlinear.

In Figure 3(a), the impact of a variation of α_1' or $i_{sm}^{u,l}$ on the output voltage of the first converter v_{c_1} can be studied by zeroing the duty cycle of the remaining subconverters. The same process can be applied to study the influence of a change of α_x' on v_{c_1} (here α_2') as described in Figure 3(b). Note that $i_{sm}^{u,l}$ must be considered null in that case.

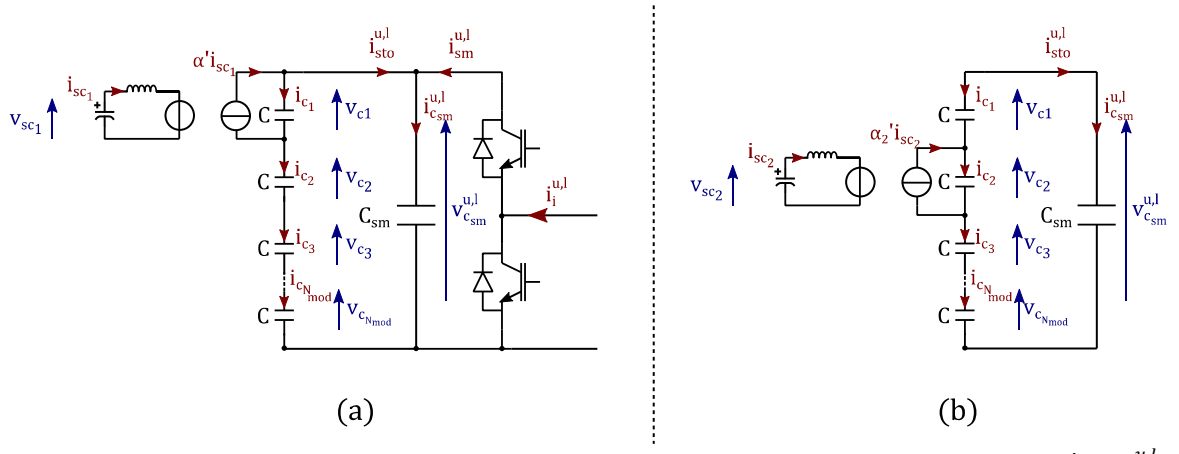

Figure 3 Equivalent model of the ES-SM for the superimposing principle in order to study: (a) the influence of α_1' and $i_{sm}^{u,l}$ on v_{c_1} (b) the influence of α_2' on v_{c_1}

By rewriting Eq.(1)-(6) according to the case studied (Figure 3(a) or (b)), one can solve each circuit by expressing the output voltage of the first converter v_{c_1} as a function of the input variables quoted previously. Therefore, Eq.(7) and (8) comes from figures 3(a) and 3(b) respectively:

$$i_{c_1} = C\frac{dv_{c_1}}{dt} = \alpha_1' i_{sc_1}\left(\frac{C + (N_{mod}-1)C_{sm}}{C + N_{mod}C_{sm}}\right) - i_{sm}^{u,l}\left(\frac{C}{C + C_{sm}N_{mod}}\right) \quad (7)$$

$$i_{c_1} = C\frac{dv_{c_1}}{dt} = -\alpha_2' i_{sc_2}\left(\frac{C_{sm}}{C + C_{sm}N_{mod}}\right). \quad (8)$$

According to the prior analysis and some simple algebra, a new average circuit for the subconverter of modular interface converter, considering Eq.(7)-(8), is drawn as illustrated in Figure 4. It shows the influence in variations of all the input variables over the output voltage of one subconverter. Note that it results from the sum of all the input variables actions. Moreover, this model can be easily adapted to different energy storage devices, such batteries or supercapacitors, by substituting the energy storage model block.

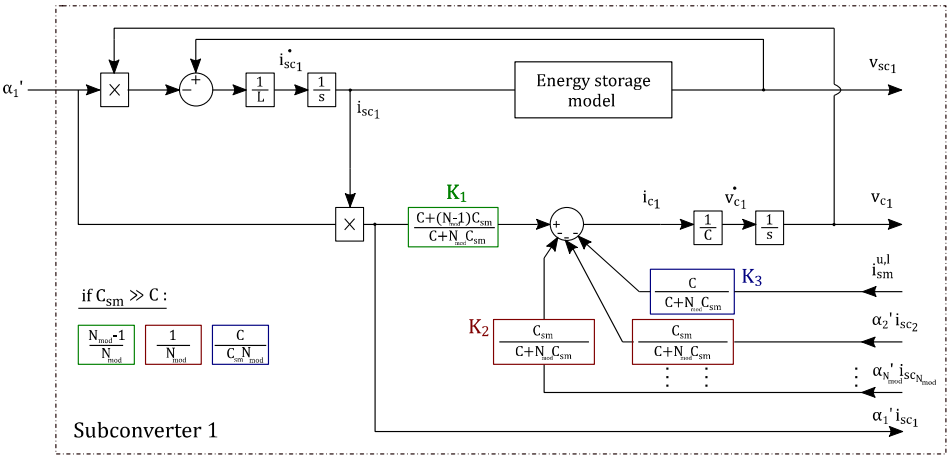

Figure 4 New average model of one subconverter of the proposed modular interface converter with internal coupling

This model outlines that the voltage variation of the output voltage of a subconverter is not only impacted by the SM current $i_{sm}^{u,l}$ and its output current $\alpha_x' i_{sc_x}$, but also by the output currents of the other subconverters of the ES-SM. This is illustrated by the presence of equivalent gains among the subconverters and the ES-SM capacitor which are functions of the ES-SM capacitance C_{sm} and the intermediate capacitance of a subconverter C. It also means that these different currents charge/discharge the capacitor C associated to the output voltage v_{c_1} in different way. Note that these gains can highly differ since the capacitance of the ES-SM capacitor C_{sm} is large and the number of subconverter N_{mod} is low. In that case, these coefficients can be simplified as:

- $\alpha_1' i_{sc_1}$ charges the capacitor of the 1st subconverter by a coefficient $(N_{mod}-1)/N_{mod}$.
- A fraction $1/N_{mod}$ of the currents $\alpha_x' i_{sc_x}$ from the other subconverters discharges this capacitor.
- A fraction of $i_{sm}^{u,l}$ discharges the capacitor associated with the voltage v_{c_1} through an equivalent capacitor $N_{mod} C_{sm}$ (in blue). Note that it contributes identically to each subconverter capacitor by actually distributing the SM capacitor voltage.

Finally, the average model developed in Figure 4 was compared with the average model depicted in Figure 2 under MATLAB/Simulink. It was noticed that the two models were strictly identical.

State space model of the ES-SM and linearization

Thanks to the above analysis, the state space model for N_{mod} subconverters in series can be described in Eq.(9), with the coefficients K_1, K_2 and K_3 given on Figure 4.

$$\dot{X} = \mathrm{AX} + \mathrm{BU} = \begin{bmatrix} 0 & E \\ F & 0 \end{bmatrix} \mathrm{X} + \begin{bmatrix} G & 0 \\ 0 & H \end{bmatrix} \mathrm{U} \quad \text{with} \quad (\mathrm{E}, \mathrm{F}, \mathrm{G}, \mathrm{H}) \in \mathcal{M}_{\mathrm{N_{mod}}}(\Re) \tag{9}$$

$$\mathrm{X} = \left[\mathrm{i_{sc_1}}, \dots, \mathrm{i_{sc_{N_{mod}}}}, \mathrm{v_{c_1}}, \dots, \mathrm{v_{c_{N_{mod}}}} \right]^{\mathrm{T}} \qquad \mathrm{U} = \left[v_{\mathrm{sc_1}}, \dots, \mathrm{v_{sc_{N_{mod}}}}, \mathrm{i}_{sm}^{\mathrm{u,l}}, \dots, \quad \mathrm{i}_{sm}^{\mathrm{u,l}} \right]^{\mathrm{T}}$$

$$\mathrm{E} = \mathrm{diag}\left(\frac{-(1-\alpha_1)}{\mathrm{L}}, \dots, \frac{-\left(1-\alpha_{\mathrm{N}_{mod}}\right)}{\mathrm{L}} \right) \qquad \mathrm{F} = \begin{bmatrix} \frac{(1-\alpha_1)K_1}{\mathrm{C}} & \cdots & \frac{-\left(1-\alpha_{\mathrm{N}_{mod}}\right)K_2}{\mathrm{C}} \\ \vdots & \vdots & \vdots \\ \frac{-(1-\alpha_1)K_2}{\mathrm{C}} & \cdots & \frac{\left(1-\alpha_{\mathrm{N_{mod}}}\right)K_1}{\mathrm{C}} \end{bmatrix}$$

$$G = diag\left(\frac{1}{L}\right) \qquad H = diag\left(\frac{-K_3}{C}\right)$$

As observed in Eq.(9), the proposed average model is a non-linear system (i.e. duty cycles appear in the state matrix A). If the controller is designed thanks to a linear approach, a linear representation of the interface converter is required. Thus, differentiation is carried out using the small signal approximation around an equilibrium point. Each variable of (9) is translated under the form $x = \tilde{x} + \bar{x}$, where $\tilde{x}$

denotes the small variations from the operating point $\bar{x}$, around which the linearization is made. The linear model of one subconverter is given as follows:

$$\begin{bmatrix} \frac{d\widetilde{i_{sc_1}}}{dt} \\ \frac{d\widetilde{v_{c_1}}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \dots & 0 & \frac{-(1-\overline{\alpha_1})}{L} \\ \frac{(1-\overline{\alpha_1})K_1}{C} & \frac{-(1-\overline{\alpha_2})K_2}{C} & \dots & \frac{-(1-\overline{\alpha_{N_{mod}}})K_2}{C} & 0 \end{bmatrix} \begin{bmatrix} \widetilde{i_{sc_1}} \\ \widetilde{i_{sc_2}} \\ \vdots \\ \widetilde{i_{sc_{N_{mod}}}} \\ \widetilde{v_{c_1}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 & \frac{\overline{v_{c_1}}}{L} & 0 & \dots & 0 \\ 0 & -\frac{K_3}{C} & -\frac{\overline{i_{sc_1}}K_1}{C} & \frac{\overline{i_{sc_2}}K_2}{C} & \dots & \frac{\overline{i_{sc_{N_{mod}}}}K_2}{C} \end{bmatrix} \begin{bmatrix} \widetilde{v_{sc_1}} \\ \widetilde{i_{sm}^{u,l}} \\ \widetilde{\alpha_1} \\ \widetilde{\alpha_2} \\ \vdots \\ \widetilde{\alpha_{N_{mod}}} \end{bmatrix} \quad (10)$$

Note that those previous models are independent of the energy storage technology, since the voltage v_{sc_x} is seen as an input. In this paper, supercapacitors have been selected as energy storage devices. So, the input variable v_{sc_x} can be substituted in (9) with an equivalent circuit of a supercapacitor such as:

$$i_{sc_x} = -C_{sc}\frac{dv_{sc0_x}}{dt} \quad (11) \qquad v_{sc_x} = v_{sc0_x} - ESR_{sc_x}i_{sc_x} \quad (12)$$

where C_{sc} is the equivalent capacitance of a supercapacitor stack, ESR_{sc_x} its equivalent series resistance and v_{sc0_x} its internal voltage. Input variables of the system v_{sc_x} are removed and state variables are added v_{sc0_x}. In order to obtain the new linearized subsystem under the small signal approximation, the same process as presented in (10) is applied. Finally, the overall state-space model of the proposed interface converter is obtained by combining all the N_{mod} individual subconverters.

Model validation and analysis

In order to validate the linear model of an interface converter, comparisons with the average model described in Figure 4 are performed under MATLAB/Simulink. The parameters of the interface converter corresponds to the case study of a 1GW 401-level MMC converter designed for providing fast frequency response with a power and energy capability of 50MW/900MJ [6], [7], [12]. Each 1.6kV ES-SM contains a modular interface converter with four subconverters (cf. Figure 1) having an average output voltage of 400V and a maximum supercapacitor stack voltage v_{sc_x} of 310V. As a reminder, here, each subconverter has the same characteristics, and as a consequence performs identically. Two simulations, with different step change on the duty cycle ($\widetilde{\alpha_1} = 0.05, \widetilde{\alpha_1} = -0.1$), were performed to show variations around different operating points. Both models were initialized as follows:

$\rightarrow \widetilde{\alpha_1} = -0.1$	$\overline{v_{c_x}} = 400\ V$	$\overline{v_{sc_0}} = 243\ V$	$\overline{i_{sc_x}} = 10\ A$	$\overline{\alpha_x} = 0.39$
$\rightarrow \widetilde{\alpha_1} = 0.05$	$\overline{v_{c_x}} = 400\ V$	$\overline{v_{sc_0}} = 180\ V$	$\overline{i_{sc_x}} = -5\ A$	$\overline{\alpha_x} = 0.55$

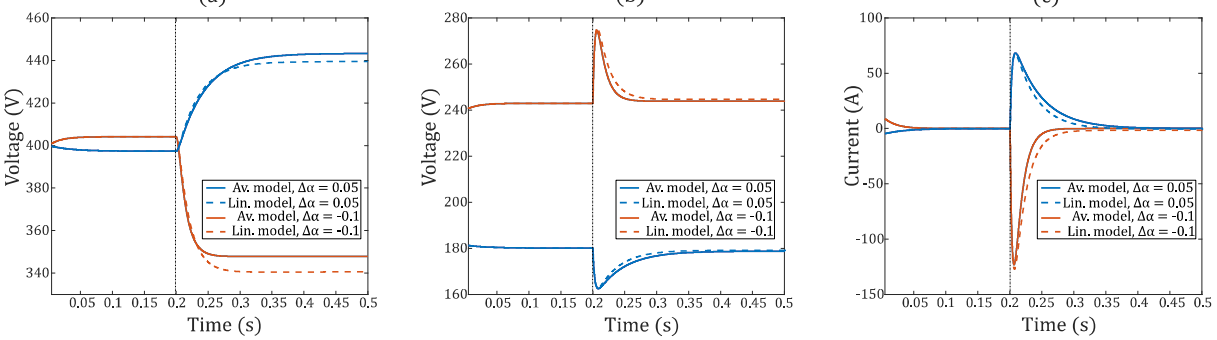

Figure 5 Comparison results between the proposed average model (continuous lines) and the linearized model (dashed line) after a change on the duty cycle, with: (a) the subconverter output voltage v_{c_x} (b) the supercapacitor stack voltage v_{sc_x} of a subconverter (c) the supercapacitor stack current i_{sc_x} of a subconverter

Firstly, at t = 0.2s, the step change on the duty cycle α_x of a subconverter is carried out. Comparison results are presented in Figure 5. As observed, only a small deviation between the two models appears. This can be explained by the fact in a linear model around an equilibrium point, some terms are disregarded such as the multiplication of two small variations, and the accuracy of the model is only high near to the equilibrium point [13]. The state space matrix representation also permits to compute the transfer matrix containing all the transfer functions from the input variables $\{\widetilde{i_{sm}^{u,l}}, \widetilde{\alpha_1}, \dots, \widetilde{\alpha_{N_{mod}}}\}$ to the state variables $\{\widetilde{i_{sc_1}}, \dots, \widetilde{i_{sc_{N_{mod}}}}, \widetilde{v_{c_1}}, \dots, \widetilde{v_{c_{N_{mod}}}}, \widetilde{v_{sc0_1}}, \dots, \widetilde{v_{sc0_{N_{mod}}}}\}$.

Since the subconverter capacitor voltage v_{c_x} is controlled in a way to be a constant fraction of the submodule capacitor voltage $v_{csm}^{u,l}$, it is interesting to observe the influence in variations of the duty cycle of one subconverter (e.g. α_1) over its supercapacitor stack current (e.g. i_{sc_1}), and the same current for another subconverter (e.g. i_{sc_2}), according to different power set-points P_{ess} of the interface converter.

Figure 6 shows the Bode diagrams obtained for both functions in open loop. Note that a configuration with four subconverters in series with the same parameters as in the previous section have been kept for this analysis. The power set-point of the interface converter, equally distributed among the subconverters, is in the range of -20.8 to 20.8 kW, while v_{sc_x} is still set at 243 V. As observed, the major change is an important phase shifting depending on the sign of the power flow for both functions. In addition, for the transfer function α_1 to i_{sc_1} (cf. Figure 6(a)), operating at low power leads to a slight decrease in the steady state gain.

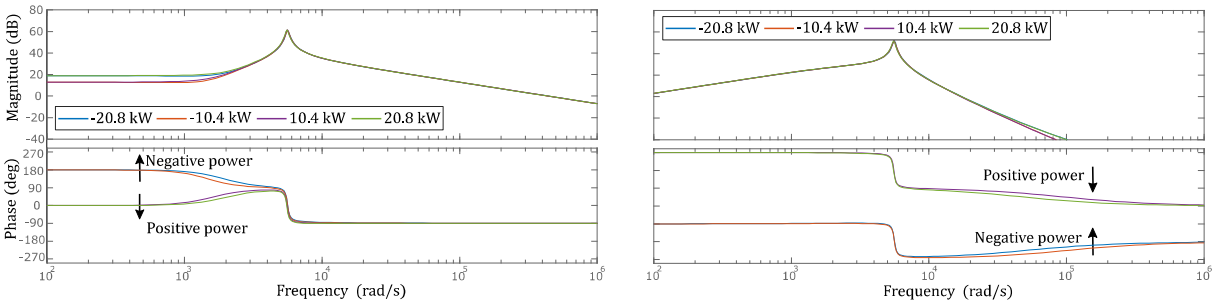

Figure 6 Bode diagram of (a) α_1 to i_{sc_1} and (b) α_1 to i_{sc_2} for a constant supercapacitor stack voltage of 243V and a power output comprises between -20.8 to 20.8 kW.

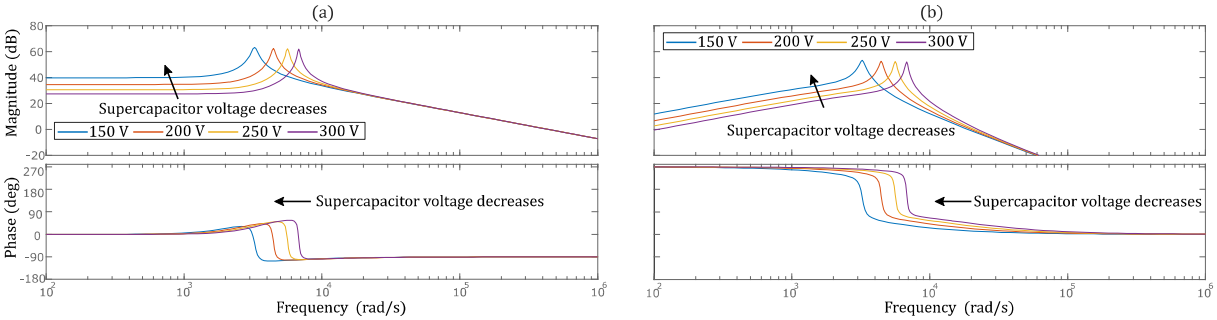

Figure 7 Bode diagram of (a) α_1 to i_{sc_1} and (b) α_1 to i_{sc_2} for a supercapacitor stack voltage varying from 150 to 300V and a constant output power of 20.8 kW.

Then, Figure 7 describes how the Bode diagrams of the same functions evolve as the operating point varies for a supercapacitor stack voltage (v_{sc_1}) between 150 to 300V and for constant output power (20.8 kW). Note that the bandwidth of the system decreases when the supercapacitor stack voltage is reduced, while steady state gain increases. The phase of the system is shifted toward low frequencies. It seems there is more risk for the system to be unstable if the supercapacitor stack voltage is low.
At last, it is observed from this preliminary analysis that the state of the system is highly modified according to the operating point of the interface converter. That is why the proposed analytical model can be useful to design the controllers for the voltage and power loops of the system in order to ensure stability over a wide range of operating points.

Design of the control scheme

This section describes the operation modes of the interface converter and its supercapacitor stack. The presence of a controllable interface between the ES-SM capacitor and the energy storage elements allows to change the way the power flow is managed in an MMC. However, the ESS of an ES-SM is a secondary function that should be added in a complex system. It cannot be freely controlled and operational constraints have to be respected. For this reason, a control scheme that allows to integrate the ESSs and keep the traditional energy based control of an MMC with only minor changes has been implemented as described in Figure 8 [6], [7].

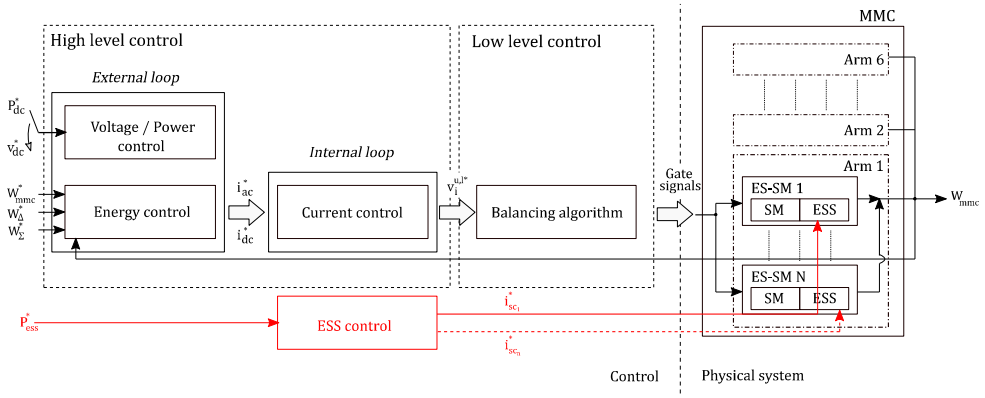

Figure 8 Schematic diagram of the proposed control of an MMC with embedded ESSs

Note that this control scheme is the same whether the ESS is used or not. The following points are addressed with the proposed control, which is more precisely described in [7], [12]:

1. The interface converter controls the power provided by the ESS within the ES-SM as shown in Figure 8. Consequently, the traditional energy control of the MMC and voltage balancing control of the SM capacitor voltages remain unchanged. The power provided by the ESS, P_{ess}, corresponds to a measurable disturbance for the SM capacitor voltage control. Note that if it is a disturbance with low dynamics for the considered ancillary services, the energy control of the MMC can easily deal with it. In contrast, if high dynamics would be requested, a feedforward action could be added to the MMC control.

2. The SM capacitor voltage must be correctly distributed among the subconverters of the interface converter which are designed to support a fraction of the SM capacitor voltage (cf. Figure 1).

3. It must be avoided that the inherent low frequency components of a SM, due to a modulated current that flows through the SM capacitor, are reflected in the energy storage elements. Indeed, this would deteriorate their lifetime [14]. This is reached thanks to an active filtering method through the control of the interface converter.

4. A balancing strategy to avoid the divergence of the state of charges of the supercapacitor stacks from one to another must be implemented. Thus, the concerns of the natural discrepancies among supercapacitor stacks due to a non-uniform manufacturing process is overcome.

Because of goals 1 and 2, all subconverters must have a voltage loop excepted one which has its voltage indirectly controlled. This latter controls the current $i_{sto}^{u,l}$ (cf. Figure 1) to ensure the correct amount of power at the ES-SM capacitor terminals since all subconverters are in series [12]. To achieve these control objectives, a cascaded control approach is used by nesting two loops and considering time scaled decoupling assumptions [13]. An inner current loop regulates the current that flows in the supercapacitor stack i_{sc_x}, while an outer voltage loop (excepted for the subconverter controlled in power) controls the dynamic of the subconverter capacitor voltages v_{c_x}. The linearized model developed (cf. Eq.(10)) allows to make stability analysis, and ease the design of the required controllers.

Experimental results

A downscaled prototype of the proposed ES-SM, with a rapid control prototyping approach, has been built to demonstrate the effectiveness of the proposed solution. Its physical parameters are presented in Figure 9. It consists in three half-bridge subconverters in series with split supercapacitor stacks connected to a main DC capacitor. This latter is supplied by an external power supply that allows to reproduce the complex shape of the current $i_{sm}^{u,l}$. Finally, all different control and supervision tasks are realized by a SpeedGoat FPGA real-time target machine. It executes all the control actions of the mock-up after retrieving the system current and voltage measurements. The controllers were designed using the developed linearized model in order to ensure a stable system in the expected operating range.

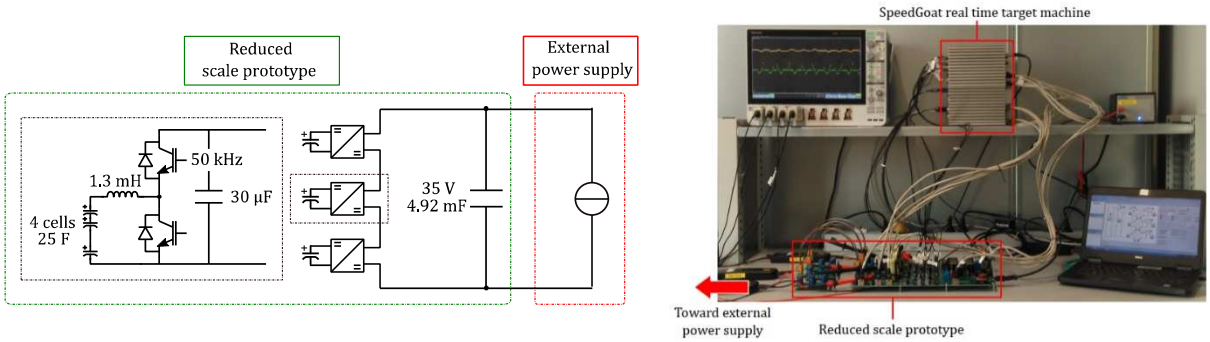

Figure 9 Downscale prototype of the proposed ES-SM with its characteristics

Figure 10 illustrates the results for the proposed ES-SM in discharging and charging mode. The supercapacitor stack voltages are initialized at half of the usable stored energy W_{sc} (i.e. 8.5V). The ES-SM has to provide a symmetrical power response that allows a charge (or discharge) of half of the usable energy stored (i.e. at 1 p.u. all the usable energy is provided or stored). The time response is limited at 500 ms since new fast ancillary services usually require a maximum activation time comprised between 500 ms and 1 sec, with a minimum support time to assist the establishment of reserves with time delay [6], [7], [12].

As it can be observed, the system responds correctly. The subconverter capacitor voltages v_{c_x} are well balanced. As a reminder, the sum of these voltages stands for the ES-SM capacitor voltage. Note that it coincides well with a stepped voltage waveform at the terminal of a SM capacitor that contains inherent low frequency components. However, these harmonics are not reflected in the supercapacitor stack voltages v_{sc_x}. This means that the proposed control scheme to suppress these voltage fluctuations (not describe here but in [7], [12]) works correctly.

Conclusion

This paper describes a state-space model of a modular interface converter for integrating an ESS in an MMC submodule. This average model considers the internal coupling that can appear when several subconverters are in series and connected in parallel to a DC capacitor. Then, a linearized model, under the small signal approximation, has been developed. This latter matches correctly with the proposed average model, and preliminary stability analysis point out instability phenomenon as a particular concern for this architecture. Indeed, the system behavior greatly varies according to the operating point. Therefore, the proposed model is useful for assessing the validity of a control of such converter. Similarly, a control strategy of the ES-SM is introduced to ensure that the energy storage function can be correctly integrated within a SM, without changing significantly the overall control of an MMC. To conclude, a downscale mock-up confirms the validity of the approach.

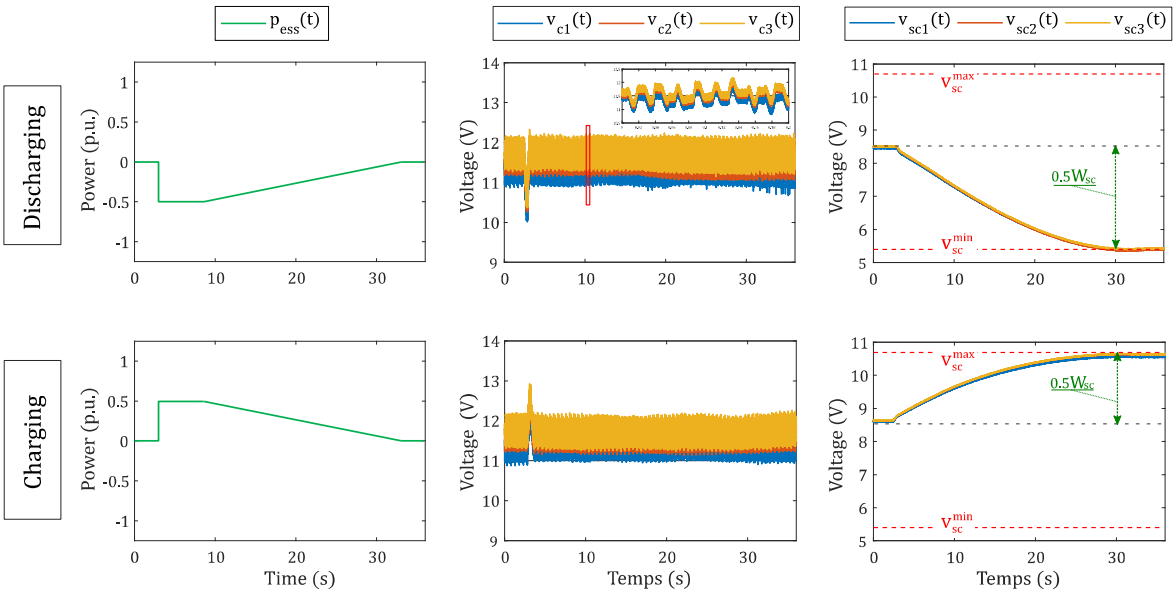

Figure 10 Experimental results in charging and discharging mode with: (left) the power the ES-SM has to provide (center) the output voltage of all the subconverters (right) The voltage of the supercapacitor stacks

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