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Florian Errigo, Florent Morel, *Senior Member, IEEE,* Cédric Mathieu De Vienne, Laurent Chédot, Ali Sari, and Pascal Venet

***Abstract*—Modular multilevel converters (MMCs) have been recognized as the most attractive technology for high voltage direct current (HVDC) applications during the last years. Their advantages include the ability to freely control the internally stored energy in the distributed submodules (SMs) and to independently control AC and DC powers. Recent studies showed that an MMC can take advantage of this degree of freedom to supply ancillary services with low energy requirements such as frequency response or power oscillation damping by connecting energy storage systems (ESSs) to its SM capacitors. This paper proposes a modular DC-DC converter as an interface between the energy storage element and the SM capacitor. As it can be built with switches allowing a high switching frequency, it is shown that the volume of the passive components can be reduced in comparison with interface converters known in the literature. The proposed control strategy avoids to transfer the harmonics of a SM to the ESS that prevents to drastically oversize the system. The proposed control method also provides an appropriate energy exchange without affecting the control philosophy of an MMC and it addresses balancing issues. Simulations and a downscaled prototype confirm the relevance of the proposed control. As the proposed interface converter is able to track the power reference with fast dynamics, it provides the same system-level advantages as other interface converters known in the literature but with a reduced volume.**

***Index Terms*—High-voltage direct current (HVDC) transmission, modular multilevel converters (MMCs), power converters, modular systems, energy storage systems, supercapacitors, ancillary services, fast frequency response.**

I. Introduction

In response to the rise of the energy consumption and global environmental concerns, renewable energy sources have been grown at a fast pace in the recent years [1]. Unlike the conventional sources mainly used in the past in electric power transmission systems, their variability and remote location will change the power system operation. As a solution, High Voltage Direct Current (HVDC) has become a suitable technology to transmit bulk power over long distances [2]. This on-going expansion leads to a high number of Power Electronics (PE) devices that are connected to the grid with no inertia since frequencies are decoupled. Consequently, the inertial response of the grid is degraded and the system frequency fluctuation becomes more prominent after severe contingencies [3].

Grid scale Energy Storage Systems (ESSs) have emerged as a promising alternative to enhance the reliability of power supply by providing multiple services [4]. Traditionally, they have been used for bulk energy storage by connecting battery modules in series to a centralized DC bus with a PE stage between batteries and AC grid to provide operating reserves [5]. Since a few years, research efforts are looking to split the ESS inside converters to benefit from the attractiveness of a high modularity and the new control opportunities that can be provided.

In this context, modular multilevel systems have received a significant interest [6]–[8]. Instead of using a common DC bus, the ESS can be freely distributed among the submodules (SMs) [9] and controlled independently at a converter level. The first publications about modular structures with ESS focus on Cascaded H-Bridge Converter (CHB) and Modular Multilevel Converter (MMC) topologies but solely for the purpose of connecting an ESS to the grid at medium voltage level [10]–[14]. Recent works are dedicated to the combination of ESS and MMC for the enhancement of HVDC converter stations, used in point-to-point links, with an energy storage function [15]–[21].

Since in an MMC-HVDC application, the SM capacitor voltage cannot vary according to the State of Charge (SoC) of the ESS, a direct connection is not reasonable. Indeed, the presence of voltage ripples, due to switched current, at the terminals of the SM capacitor participates to reduce the lifetime of the ESS [22]. Therefore, passive filters and proper control methods were proposed for batteries to integrate them into SMs [14], [19], [23]. However, the high SM capacitor voltage leads to a complex series connection of cells in addition to no voltage decoupling. Thus, the insertion of a DC-DC converter is compulsory [7], [14]–[17], [24], [25]. A single stage DC-DC converter is generally assumed and the design of the solution is rarely considered.

This paper pays special attention to the conception of this interface converter. It consists in determining the suitable interface converter with its energy storage element to achieve the desired energy exchange to provide ancillary services [20]. Several topologies are compared before illustrating the advantages of a modular design. These advantages include a better power density. In addition, this paper provides a control strategy that enables to mitigate the low frequency fluctuations of a SM and equalize the SoC of the storage elements without modifying the overall control of the MMC. The paper is organized as follows. Section II recalls the fundamentals of

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an MMC and the specifications of the considered application. In Section III, the comparative analysis is introduced. In Section IV, the control concept and simulation results of the proposed interface converter are presented. Section V depicts the experimental results and Section VI concludes with the advantages of the proposed solution.

II. Specifications

The general structure of a 3-phase MMC is illustrated in Fig. 1. Each converter leg comprises an upper and lower arm that consists of a set of identical half-bridge SMs.

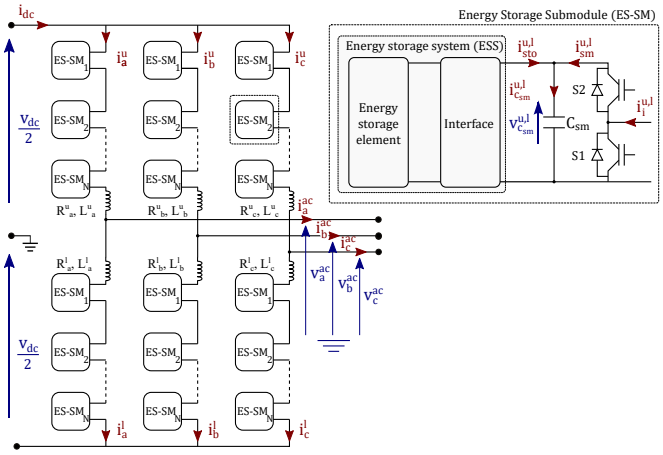

Fig. 1: Topology of an MMC with ES-SMs (Note that the classical configuration of an MMC is obtained when ESSs are not fitted)

In an MMC, the stored energy (typically 30 MJ for a 1 GW converter [26]) is extremely small compared with a conventional AC power plant or grid scale ESS. For this reason, the converter cannot provide ancillary services to the AC power system. Generally, some of these short-term services, such as primary reserves [27] and particularly the relatively new fast frequency response services [28]–[33] require low energy capabilities from a grid perspective but reasonably high in comparison to the stored energy inside an MMC. However, the requested powers only represent a small part of the converter rating [16]. A typical maximum power reserve for a single entity varies from 25 to 50 MW and it has to be provided during a minimum support time to assist the establishment of frequency containment reserves with time delay [30], [32].

This implies that, by increasing the energy stored with energy storage elements, this solution is feasible without significantly affecting the design of the MMC. Similar enhanced Flexible AC Transmission Systems (FACTS) with an energy storage function have already been implemented to face fast frequency challenges with a 50 MW power capability during 10 seconds [34]. In this paper, it is assumed that an energy storage element is connected to each SM capacitor through a DC-DC converter to make an Energy Storage Submodule (ES-SM) as shown in Fig. 1. These interfaces are controlled to track a power reference given by the high-level control of the MMC. Energy is thus exchanged between the energy storage element and the SM capacitor. Otherwise, the MMC acts as if no ESS is included.

The requirements for the present work are as follows. A 1 GW-MMC [26], [35], [36] has to provide 5% of its power rating with an energy capacity of 900 MJ, which stands for a full output power during 18 seconds. Regarding the MMC features, data are taken from the INELFE project [26], [37].

Nowadays, supercapacitors have become an attractive alternative for short-therm applications [34] with high power density since the recent progress has led to greater capacitances and energy densities. Because the energy is stored electrostatically, a high number of cycles at full power is possible with a high reliability and a very long life span. Moreover, the maintenance of an MMC is simplified since they can be fully discharged contrary to batteries. Because of the aforementioned reasons, supercapacitors have been selected as energy storage devices.

III. Interface Converter Topology Selection

This section is dedicated to the choice of the topology of the interface converter between the energy storage element and the capacitor of an ES-SM. In the literature, most authors assumed a single stage bidirectional converter (Fig. 2a) owing to its simplicity [7], [12]. Interleaved converter (Fig. 2b) was also mentioned in [15], [16]. Note that isolated topologies, such as a Dual Active Bridge converter [8], [15], are omitted here, because galvanic isolation is not compulsory and would increase the cost and size. To the best of our knowledge, a modular converter with N_{mod} subconverters (Fig. 2c) has never been studied in the context of an MMC with an energy storage function. In this section, a sizing methodology, based on analytical calculations, is given for the main components of these converters. Then, it is applied to the different DC-DC converters shown in Fig. 2 to identify the most attractive topology. The attractiveness of a converter is assessed here thanks to its cost and volume. This is mainly motivated by the fact that the present volume of a SM is large and the mechanical assembly of SMs is complex. Therefore, the introduction of an energy storage function must not lead to a drastic increase of the volume of a SM.

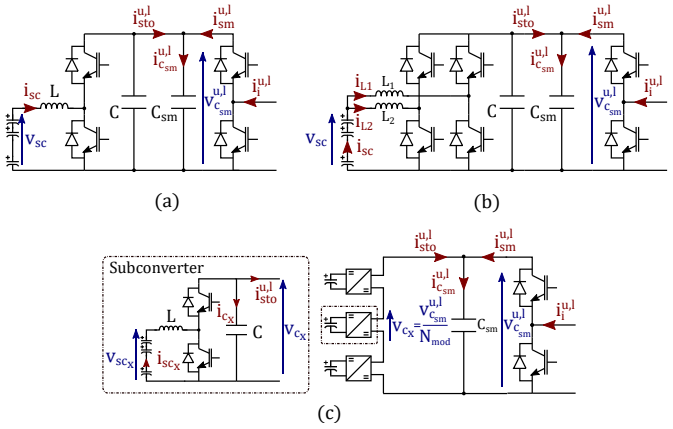

Fig. 2: Interface converter topologies compared in this paper with: (a) Single stage converter (b) Interleaved converter (c) Modular converter.

A. Methodology and assumptions

In order to compare the different variants, each ES-SM is sized to achieve the energy and power requirements introduced in section II. These constraints lead to define the number of required supercapacitors but also to the determination of the passive components and the needed switching devices. A supercapacitor stack consists of N_s cells with a capacitance C_{cell} in series in a branch and N_p branches in parallel as shown in Fig. 3 (Note that in this paper, the term cell refers to a supercapacitor). For such a stack, the total energy stored W_{sc}^{tot} depends on the voltage at its terminals v_{sc} and its equivalent capacitance C_{sc} as described in (1) considering ideal components.

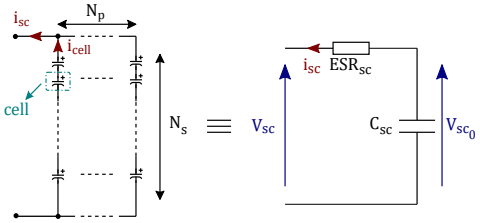

Fig. 3: Topology of a supercapacitor stack

$$W_{sc}^{tot} = \frac{1}{2} C_{sc} v_{sc}^2 = \frac{1}{2} \frac{C_{cell} N_p}{N_s} v_{sc}^2 \tag{1}$$

Consequently, many combinations of N_s and N_p are possible for a given energy requirement. From this, an optimization process is conducted. The approach consists in sizing an ES-SM for all the depths of discharge and different supercapacitor cell values from 25 to 3000 F [38]. The goal is to minimize the total cost of the energy storage system by finding the combination of the number of cells (N_s, N_p) and their capacitance. For the result which minimizes the cost of the stack, the voltage range ($v_{sc_0}^{min}$ and $v_{sc_0}^{max}$) is obtained and the passive components are sized. Note that the goal is to minimize the stored energy to the bare minimum. Since the energy storage element represents most of the cost of the ES-SM and since its cost and volume evolve approximately linearly with the stored energy, the volume is also optimized. Then, the best solution for each topology is retained and these results are compared in sub-section III-B. In the next paragraphs, the different models used for designing the ESS of an ES-SM (see Fig. 2) are succinctly developed.

1) Sizing of the supercapacitor stack: The supercapacitor stack is sized considering a constant power discharge/charge per ES-SM, P_{sm}. It corresponds to the additional power that should be supplied by the MMC divided by the number of ES-SMs. Internal losses, due to the equivalent series resistance ESR_{sc} of the supercapacitor stack, are also taken into account as shown in Fig. 3. In reality, the usable energy W_{sc} of a supercapacitor stack is only a fraction of W_{sc}^{tot} which depends on the maximum $v_{sc_0}^{max}$ and minimum $v_{sc_0}^{min}$ allowable internal voltage:

$$W_{sc} = \frac{1}{2} \frac{C_{cell} N_p}{N_s} \left(v_{sc_0}^{max^2} - v_{sc_0}^{min^2} \right). \tag{2}$$

However, these voltages are not equal to the maximum and minimum voltage at the terminals of the stack v_{sc}^{max} and v_{sc}^{min} since they are dependent on its equivalent series resistance and the load current i_{sc} as observed in Fig. 3. At constant power, the voltage $v_{sc_0}^{min}$ is limited by the internal resistance of the stack. Consequently, the depth of discharge cannot be chosen arbitrarily such as [39]:

$$v_{sc_0}^{min} \geq \sqrt{4 ESR_{sc} P_{sm}}. \tag{3}$$

At the same time, the power provided by all the supercapacitors in one stack must be high enough to satisfy the power requirement. Otherwise, additional branches of cells in parallel are necessary. The minimum voltage of the stack is also determined by its current capability criteria (4):

$$v_{sc}^{min} \geq \frac{P_{sm}}{N_p i_{cell}^{max}} \tag{4}$$

where i_{cell}^{max} is the current capability of one supercapacitor cell. This value is chosen in order to avoid an overheating within an ES-SM. In the worst case, the ESS can be cycled during a long period of time, with significant power changes, while its voltage remains close to its lower limit v_{sc}^{min}. It is then considered, here, that i_{cell}^{max} is the current that can be fed without increasing the cell temperature over a certain threshold. In a supercapacitor datasheet, this value is given as the maximum continuous current. Finally, the maximum voltage of the stack v_{sc}^{max} depends on the interface converter. Because the control of the voltage variation across the stack is considered as a degree of freedom, this value can be adjusted according to the desired depth of discharge, and so the number of supercapacitors in series. Note that, for the topologies investigated in Fig. 2, the stack voltage cannot be greater than the ES-SM DC bus voltage $v_{c_{sm}}^{u,l}$. This limits the number of series connected supercapacitors, with a rated voltage v_{cell}^{nom}, as follows:

$$N_s \geq \frac{v_{sc}^{max}}{v_{cell}^{nom}}. \tag{5}$$

Once the number of required supercapacitors (product of $N_s N_p$) is known, the volume and the cost of the stack can be easily estimated with data from manufacturers.

2) Considerations for switching devices: As seen in Fig. 2, several subconverters can be connected in series or in parallel depending on the interface converter topology. For each structure, an appropriate switching technology has to be selected. To withstand the high submodule capacitor voltage $v_{c_{sm}}^{u,l}$ (1.6 kV here), 3.3 kV IGBT power modules are necessary for a single stage (Fig. 2a) and for an interleaved converter with N_{ph} phases (Fig. 2b. Note that a topology with two phases is first considered). A 1 kHz switching frequency f_{sw} is considered, which is typically the case in those applications. Note that this switching frequency is higher than the typical switching frequencies used in MMCs. Even if the rated voltage is the same, the switched currents are quite different (up to few kiloamperes in the arms and few tens of amperes for the interface

converter). On the contrary, MOSFETs, with lower voltage and current capabilities, can be used with a modular converter because the high voltage is divided according to the number of subconverters N_{mod}. Thereby, the operating frequency can be highly increased. In this paper, a switching frequency of 50 kHz is selected while the number of subconverters is limited to 4, 5 and 7 because of the rating of the available semiconductors on the market.

3) Sizing of passive components: For each converter, the design of the passive components is pivotal. The inductance L for the desired current ripple Δi_{sc} (10%) and the intermediate capacitor C (see Fig. 2) for the requested voltage ripple Δv_c (5%) for each topology are calculated with the formulae from Table I. α is the duty cycle of a DC-DC converter and $i_{sto}^{u,l}$ is the current that flows from the ESS toward the main ES-SM capacitor C_{sm} as defined in Fig. 2. Note that, for Fig. 2a and 2b, C is in parallel with C_{sm}. However, the capacitance of the intermediate capacitor is relatively smaller in regard with the capacitance of the SM capacitor. This implies that it is not necessary to increase the value of the latter.

Topologies	Inductance	Capacitance
Single stage bidirectional	$\frac{\alpha(1-\alpha)v_{c_{sm}}^{u,l}}{f_{sw}\Delta i_{sc}}$	$\frac{\alpha i_{sto}^{u,l}}{f_{sw}\Delta v_c}$
Interleaved converter	$\frac{\alpha(1-N_{ph}\alpha)v_{c_{sm}}^{u,l}}{f_{sw}\Delta i_{sc}}$	$\frac{\alpha i_{sto}^{u,l}}{N_{ph}f_{sw}\Delta v_c}$
Modular converter, subconverter	$\frac{\alpha(1-\alpha)v_{c_{sm}}^{u,l}}{N_{mod}f_{sw}\Delta i_{sc}}$	$\frac{\alpha i_{sto}^{u,l}}{f_{sw}\Delta v_c}$

TABLE I: Passive components calculation

To evaluate the volume of the inductor, a double E-core is considered as shown in Fig. 4. Its dimensions can be expressed as a function of a scale parameter a. This characteristic length can be deduced from the sizing of the core A_e and the winding A_w areas based on the magnetic stored energy relation [40]. The core should comply with the design value of the inductor such as:

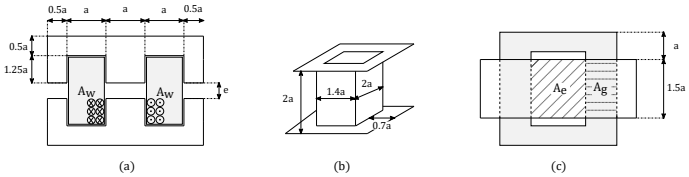

Fig. 4: Double E-core: (a) front view (b) coil support (c) top view

$$A_e \geq \frac{L i_L^{max}}{N_{coil} B_{max}} \tag{6}$$

where B_{max} is the maximum core flux density, i_L^{max} the maximum current that flows through the inductor and N_{coil} the number of turns. Assuming that the air gap reluctance is high in comparison with the core reluctance, the inductance is expressed by:

$$L = \frac{\mu_0 N_{coil}^2 A_g}{2e} \tag{7}$$

with e the air gap length, A_g the air gap cross-section and μ_0 the air magnetic permeability. Similarly, wires must fit through the core window A_w as:

$$A_w \geq \frac{N_{coil} i_L^{max}}{J_{max} K_b} \tag{8}$$

with K_b a window utilization factor (here 0.55) and J_{max} the maximum current density (here 5 A/mm^2) of the copper conductors. By satisfying constraints (6), (7) and (8), the core size can be thus roughly determined. Regarding materials, ferrite and amorphous are respectively used for MOSFETs and IGBTs. The characteristics of magnetic circuits are based on products available on the market [41], [42] while the cost of inductors are evaluated on the quantity of raw materials and copper. Finally, the volume of the intermediate capacitor C is calculated by extrapolating the evolution of the volume of polypropylene capacitors as a function of the energy stored for a range of data from [43].

B. Comparison of results

For each considered topology for the interface converter, the results of the sizing methodology, presented in subsection III-A, are compared in Fig. 5.

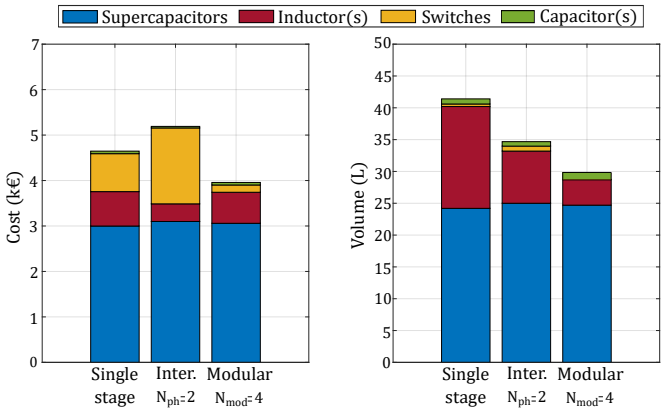

Fig. 5: Cost and volume comparison of the interface converter for the three topologies of ES-SM considered in Fig. 2

First, one can notice that the supercacitor stack represents the main cost of the ESS. Moreover, it is similar for all topologies. This implies that this cost is directly linked to the stored energy.

Secondly, it can be observed that a modular interface converter has a lower cost and volume. Regarding the volume, the inductor is mainly responsible for this wide gap. For topologies without a series connection of subconverters, the low switching frequency of IGBT modules leads to large inductance values (see Table I), which can be not practicable. Conversely, a modular converter, based on MOSFETs, permits to operate at high frequency and to drastically reduce the total magnetic energy stored within the interface converter. Thus, the size of the magnetic components is reduced. Even if an interleaved converter also provides the same opportunity, by decreasing the current that flows through the inductors, the gain remains not significant and the cost is prohibitive. This is

because the costly IGBT modules are duplicated according to the number of phases N_{ph}. Moreover, for this application, the ESS current $i_{sto}^{u,l}$ is low (i.e. 13 A_{rms}) compared to the current capability of 3.3 kV IGBTs (i.e. few hundreds of amperes). Note that the following observation can also be made for IGBT modules. The higher the voltage class, the higher the current capability but the lower the switching frequency [44]. To avoid prohibitive inductances in interface converters, the solution is then to stack high frequency subconverters in series. In addition, 600V MOSFETs, for instance, are much less expensive than 3.3 kV IGBTs. This can decrease the cost of the solution although the number of needed switches is higher. They can be operated at their optimal voltage and current range with a modular topology in opposition to IGBT power modules which are underused and more expensive as seen in Fig. 5. Finally, a modular structure also allows the implementation of a potential fault tolerant mode and promising control perspectives. As an example, advanced control methods can be implemented in a near future to manage the temperature of each supercapacitor stack so as to improve their lifetime.

Lastly, the parameters of the optimum ESS design are listed in Table II. Next section deals with the control of this interface converter.

Parameters	**Values**
Energy Storage Submodule (ES-SM)	
SM capacitor voltage, $v_{c_{sm}}^{u,l}$	1.6 kV
SM capacitor, C_{sm}	10 mF
Maximum power, P_{sm}^{max}	20.83 kW (1 p.u.)
Interface converter	Modular topology
Number of subconverters, N_{mod}	4
Subconverter characteristics	
Switches	MOSFET 600 V
Operating voltage, v_{c_x}	400 V
Inductance, L	0.91 mH
Intermediate capacitance, C	13 μF
Number of supercapacitors	115 (one row)
Supercapacitor cell, C_{cell}	Maxwell 310 F
Maximum supercapacitor stack voltage, v_{sc}^{max}	310 V
Usable energy, W_{sc}	95 kJ

TABLE II: Main parameters of the chosen design for the ESS

IV. Control of the proposed interface converter

A. Control objectives

The main goal of the control scheme is to ensure that the correct amount of power is exchanged from the ESSs to the SM capacitors when an ancillary service is needed. For an MMC without embedded ESSs, the submodule capacitor voltages are controlled by the overall MMC control. However, in presence of a storage unit, some changes are required in this energy management. Several publications propose to use the energy of the ESS to keep this voltage constant with the help of the interface converter [14], [24], [25]. Consequently, the control structure is significantly different from the case without ESSs. As the goal is only to add a storage function to extend the set of services of the converter, a better approach consists in decoupling the management of the ESSs and the MMC control. In this instance, the overall control remains unchanged and the inclusion of ESSs does not lead to significant changes [16], [45] since these additional power sources are seen as a disturbance for the energy control. The classical energy control loops of an MMC are able to deal with this disturbance to keep stable the SM capacitor voltage (e.g. by sending energy to the AC side when ESSs feed energy). In this paper, this philosophy is thus considered. Note that the effectiveness of this strategy has already been demonstrated in [20], using an arm average model, and in a more detailed manner in [16], [46] considering the low level control (i.e. capacitor voltage balancing algorithm) of an MMC.

Moreover, large uneven load distribution among subconverters is not acceptable since components are not sized to support significant variations. The voltage at the intermediate capacitances v_{c_x} must be well-distributed.

In addition, the current $i_{sm}^{u,l}$, that flows toward the floating capacitor of an ES-SM, corresponds to the switched arm current $i_i^{u,l}$ which is composed of an AC and DC component. Inevitably, this current contains AC components and steep pulses. It leads to a voltage variation at the SM capacitor terminals which are thus reflected at the ESS side [22], [23]. They induce a current with low frequency components at least at the line and double line frequency that may deteriorate the supercapacitor stack lifetime and cause its oversizing. The control of the interface converter must mitigate these ripples to ideally create a pure DC current in the stack.

Finally, the proposed topology relies on several subconverters. Each of them has its own supercapacitor stack with natural discrepancies in their electrical parameters due to manufacturing process. Consequently, unbalanced aging occurs over time. It is then necessary to implement balancing strategies to avoid that SoCs of the supercapacitor stacks diverge from one to another. Similarly, a control method has to be designed to maintain an average SoC over time to deal with inherent ohmic losses during successive discharging (or charging) events and ensure a minimum energy content.

To comply with the control objectives mentioned above, Fig. 6 shows the proposed control architecture of the interface converter that will be discussed in the next subsections.

B. Control of the output power

According to the aforementioned objectives, an active power set-point P_{sm}^{*} is assigned to the ES-SM and equally distributed among the N_{mod} subconverters. This reference is further translated in a current reference for each supercapacitor stack based upon the measure on their voltage v_{sc_x} with $x \in \{1,..., N_{mod}\}$. This inner current loop is illustrated in black in Fig. 6. Because the SM capacitor voltage is regulated by the MMC control, all subconverters must have an additional outer voltage loop (in violet) except one which has its voltage indirectly controlled. In this way, as the subconverters are in series, one of them controls the current $i_{sto}^{u,l}$ while the others ensure the SM capacitor voltage, which is still managed by the MMC overall control, is well distributed. To avoid interferences between the inner current and outer voltage loop, the inner loop response time is set several times faster. Note that the average voltage $\overline{v_{c_x}}$ is regulated since the ES-SM capacitor voltage has inherent fluctuations. Thus, a second order Buterworth filter F_v is used. It is set to be faster than the voltage loop to be treated as a unitary gain.

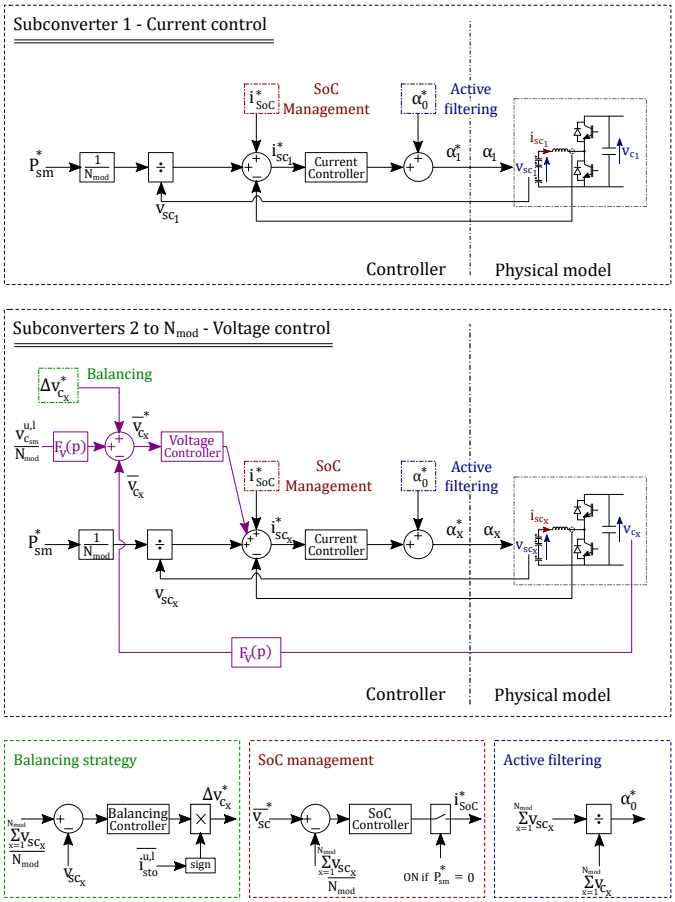

Fig. 6: Control architecture of the modular interface converter

C. Cancellation of voltage fluctuations

When the ESS is controlled to keep the ES-SM capacitor voltage constant, numerical filters can be added to the voltage control loop to suppress low frequency components [24], [25]. In the proposed control scheme, it is not feasible since only the power delivered from the ESS is regulated for one subconverter. To avoid AC components in the current that flows through the stacks, a control action is implemented as seen with the block diagram in blue in Fig. 6. The concept consists in superimposing the voltage fluctuations of the ES-SM capacitor on the duty cycle of each subconverter α_x with the help of a feedforward component α_0^*.

D. Energy management for supercapacitor stacks

The goal of this regulation is to address imbalance SoC issues. An additional SoC management also completes this controller with the aim of keeping the SoC of the supercapacitor stacks at a given level when they are unused. This is done to keep the stored energy at an appropriate level to deal with future requests. Note that their response time is set sufficiently slower than the previously mentioned voltage and current controllers to decouple control dynamics. Moreover, the related current should also remain low in order to not to impact the behavior of the ES-SM capacitor in normal operation. Fig. 6 presents block diagrams in green and red that illustrate those concepts.

1) Balancing strategy: This control forces each supercapacitor stack to follow the mean SoC value by adding a small variation $\Delta v_{c_x}^*$ on the voltage set-point of the associated subconverter. Since the branch current $i_{sto}^{u,l}$ is common, the power distribution can be slightly unevenly shared among subconverters. As a consequence, the charge and discharge rates in the supercapacitor stacks are not identical. This allows a controlled balancing. One can remark that it also implies to consider the sign of the power flow. If a stack has a voltage v_{sc_x} lower than the other stacks, when $i_{sto}^{u,l}$ is positive, it should be less discharged and its voltage v_{c_x} decreased. Conversely, if $i_{sto}^{u,l}$ is negative, this voltage has to be larger than for the other subconverters to provide more energy to this stack.

2) State of Charge management: This strategy imposes that each supercapacitor stack converges toward a given average voltage $\overline{v_{sc}}^*$ when the energy storage is not used ($P_{sm}^* = 0$), assuming the aforementioned balancing controller is fast enough. Note that a long time response is chosen to limit the effect of this action on the ES-SM capacitor and make it unnoticeable for the MMC operation.

E. Simulation results

In this subsection, to validate the effectiveness of the proposed control, simulations of an ES-SM are carried out in MATLAB/Simulink. The interface converter with its supercapacitor stacks is modelled with an average model and connected to a capacitor with a controlled current source in parallel to model the current $i_{sm}^{u,l}$. To simulate realistic conditions, a detailed model of an MMC, where each SM in an arm is individually represented, has been used to generate the switched waveforms of this current. The real dynamics of the converter are thus conserved. Specifications are the same as stated in Section II and Table II.

In Fig. 7, the voltage and current waveforms in an ES-SM, when no energy is requested from the ESS, are presented. Fig. 7a shows that the oscillating voltage at the ES-SM capacitor is correctly distributed between subconverters. If the cancellation of voltage fluctuations is not introduced, fluctuations are reflected in the supercapacitor stack as seen in Fig. 7b and 7c. This implies the presence of harmful low frequency current components. By contrast, the dynamic clearly changes in presence of the proposed active filtering. As shown in Fig. 7b and 7c, those ripples are removed which leads to greatly improve the performance of the supercapacitor stack over its lifetime.

The obtained results with the proposed energy management are illustrated in Fig. 8. The ESSs of the MMC are used to provide a symmetrical response of 25 MW, which means 0.5 p.u. by ES-SM (see Section II and Table II). The time response is limited at 500 ms since these new ancillary services can require a maximum activation time comprised between 500 ms and 1 second [28]–[33]. The supercapacitor stacks are thus discharged and charged successively after their SoCs are randomly initialized as seen in Fig. 8b. Fig. 8a and 8c show the power p_x for each subconverter and the variations of the average voltage at their intermediate capacitance $\overline{v_{c_x}}$. As observed, the ES-SM provides the requested power. As

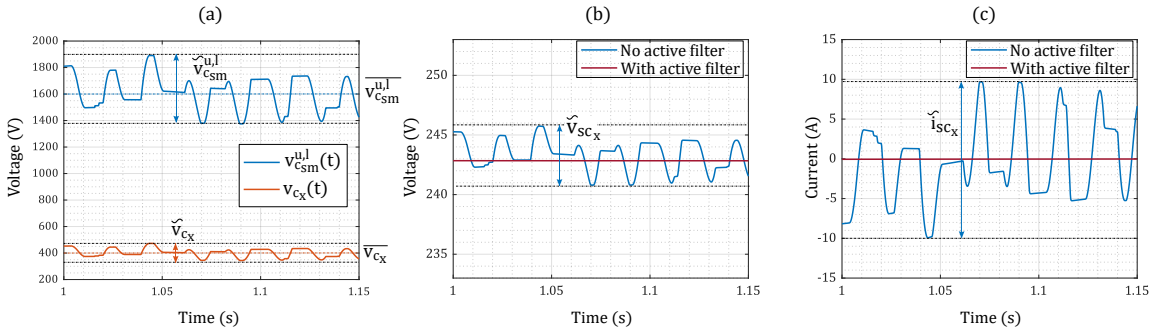

Fig. 7: Steady state simulation results with: (a) ES-SM capacitor voltage and intermediate capacitance voltage (b) Supercapacitor stack voltage (c) Supercapacitor stack current

long as the correct amount of power is supplied to the ES-SM capacitor, the structure of the interface converter does not change the dynamics of the ES-SM capacitor voltage and the ancillary services that have to be provided by the MMC with ES-SMs. Finally, the voltage of the supercapacitor stacks clearly converges in Fig. 8b. This means that the unequal power distribution strategy for the balancing purpose works correctly.

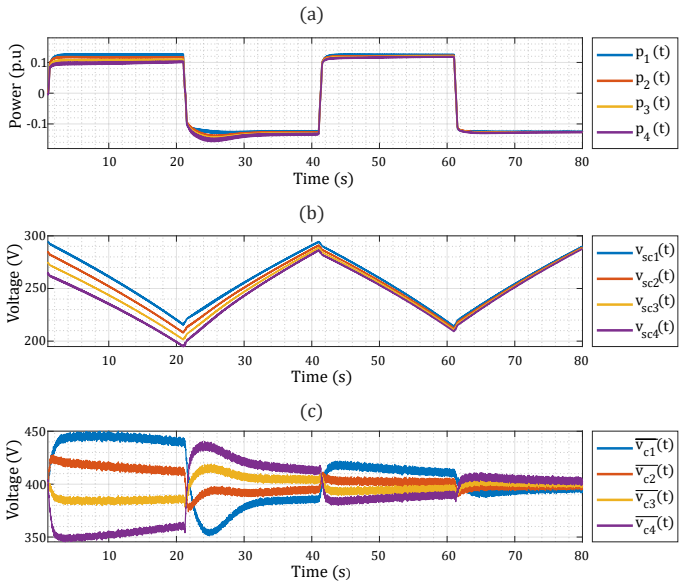

Fig. 8: Simulation results of the energy management scheme with: (a) Power exchanged per subconverter (b) Supercapacitor stack voltages (c) Intermediate capacitance average voltages

V. Experimental results

In order to validate the proposed concept and control methods, a downscaled prototype of an ES-SM has been designed and a controller has been implemented with a rapid control prototyping approach. The overview of the test bench and its schematic representation, with the main parameters, are shown in Fig. 9 and 10.

The board is based on a connection of three subconverters in series, with split supercapacitor stacks connected to a main capacitor powered by an external bidirectional power supply. Each of them consists in an half-bridge converter with a stack

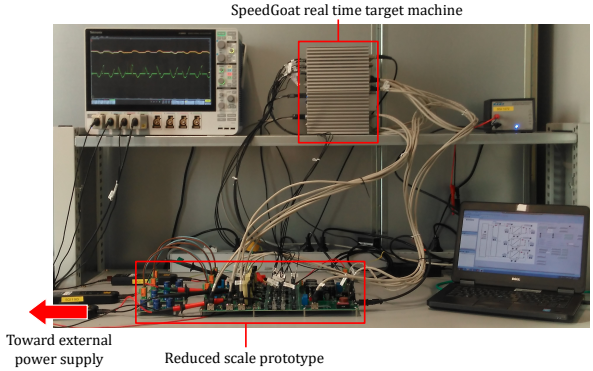

Fig. 9: ES-SM downscaled prototype test bench

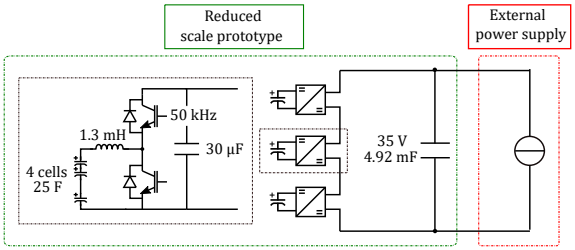

Fig. 10: Schematic of the downscaled prototype

of four supercapacitors of 25 F in series with a self-controlled cell balancer to avoid over-voltages. The ES-SM mock-up and the power supply are controlled by a SpeedGoat FPGA real-time target machine. The high level control algorithm, developed under Simulink, is thus directly imported from a workstation. The FPGA retrieves all the necessary measurements from the board. It generates the modulation signals, transmits the firing signals by fiber optics and manages the protection of the test bench.

For the purpose of the test, the regulation of the ES-SM capacitor voltage is performed by controlling adequately the power supply in order to generate a current shape $i_{sm}^{u,l}$ similar to what can be observed in a conventional MMC. This means that a balancing control algorithm of the SM capacitor voltages is emulated, and a switched current from the power supply is provided as if the ES-SM belongs to an MMC arm. As a results, the capacitor voltage dynamics is kept with a non-smooth slope (i.e. a constant ES-SM capacitor voltage denotes the ES-SM is bypassed in the MMC arm). Fig. 11 illustrates

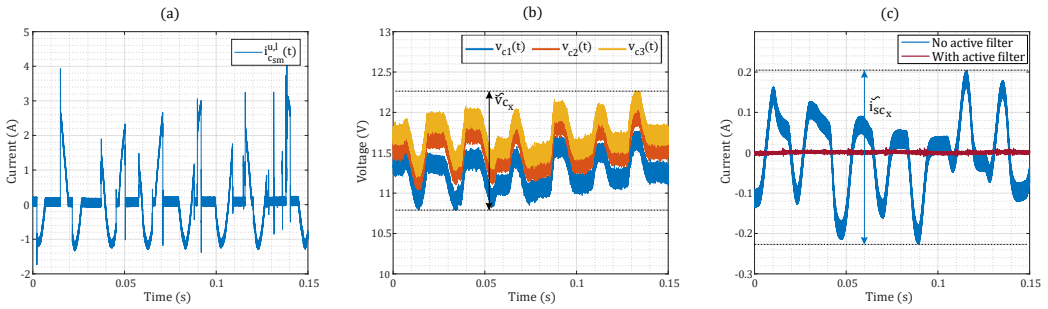

Fig. 11: Experimental results during normal operation ($P_{sm} = 0$) with: (a) ES-SM capacitor current (b) Intermediate capacitance voltage of each subconverter (c) Supercapacitor stack current

the main waveforms for an idle operation mode with no energy exchange. A detailed view of the switched ES-SM capacitor current is depicted in Fig. 11a. It leads to fluctuations on the ES-SM capacitor voltage which are correctly distributed among the three subconverters thanks to the proposed control scheme as seen in Fig. 11b. Note in Fig. 11c that the current in a supercapacitor stack does not contain low frequency components when the active filtering is enabled.

Finally, the ESS is used to absorb or provide energy. The balancing control scheme is tested in Fig. 12. At first, this control was disabled and the supercapacitor stacks were charged and discharged successively with a symmetrical load profile. This led to unbalanced stack voltages as seen in Fig. 12a and d. The balancing controller is turned on at $t = 1350$ sec. From there, it creates an unequal power distribution among subconverters. It can be seen that significant SoC differences lead to larger variations on the intermediate capacitor voltages as shown in Fig. 12c. After several cycles, SoCs are well-balanced as shown in Fig. 12d. Similarly, the average SoC is kept constant throughout the whole test. This implies that the SoC management works properly. Note in Fig. 12b that transients are present on the ES-SM capacitor voltage, which is due to the energy based control scheme used to emulate the MMC control. On the test bench, this loop has a limited time response compared to the faster action of the ESS.

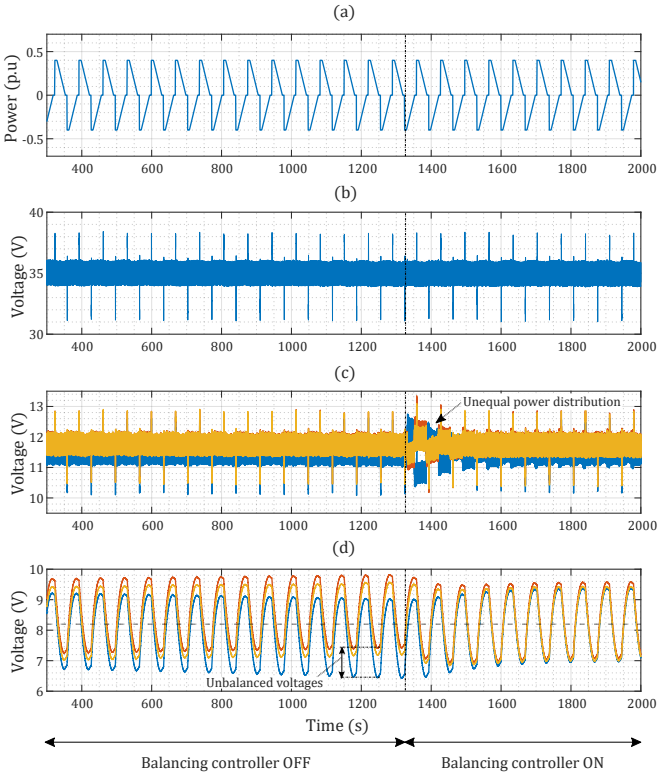

Fig. 12: Experimental results of the proposed energy management strategy with : (a) Power exchanged from the ES-SM (b) ES-SM capacitor voltage (c) Intermediate capacitance average voltages (d) Supercapacitor stack voltages

VI. Conclusion

This paper introduces an interface converter for a submodule of an MMC-HVDC with embedded storage to provide fast frequency services. It is often quoted in the literature that this solution can enhance grid stability. However, the technical issues regarding the interface converter between the SM capacitor and the energy storage element is rarely discussed. Therefore, the design and the control of this structure have been investigated. Supercapacitors have been interfaced to the submodule capacitor by the means of a non isolated modular converter made of a series connection of half bridge subconverters using fast switching semiconductors such as MOSFETs. The proposed interface converter offers an additional degree of freedom to the designer for implementing an appropriate ES-SM. Fast switching semiconductors used close to their rated values allows to reduce the total cost and volume of the solution. In this paper, typical switching frequencies have been considered and further works can be performed to define the optimal switching frequency for each considered topology. To some extent, it would help to minimize a criterion such as volume or cost. From an energy management standpoint, the proposed ESS control is independent from the conventional MMC control, which remains unmodified, as if there were an auxiliary power source for the submodule capacitor. By simply receiving a power set-point, additional energy can be brought to adjust the internal energy of an MMC when AC and DC powers are decoupled. From a systemic point of view, the interface converter acts identically, and with the same level of performance, as other converters in the literature. Besides, further studies could be carried out to compare the different perspectives of control implementation of the ESS at the MMC level. An energy management scheme is also proposed to

address balancing issues of the distributed ESSs within a submodule. Moreover, to avoid performance degradation due to the inherent low frequency components of an MMC, an active filter has been designed. In addition, attractive energy management perspectives are offered by dividing the ESS in several subconverters rather than having a long row of supercapacitors as mentioned. Finally, to validate the concept, the feasibility of the solution has been demonstrated in simulations and on a downscaled prototype.

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