Analog Duty Cycle Controller Using Backgate Body Biasing For 5G Millimeter Wave Applications

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***Abstract*—This work presents the first 21 - 43 GHz CMOS analog Duty Cycle Controller (DCC) implemented in 28 nm FDSOI. The main application is millimeter wave mixers with CMOS digital signals. The proposed circuit corrects the input duty cycle with a negative feedback analog loop. Observability of the duty cycle is made through a passive low pass filter and the control is achieved by modifying the rise and fall time of the input clock signal, via backgate biasing of an inverter chain. The circuit has been validated by post layout, Monte-Carlo and corner simulations. At 28 GHz, the duty cycle correction range varies from 40 % to 55 %, and the additional power consumption introduced by the correction loop is frequency independent and is equal to 0.6 mW.**

***Index Terms*—CMOS, 28 nm FDSOI, Duty Cycle Controller, Millimeter Wave Frequency, Body Biasing**

I. Introduction

In many applications such as millimeter wave mixers, it is mandatory to have a good control over the duty cycle. One efficient way to achieve this goal is using a duty cycle control (DCC). The duty cycle correction can be implemented fully in digital [1], in analog [2] or in mixed mode [3], and often includes a feedback loop path control. In many cases, the duty cycle is controlled with a current starving method, by modifying the rise and fall time of the signal (also known as pulse stretching/shrinking introduced in [4]). The sensitivity of the duty cycle to the rise and fall time is proportional to the operating frequency. The parasitic elements introduced by the DCC circuit will limit its speed. Currently, the highest frequency of operation for DCC circuit in literature is 10 GHz [2]. As the data transmission rate demand is rising, wide band telecommunication systems are driven towards millimeter wave frequency of operation, and there is a need for low power, high speed DCC with acceptable jitter performance. Usually, millimeter wave frequency signals are propagated using differential Current Mode Logic (CML) blocks to guarantee a 50 % duty cycle and the phase alignment of the complementary signals. However, it is difficult to achieve high output swing as well as fast rise and fall time. Therefore, a CML-to-CMOS circuit is often implemented at the end of the clock tree to provide the latter performance. The CML-to-CMOS is typically designed as a chain of CMOS inverters with increasing W/L ratio, in order to drive the input capacitive load of the mixer. At millimeter wave frequency, this operation degrades the duty cycle and phase alignments of the clock signal due to rise and fall time mismatches in the inverter chain. The main challenge is that the W/L ratio of the PMOS and the NMOS of one inverter must be tuned to match the capacitive load of the next inverter, however this next inverter ratio must also be tuned to match the capacitive load of the next stage, which will in return modify its input capacitance, leading back to another adjustment of the first inverter. Each new buffer added to the chain will increase the design complexity, and will also degrade the duty cycle at the output, as the duty cycle error is transmitted from one stage to another. Additionnaly, some capacitances are introduced by metal routing lines between stages and require another cycle of adjustment of the W/L ratio of each PMOS and NMOS of the inverters.

This paper proposes an analog DCC in 28 nm FDSOI, designed to drive millimeter wave mixers with CMOS digital signal. This circuit corrects the duty cycle error introduced by process variations, through the body biasing of a chain of inverters. This approach is well adapted for high frequency operation, as the duty cycle control is very fine, but most importantly because it does not add parasitic elements in the high frequency path. Initially designed to operate at 28 GHz, it reaches a maximum frequency of 43 GHz. The power consumption of the control loop is 0.6 mW and is frequency independent. At 28 GHz the inverter chain consumes 2.6 mW for a total power consumption of 3.2 mW.

Section II characterizes the effect of backgate biasing on the output rise and fall time of an inverter, and explains the operating principle of the DCC circuit. Section III presents simulation results and section IV concludes this paper.

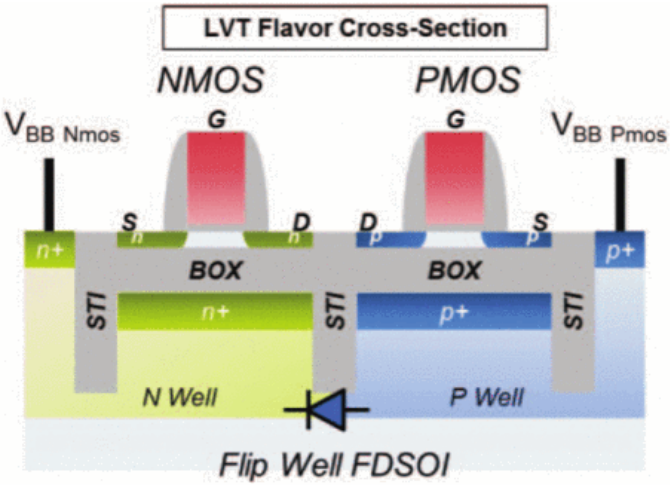

Fig. 1. Cross section of transistor NMOS and PMOS with a flipwell

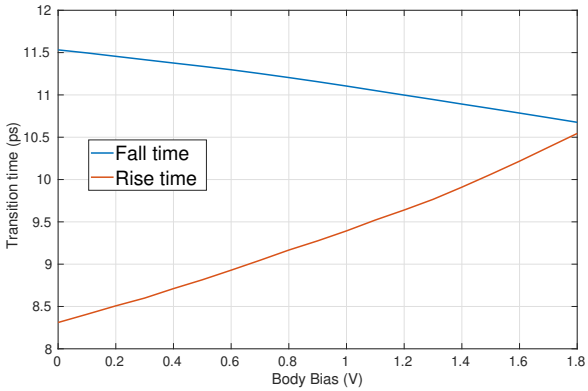

Fig. 2. Effect of Body bias on the rise and fall time of an inverter output

II. Duty Cycle Controller Architecture

A. Duty cycle control via backgate biasing

The design uses low voltage (LVT) flip well transistors, to benefit from lowest treshold voltage, and therefore the highest transition frequency. In 28 nm FDSOI, a modification in the backgate biasing ΔVBB of a transistor directly modifies its treshold voltage (ΔVt) as shown in Fig. 1. As explained in [5] the variation is linear, with a coefficient of $-85\,\mathrm{mV/V}$. By simulation, we verify that for a PMOS transistor :

$$\Delta Vt = \Delta VBB \times 0.087, \tag{1}$$

and for a NMOS transistor :

$$\Delta Vt = \Delta VBB \times (-0.098). \tag{2}$$

Fig. 2 shows the effect on the rise and fall time of an inverter driven by a rail to rail input, when the NMOS and PMOS have the same bodybias voltage. By introducing asymmetric rise and fall time, it is possible to control the duty cycle through pulse shaping. From the transition time variation (ΔTrf), it is possible to deduce the pulse width variation (ΔPwv) contribution from N bodybiased controlled inverters as following :

$$\Delta Pwv = (N) \times (\Delta Trf/2). \tag{3}$$

Based on this, the duty cycle (ΔDcy) control range for a given clock frequency with a period $Tclk$ can be expressed as :

$$\Delta Dcy = \frac{Tclk/2 \pm \Delta Pwv}{Tclk}.. \tag{4}$$

B. Circuit description

Fig. 3 shows the circuit implementation to realize the duty cycle correction function. The clock input is connected to a chain of three inverters with increasing W/L ratio. The first and second inverters implement the duty cycle control function, by

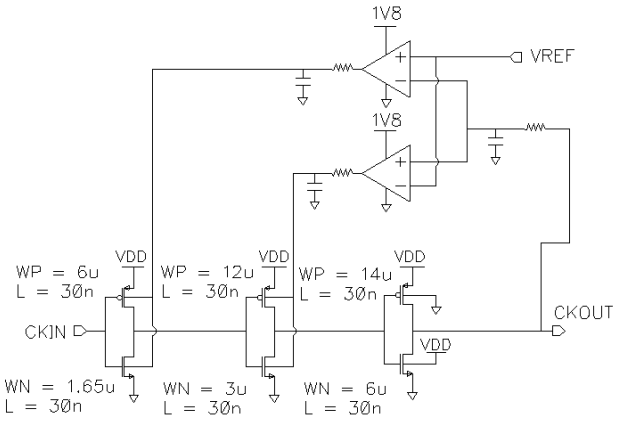

Fig. 3. Duty Cycle control Circuit schematic description

applying the same voltage to both the PMOS and NMOS body of the transistors, allowing to provide either fast rise time and slow fall time, or the reverse (Fig. 2). The clock output signal is filtered by an RC low pass filter which generates a DC value, equivalent to a direct image of its duty cycle. This signal is compared with the external voltage reference and injected in the negative feedback loop. The output of the two operational transconductance amplifiers (OTA) are filtered and respectively connected to the backgates of the first two inverters, to adjust the output duty cycle. The last inverter reshapes the signal and is biased to provide the fastest rise and fall time at the output.

C. Design implementation

From (4), it can be seen that the duty cycle control range is proportional to the clock frequency. This result is interesting because the process variation impact on duty cycle is also proportional to the operating frequency. Control range can be increased by adding more inverters to the chain, but it will result in higher power consumption, and increased jitter. A high gain for the two OTAs will reduce the closed-loop static duty cycle error. However, as the RC low pass filter extracts the DC value of the clock output with a delay, high gain and high duty cycle control sensitivity will lead to an unstable control

TABLE I
MAXIMUM DUTY CYCLE ERROR INPUT RANGE VERSUS OPERATING FREQUENCY

Frequency	15 GHz	21 GHz	28 GHz	35 GHz	43 GHz
Maximum	50.1 %	53.1 %	55.2 %	56.3 %	57.9 %
Minimum	43.2 %	41.5 %	39.8 %	40 %	41 %

loop. As the two OTAs are designed to work at DC frequency, they can be sized for a good matching. It is worth noting that as the two negative feedback loops are working in the same direction, an offset mismatch between the two OTAs will not result in a conflict between the feedback and does not generate instability. It will still impact the final output duty cycle value, in the same way as if the VREF voltage was changed. In this work, the targeted duty cycle is 50 %, therefore, VREF is set to VDD/2. To achieve a different duty cycle value, it is sufficient to adjust VREF linearly. The possible voltage range of the body bias extends from -3 V to 3 V. To reduce the number of supply domains, we fixed the bottom limit at 0 V. The upper range, fixed at 1.8 V, is the maximum voltage supported by the transistors used in the OTAs. A higher range of body bias voltage will directly increase the duty cycle control range of the circuit.

III. SIMULATION RESULTS

A. Duty cycle control range

As shown in Fig. 4, in order to characterize the DCC, simulations were carried out with a rail to rail input signal,for various frequencies, and duty cycles. Fig. 5 shows the maximum duty cycle error at the input, for which the DCC can guarantee a 50 ± 1 % duty cycle at the output. Table I presents the performance achieved at various frequencies. We compare this simulation result with (4) (from Fig. 2 we use ΔTrf = 2.5 ps. We also extrapolate the range for an increased number of body biased inverters in the chain. Up to 28 GHz, the first order approximation fits the simulation results, the center of the control range at 47 % instead of 50 % can be explained by the non idealities in the last inverter of the chain. The maximum frequency of operation is 43 GHz, for higher frequency, the loop is unstable. The unstability can be explained by the duty cycle observability through the first RC low pass filter : when the clock output duty cycle become 50 %, the DC value will reach VDD/2 after a delay linked to the RC constant of the filter. During this time the loop will still be modifying the duty cycle. If the loop gain is too high, or the delay is too long, the error produced at this time will prevent the loop from converging to a stable value. Fig. 6 shows the evolution of the body bias voltages during the convergence of the loop. As can be noted, the convergence of the backgate voltage is achieved at 300 ns.

B. Impact of process variation

When operating at millimeter wave frequency, it is recommended to use CML circuits to propagate the signal, as the differential structure provides duty cycle matching and phase

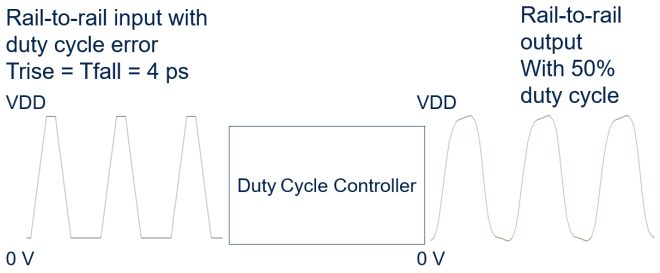

Fig. 4. Testbench for caracterization of the duty cycle input error range with rail-to-rail input signal

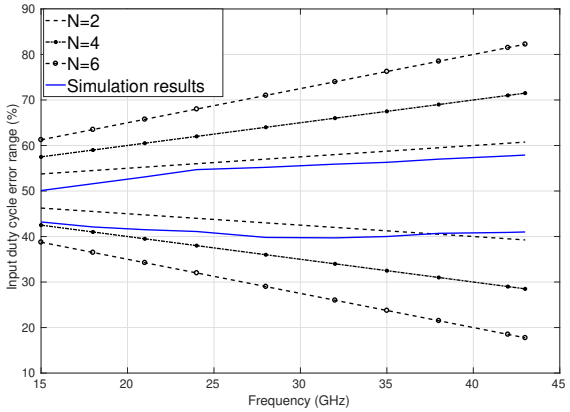

Fig. 5. Maximum duty cycle error at the input leading to 50 % duty cycle at the output, in function of the frequency of operation.

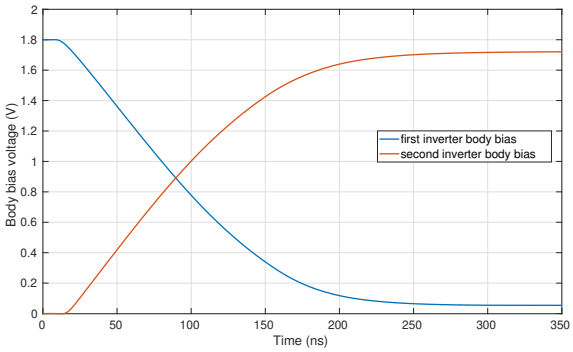

Fig. 6. Body bias voltage convergence for a 28 GHz input signal with 57.5 % duty cycle

TABLE II
OUTPUT DUTY CYCLE RESULTS FOR 120 MONTE-CARLO RUNS

Average	**Standard deviation**	**Minimum**	**Maximum**
50.3 %	0.17 %	49.9 %	50.8 %

TABLE III
OUTPUT DUTY CYCLE FOR CORNER SIMULATIONS

Corner	**FF**	**FS**	**SF**	**SS**
Output duty cycle	50.5 %	49.4 %	50.3 %	50.8 %

TABLE IV
COMPARISON WITH OTHER WORKS

Type of DCC	Mixed mode digital feedback [3]	Analog feedback [2]	All-digital [1]	This work
Process(nm)	NA	16	180	28 FDSOI
Operating frequency	4 GHz - 8 GHz	5 GHz - 10 GHz	1 GHz - 1.6 GHz	21 GHz - 43 GHz
Supply voltage (V)	1	0.8	1.8	1.1
Power consumption	5.83 mW at 8 GHz	1.8 mW at 8 GHz	4 mW	3.2 mW at 28 GHz
Correction Range	40 % - 60 %	20 % - 80 %	10 % - 90 %	41 % - 57.9 % at 43 GHz
Duty accuracy	$< \pm 1$ %	$< \pm 0.05$ %	$< \pm 1.4$ %	$< \pm 1$ %
jitter	1.61 ps at 8 GHz	NA	10 ps at 1 GHz	48 fs at 28 GHz

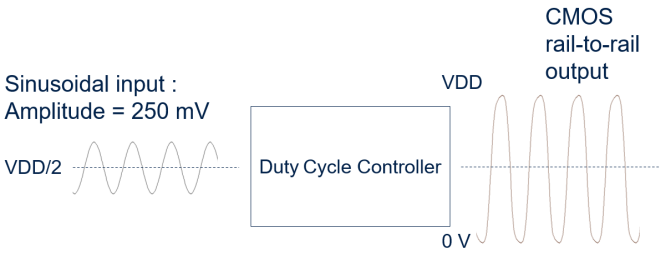

Fig. 7. Testbench for Monte-Carlo simulations with 250 mV amplitude ideal sinusoidal signal at the input

alignment. As shown in Fig. 7, we now simulate the DCC circuit with an ideal sinusoidal signal with amplitude of 250 mV at the input (first order modelization of the output of a high frequency CML amplifier). Table II regroups the results of 120 Monte-Carlo runs, with both devices and lots variations. Corner simulations results can be found in Table III. These results show that the presented DCC consistently converges to $50 < \pm 1$ % duty cycle, and appropriately corrects the duty cycle errors introduced by process variations. It is worth noting that in the case of a small amplitude signal at the input, the first order approximation of (4) is no longer correct, as for the first inverter, the determinant factor will be the threshold modification of the inverter through the body bias voltage, leading to a higher range of correction.

C. Jitter

The main source of jitter is introduced by the chain of three inverters. The jitter introduced by the control loop is negligible. By simulation, the σ rms jitter of the proposed DCC is 48 fs. In comparison to the period of a 28 GHz signal (36 ps), the jitter performance of this DCC is very good.

IV. CONCLUSIONS

In this paper we presented a DCC circuit operating at millimeter wave frequency. Initially designed to realize a CML-To-CMOS conversion at 28 GHz with 50 % output duty cycle in Monte-Carlo and corner simulations, we showed that it can also operate with rail to rail input from 21 GHz up to 43 GHz. The duty cycle correction range vary from 40 % to 55 % at 28 GHz. The power consumption is mainly due to the 3 inverter switching at high frequency. At 28 GHz, the inverter chain consume 2.6 mW and the correction loop consumes 0.6 mW, for a total power consumption of 3.2 mW. The proposed DCC performances are summarized and compared to other DCC architecture in table IV. This work achieves the highest operating frequency, with an acceptable power comsumption.

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