Transadmittance Efficiency Under NQS Operation in Asymmetric Double Gate FDSOI MOSFET

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Transadmittance efficiency in presence of NQS transport in Asymmetric Double Gate FDSOI MOSFET

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***Abstract*—The state of the art RF and millimeter-wave circuits design requires accurate prediction of the non-quasi-static (NQS) effects at high frequency for all levels of channel inversion. This work provides a practical insight to help high frequency performance assessment of UTBB FDSOI MOSFETs through a powerful frequency normalization scheme. Frequency dependence of small signal characteristics derived from experimental S-parameters are analyzed and reveal that the transconductance efficiency (g_m/I_D) concept, already adopted as a low frequency Analog figure-of-merit (FoM), can be generalized to high frequency, including under asymmetric operation. We report that the normalized frequency dependence of the generalized transadmittance efficiency (y_m/I_D) FoM only depends on the mobility and inversion coefficient (IC). In addition, this approach is also used to extract essential parameters such as the critical NQS frequency f_{NQS}.**

Keywords— NQS; HF; Transadmittance; Transconductance efficiency; gm over Id; Double-gate FETs; FDSOI; UTBB; Analog and RF; Low-Power; Low-Voltage

I. INTRODUCTION

RF CMOS based MOSFETs have been widely used in RF integrated circuits (RFIC) thanks to the geometry down-scaling. Critical issues related to short-channel effects have been mitigated using innovative architectures coupled with new materials [1]. The new architectures allow for higher level of integration and higher frequency operation of the CMOS technology. For analog and RF applications, the ultra-thin Body and Box (UTBB) fully depleted (FD) Silicon-on-Insulator (SOI) technology has proven to be relevant, especially when power consumption matters [1]. UTBB FDSOI MOSFETs exhibit high analog and RF performances thanks to the reduced parasitic capacitances and resistances. Moreover, the independent back gate allows threshold voltage and channel mobility controls [2][3].

In this work, the UTBB FDSOI MOSFET transconductance efficiency (g_m/I_D) is generalized and studied at high frequency for different channel inversion levels. The main attention is paid to the impact of Non-Quasi-Static (NQS) effect on the proposed transadmittance efficiency Figure-of-Merit (FoM), and in particular how a proper choice of the normalization factors ends with simple representation of this fundamental figure of merit, with special focus on low-moderate inversion levels. The goal is to provide RF designers with a practical tool for high frequency performance assessment. The paper is organized as follows. The device architecture along with the high frequency characterization are described in Section II. Next in section III we discuss and validate experimentally the generalization of the transconductance efficiency concept in UTBB FDSOI MOSFETs derived at low frequency in [3]. The distributed gate effects are assessed using high frequency measurements of large gate devices in Section IV, and an onset frequency of the channel NQS effect is defined and compared with transit frequency in Section V. The back gate transadmittance efficiency is also analyzed using TCAD simulations in Section VI. Finally, discussion and conclusion are presented in Section VII and VIII, respectively.

II. DEVICE DESCRIPTION AND CHARACTERIZATION

Measured UTBB FDSOI MOSFETs were processed at STMicroelectronics. Si film, BOX and equivalent gate oxide thicknesses are 7 nm, 25 nm and 1.3 nm, respectively. More details on the process can be found in [4]. DC and CV measurements are carried out to extract the device electrical parameters (e.g. threshold voltage $V_{TH,}$ oxide capacitance C_{ox}, etc.). In particular, the Inversion Coefficient (IC) is derived following the method in [3]. Multi-finger MOSFETs are embedded into CPW (Coplanar-Waveguide) transmission lines for high frequency characterization. After a standard short, open, matched load, and through (SOLT) calibration for reference plan definition, 2-port S-parameters are measured using ground-signal-ground (GSG) configuration probes up to a frequency of 110 GHz, under several DC bias conditions. All modes of operation are covered: non-saturation, saturation, weak inversion (WI), moderate inversion (MI) and strong inversion (SI). Measurements are de-embedded using Open-Short method. The gate lengths of the measured devices range from 28 nm to 1 µm, while gate widths range from 200 nm to 5 µm. Both N and P MOSFET types are measured and analyzed in this work. Comparable results are obtained for both types with a more pronounced NQS effect in the case of P type due to a lower carrier mobility. However, for reasons of limited space, only NMOS results are shown here.

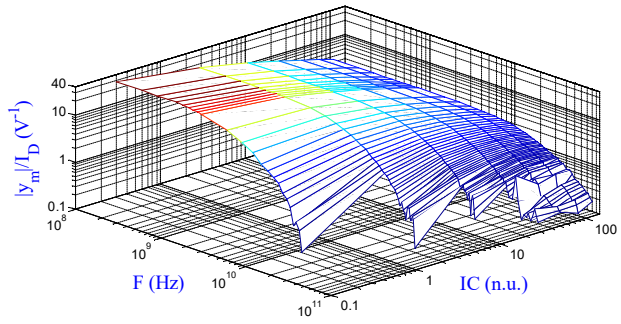

Fig. 1 3-D plot of the measured transadmittance efficiency modulus over I_D versus the frequency and inversion coefficient IC for L = 1 µm at V_{DS} = 1 V.

III. Frequency Dependence of the Transadmittance Efficiency in Long Channel UTBB FDSOI MOSFETs

In [3], the invariance of the transconductance efficiency, a well-known feature of bulk MOSFETs, was shown to remain valid for UTBB FDSOI MOSFETs that are controlled by two independent gates. This finding was not expected and constituted a major result for low frequency design methodologies. The detrimental impact of the high inversion level on the transconductance efficiency is further amplified under NQS operation, as shown in reporting the measured transadmittance efficiency modulus versus IC and frequency (F) in Fig. 1. Here, IC is the inversion coefficient defined as [3]:

$$IC = \frac{I_D}{\frac{W}{L} \cdot I_{spec}} \tag{2}$$

where I_D, L, W and I_{spec} are respectively the DC drain current, the MOSFET length, width, and the 28 nm FDSOI technology current estimated for the front gate at $I_{spec} = I_1 = 0.7028$ µA when assuming W = L [3].

Various models of NQS effect have been reported for bulk [5][6] and for common double gate MOSFETs [7][8]. A practical large signal model has also been published in [9]. However, none of these models proposes an exact analytical solution of the NQS behavior. To the best of the author's knowledge, the first analytical model of NQS in bulk MOSFETs valid in all regions of operation was derived in [10] which gave rise to a dimensionless powerful abacus where normalized transadmittances are represented in terms of normalized frequencies [11].

In this respect, we propose to investigate the front and back gates high frequency NQS behavior, and verify if this invariant still holds for UTBB FDSOI MOSFETs. As for the g_m/I_D figure of merit [3], we define the transadmittance efficiency as:

$$TE_i = \frac{y_{mi}}{I_D} = \frac{y_{DG} - y_{GD}}{I_D} \tag{1}$$

where y_{mi} is the mutual transadmittance defined as the difference between the gate-to-drain and drain-to-gate transadmittances, i.e. y_{dg} and y_{gd} respectively. The transadmittance efficiency is a generalization of the transconductance efficiency defined at low frequency operation.

At high frequency, the front or back gate transconductance is an imaginary number with a modulus and phase. Since g_{mi} represents the mutual interaction between the gate and drain, y_{mi} keeps the same meaning even for high frequency (note that y_{mi} reverts to g_{mi} at low frequency). It should be noted that the capacitive coupling attributed to C_{gd}, which dominates y_{DG} at high frequency, cancels in the definition of y_{mi}, as $y_{GD} \approx -j\omega C_{gd}$ [12] in the low frequency limit. Then, g_{mi} and y_{mi} assess the gate control of the intrinsic MOSFET channel. At low frequency (quasi static operation) we have [12]:

$$g_{mi} = real(y_{mi}) = |y_{mi}| \tag{3}$$

At any frequency, the y_{mi}/I_D FoM determines the gain and phase shift for a given DC current I_D. The evolution of the transadmittance efficiency versus frequency provides a very valuable insight in terms of power performances and efficiency at high frequency in presence of NQS effects.

At low frequency, it is well known that the transconductance efficiency is the highest in weak inversion as evidenced in [3]. However, at high frequency as shown in Fig. 1, the NQS transport degrades the low frequency efficiency, in particular for weak and moderate inversion (IC < 10). This is also illustrated in Fig. 2, a side view of Fig. 1. The higher efficiency of the moderate and weak inversion modes (i.e. $g_{m1}/I_D > 10$) does not hold anymore beyond F = 4 GHz for L = 1 µm. Moreover, beyond 13 GHz and unlike in low frequency operation, strong inversion performs better with regards to the transadmittance efficiency. At high frequency, the lower cut-off frequency (lower current) in weak inversion results in a lower transconductance efficiency. Indeed, at high frequency, the transit time is large below the threshold, and the current lags behind the voltage excitation. Conversely, in SI, the transit time is small and, even though the DC g_m/I_D is lower, combining these effects give a transconductance efficiency that is greater than in weak inversion. Plotting the integral of each curve in Fig. 2 over the interval [0, F_{NQS}] versus IC where F_{NQS} is an onset frequency of NQS effect defined in (19) or (20), the maximum is found in SI (IC > 10) for L = 1 µm, while it is located in MI for L = 300 nm. This integral is a new FoM that we propose for the tradeoff between performance, power consumption, and speed.

$$FOM_{HF} = \int_0^{F_{NQS}} \frac{|y_{mi}|}{I_D} dF \tag{4}$$

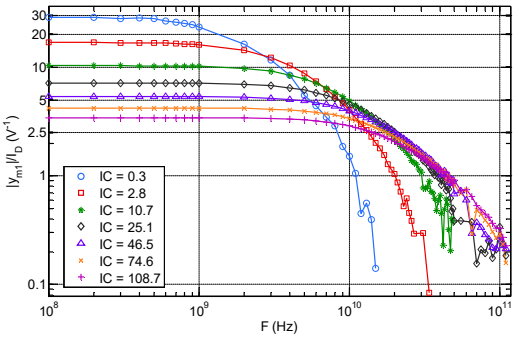

Fig. 2 Measured transadmittance efficiency modulus versus the frequency for different IC for a NMOS (L = 1 µm) in saturation (V_{DS} = 1 V) and back gate voltage V_{bG} = 0 V.

This FoM is more realistic than the previously defined $f_T.g_m/I_D$ in [13] since it does not assume that the transconductance vanishes beyond f_T and does not underestimate the performance in weak inversion. Indeed, as it will be discussed later, f_T is not the onset of NQS operation in weak inversion. The real high frequency capability is better captured by a NQS onset frequency F_{NQS} that will be defined in Section V. Moreover, in contradiction to the previously reported conclusions such as in [13], the optimum is now located in SI for long channels, and no longer in moderate inversion. For shorter devices, the optimum is still located in MI, as already reported using the $f_T.g_m/I_D$ FoM.

Fig. 3 shows the phase of the transadmittance efficiency versus frequency for various IC values. According to the approximation of the transadmittance efficiency expression in (9), in regard to the modulus, the phase is more sensitive to NQS effects and particularly in weak inversion. For instance, at lower frequency (F < 500 MHz) and for IC = 0.3, the phase delay is more than 31° while the modulus remains almost unaffected, i.e. 97 % of its DC value. Fig. 2 and Fig. 3 reveal that the effect of NQS transport on the transadmittance efficiency is gradual and depends on the channel inversion coefficient. Having a clear definition for the onset frequency of NQS operation is then needed to provide a more realistic insight into the high frequency performance of MOSFETs.

Exact small signal analytical expressions for NQS operation are presented in [10] for single gate MOSFETs and simplified in [11] to derive a compact model. The model reported in [11] proposed a frequency normalization scheme using the first pole obtained from the first order approximation of the NQS model of bulk MOSFETs. The critical frequency F_{crit} expression, which corresponds to the first pole of the frequency characteristic of the device, as a function of the inversion coefficient IC concept redefined in [3] for a double gate (DG) UTBB FDSOI MOSFET is:

$$F_{crit} = \frac{1}{2\pi}\frac{15}{4}\cdot\frac{\mu U_T}{L^2}\cdot\frac{2+6\,IC+3\sqrt{IC+\frac{1}{4}}+4\left(\sqrt{IC+\frac{1}{4}}\right)^3}{1+2\,IC+3\sqrt{IC+\frac{1}{4}}} \quad (5)$$

$$\approx \frac{15}{4\pi}\times\frac{\mu U_T}{L^2}\cdot\sqrt{IC}\ \text{(in SI)} \quad (6)$$

where μ and U_T are respectively the effective mobility and the thermal voltage. (6) is an approximation of (5) while neglecting smaller terms in strong inversion, with less than 1 % error on F_{crit} for IC > 2. The effective mobility is taking into account the impact of the vertical electrical field on scattering. The velocity saturation effect is found to be negligible. Indeed, according to [14], an anomalous frequency dependence of the gate-to-drain transadmittance y_{DG} in saturation is expected. This would manifest by an increase of y_{DG} with frequency, a trend which is not observed in our case.

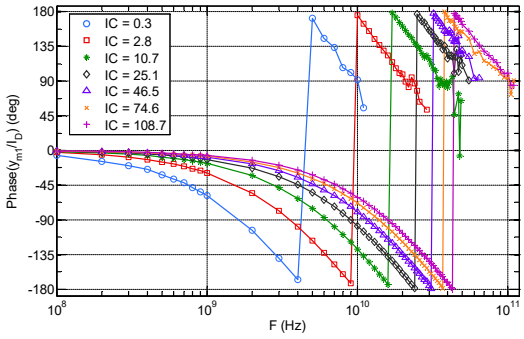

Fig. 3 Measured phase of the transadmittance over I_D versus frequency at different IC for NMOS (L = 1 μm) in saturation (V_{DS} = 1 V) and back gate voltage V_{bG} = 0 V.

It should be noted that F_{crit} is proportional to the effective mobility and U_T, inversely proportional to the square of gate length, and importantly, it accounts for the dependence of NQS on the inversion coefficient IC. This critical NQS frequency will be used for frequency normalization hereafter.

The transadmittance efficiency in saturation is derived from [11] as :

$$\frac{y_{m1}}{I_D} = \frac{g_{m1}}{I_D}\xi_m\left(\frac{F}{F_{crit}}, IC\right) \quad (7)$$

where g_{m1} is the low frequency front gate transconductance, I_D is the DC drain current, F is the operation frequency, F_{crit} is given by relation (5), and ξ_m is a NQS small-signal function based on the first kind Bessel functions. Defining a critical time delay as:

$$\tau_{crit} = \frac{1}{2\pi\cdot F_{crit}} \quad (8)$$

An approximation of (7) using the first pole of ξ_m becomes:

$$\frac{y_{m1}}{I_D} = \frac{g_{m1}}{I_D}\frac{1}{(1+j\omega\tau_{crit})} \quad (9)$$

where ω is the angular frequency (ω =2πF).

In Fig. 4, a normalized modulus of the transadmittance efficiency $(|y_{m1}|/I_D)_{norm}$ is shown for various values of IC versus the normalized frequency F_{norm1} defined as:

$$F_{norm1} = \frac{F}{F_{crit}} \quad (10)$$

In addition, a further normalization of $|y_{m1}|/I_D$ is applied using the low frequency transconductance efficiency g_{m1}/I_D as follows:

$$\left(\frac{|y_{m1}|}{I_D}\right)_{norm} = \left(\frac{|y_{m1}|}{I_D}\right)/(g_{m1}/I_D) \quad (11)$$

All normalized moduli plotted in Fig. 4 from weak to strong inversion are almost superposed as a result of the frequency normalization process in (10) (despite the very high frequency disturbance of the parasitic elements). The invariance is also evidenced for the phase in Fig. 5 up to a phase shift as large as 270°. It should be noted that a phase shift of 45° is reached at F_{norm1} = 1.

These results are of prime importance for modeling NQS effects in UTBB SOI FETs. For the first time, a simple but powerful analytical approach can predict the gate transconductance, modulus and phase, during highly non static operation of the intrinsic channel and in all the regions of

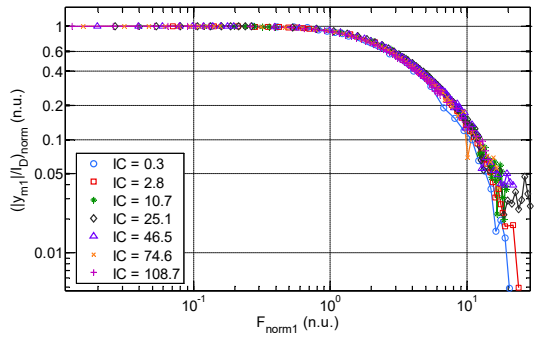

Fig. 4 Normalized transadmittance modulus over I_D versus normalized frequency F_{norm1} at different IC for NMOS (L = 1 µm & W = 1 µm) in saturation (V_{DS} = 1 V) and back gate voltage V_{bG} = 0 V (Measurements).

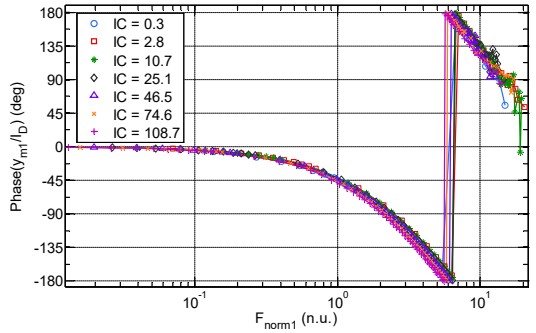

Fig. 5 Phase of the transadmittance over I_D versus normalized frequency F_{norm1} at different IC for NMOS (L = 1 µm & W = 1 µm) in saturation (V_{DS} = 1 V) and back gate voltage V_{bG} = 0 V (Measurements).

operation. Additional normalizations in terms of the inversion coefficient and critical frequency were used to derive a kind of abacus, paving the way to a simple and efficient HF design methodology where device parameters, biasing conditions and frequency are treated on the same ground.

IV. Impact of the Intrinsic Gate Dealy

In this Section, we investigate the breakdown of the normalized transadmittance efficiency invariance detailed in Section III. In particular, we will study the impact of the distributed effects along the gate on the critical frequency F_{crit} used for normalization.

A closer look at the normalized curves depicted in Fig. 5 reveals that in SI regime the transadmittance efficiency decreases earlier than in WI while the frequency increases. This enhanced phase shift in SI can be explained either by a decrease in the mobility or by an additional delay caused by the gate distributed effect. Note that in our previous normalizations (Fig. 4 and Fig. 5), the gate delay generated by the 1 µm finger length (i.e. gate width) was ignored.

At high frequency, the gate can be considered as a transmission line because of the limited electromagnetic wave velocity along the gate finger length. An estimation of the time constant of the distributed gate finger is given by [15]:

$$\tau_g = R_{gg} C_{gg} \tag{12}$$

where R_{gg} and C_{gg} are gate resistance and average gate capacitance respectively. It should be noted that C_{gg} depends on the level of inversion, which could explain the lower critical frequency in SI case when gate distributed effect is important. Conversely, in weak inversion C_{gg} is lower and a higher critical frequency is expected. According to [16][17], we have:

$$R_{gg} = \frac{R_g}{\eta} \tag{13}$$

where η is equal to 3 for a single-side connected gate and is equal to 12 for a double-side connected gate. R_g is the resistance of the MOSFET finger at low frequency (i.e. without the distributed effect) and extracted in SI. If we consider the additional pole due to the gate distributed effect, we can derive an equivalent global time constant as:

$$\tau_{dis} = \tau_{crit} + \tau_g \tag{14}$$

Considering that delays add, the delay caused by both gate finger length (i.e. the width of the transistor) and NQS are added using the semi-empirical formula (14). Consequently, the time constant in (14) includes distributed effects along the channel (i.e. NQS) and through the gate. Thus, the new critical frequency is:

$$F_{dis} = \frac{1}{2\pi \cdot \tau_{dis}} \tag{15}$$

Finally, neglecting higher order terms in the denominator and using the same approach, the transadmittance efficiency expression given in (9) becomes:

$$\frac{y_{m1}}{I_D} \approx \frac{g_{m1}}{I_D} \frac{1}{1 + j\omega \cdot \tau_{dis}} \tag{16}$$

A new normalized frequency considering non static transport in the channel and along the gate is now given by:

$$F_{norm2} = \frac{F}{F_{dis}} \tag{17}$$

For L = 1 µm, the error on the frequency predicting a 45° phase shift while using the normalization F_{norm2} (not shown here) is less than 15 % (5 % enhancement versus Fig. 5) since gate distributed effects are negligible in regard to NQS effect. According to (5), this residual discrepancy could be explained by a mobility varying with IC, which would be estimated at about 15 % between WI and SI for a long channel (i.e. L = 1 µm). Conversely, the error on the phase shift prediction for a given frequency is less than 6 %.

For L = 300 nm, the normalization using either F_{crit} or F_{dis} leads to similar conclusions as for the L = 1 µm case. Fig. 6 shows the phase shift for L = 300 nm MOSFET versus frequency. Based on the apparent critical frequency, the dominant distributed effect is the channel NQS. In Fig. 7, the frequency is normalized using F_{crit} to account for the channel NQS effect only. Clearly, the gate delay is evidenced since a higher inversion coefficient is responsible for 'earlier' phase shift. This cannot be attributed to the channel where higher IC moves the phase shift to higher frequencies. In Fig. 8, the second normalization is introduced using F_{dis} instead of F_{crit} to also account for the distributed gate delay. The normalization using F_{dis} is taking into account both delays: (1) the one caused by the distributed effect along the gate finger, and (2)

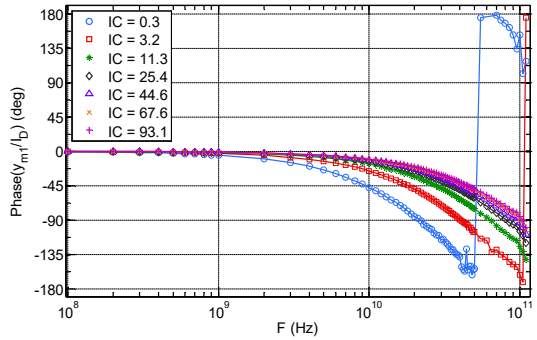

Fig. 6 Phase of the transadmittance over I_D versus frequency at different IC for NMOS (L = 300 nm & W = 1 µm) in saturation (V_{DS} = 1 V) and back gate voltage V_{bG} = 0 V (Measurements).

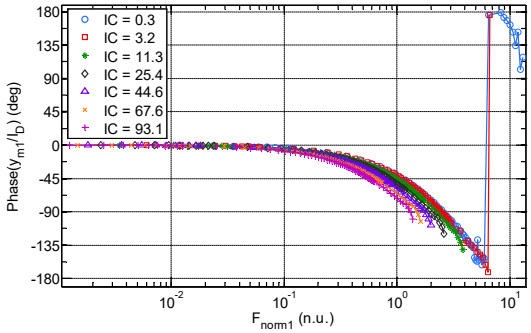

Fig. 7 Phase of the transadmittance over I_D versus normalized frequency F_{norm1} with constant mobility at different IC for NMOS (L = 300 nm & W = 1 µm) in saturation (V_{DS} = 1 V) and back gate voltage V_{bG} = 0 V (Measurements).

the other caused by the NQS effect along the channel. Therefore, F_{dis} is representing same critical frequency for each value of IC. Normalization using F_{dis} in Fig. 8 wipes out the differences generated by IC in the critical frequencies through both the gate delay and NQS, which finally results in merging all the curves in a single one. As a result, the discrepancy of the frequency for a 45° phase shift is reduced to less than 14 % as shown in Fig. 9, and the error on the predicted phase is less than 6 %. Again, the remaining mismatch could be explained by a variation of the mobility with the gate voltage. This point will be investigated in future work.

For shorter devices in RF circuits such as high gain amplifiers, the gate finger length is usually long (i.e. increased width for higher current drive or larger transconductance). In this case, the distributed effect along the gate finger adds an important delay that dominates the NQS effect in the shorter channel. This is evidenced on the phase delay versus the real frequency for the 28 nm channel length displayed in Fig 10. In the short device, the inversion level (IC) seems to have minimal impact on the critical frequency, see Fig. 10, and the two counter effects almost compensate each other. The gate distributed delay slightly take over since the phase shift happens earlier when IC is increased, which should not be if the channel would still be the bottleneck in terms of delay. To follow up with the normalization scheme, we calculate the 'intrinsic channel normalization frequency' F_{norm1} from relation (10) and plot the phase shift accordingly in Fig. 11. Whereas for 'long' channels, this first normalization almost

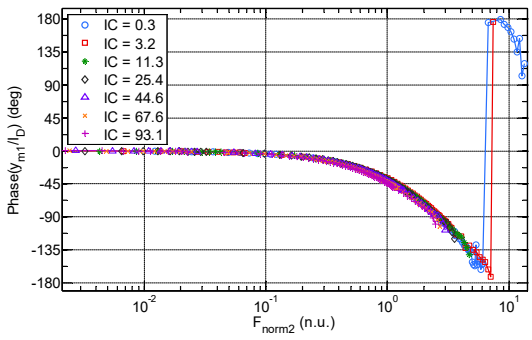

Fig. 8 Phase of the transadmittance over I_D versus normalized frequency F_{norm2} with constant mobility at different IC for NMOS (L = 300 nm & W = 1 µm) in saturation (V_{DS} = 1 V) and back gate voltage V_{bG} = 0 V (Measurements).

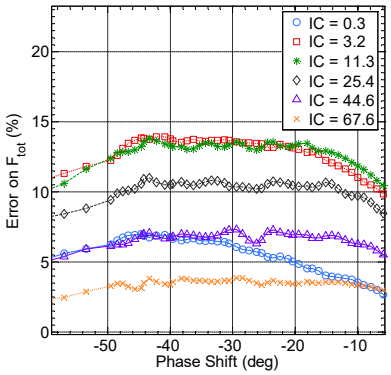

Fig. 9 Frequency error versus phase shift after normalization using F_{dis} (IC = 93.1 is taken as a reference)

condenses the bunch of curves in a single characteristics (see Fig. 5 and Fig. 7), here it spreads out. The gate distributed effect could explain this dispersion. Fig. 12 shows the phase shift for the 28 nm channel length device when using the normalization frequency F_{norm2} as given from (17) which now includes the first order non quasi static effect originating from the gate. The way the different characteristics are distributed in a narrow region is in favor of the predominance of the enhanced gate delay in short channel devices. Moreover, thanks to the mitigated channel NQS effect, the phase shift does not reach 45° within the frequency range from 100 MHz to 110 GHz for all levels of inversion.

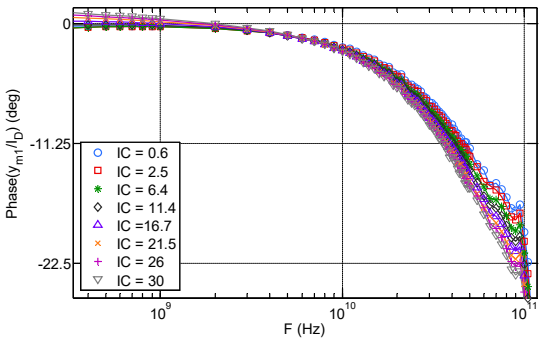

Fig. 10 Measured phase of the transadmittance over I_D versus frequency at different IC for NMOS (L = 28 nm & W = 1 µm) in saturation (V_{DS} = 1 V) and back gate voltage V_{bG} = 0 V.

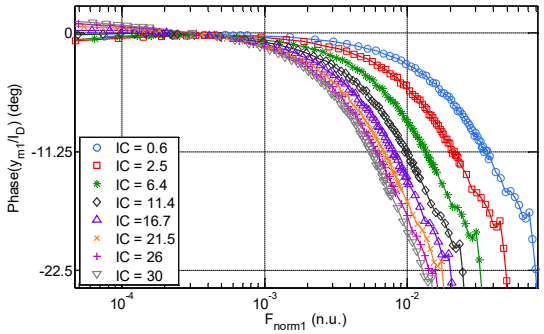

Fig. 11 Phase of the transadmittance over I_D versus the normalized frequency F_{norm1} estimated with a constant mobility at different IC for NMOS (L = 28 nm & W = 1 µm) in saturation (V_{DS} = 1 V) and V_{bG} = 0 V (Measurements).

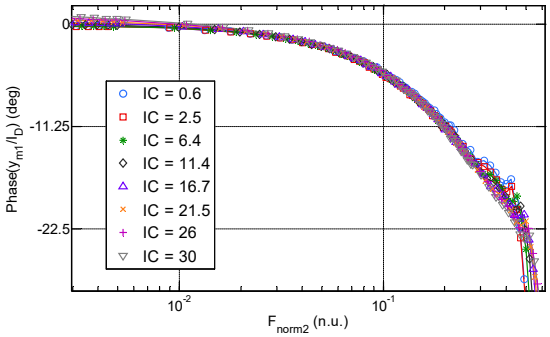

Fig. 12 Phase of the transadmittance over I_D versus normalized frequency F_{norm2} with constant mobility at different IC for NMOS (L = 28 nm & W = 1 µm) in saturation (V_{DS} = 1 V) and V_{bG} = 0 V (Measurements).

V. Onset of NQS effects

Significant NQS effects pop up when the operation frequency reaches the critical frequency F_{crit} defined in (5). In particular, a phase shift greater than 45° is measured at this characteristic frequency, meaning that F_{crit} overestimates the threshold of the NQS effect. To our knowledge, no clear definition is given for the emergence of NQS transport. Usually, the concept of transit frequency f_T is used, i.e. the frequency where the modulus of the current gain H_{DG} falls to unity (i.e. 0 dB), and the NQS frequency is often defined as being proportional to f_T [12]. However, this definition relies on the low frequency transconductance g_m, and therefore it is implicitly a quasi-static definition. Noting that the current gain H_{DG} is defined for a 2-port structure as:

$$H_{DG} = \frac{I_D}{I_G}\bigg|_{V_D=0} = \frac{y_{DG}}{y_{GG}} \tag{18}$$

where I_D and I_G are the current phasors across port-2 (drain) and port-1 (front gate), respectively. V_D is the voltage across port-2, which is impedance-matched in this case. In order to assess the relation between f_T and the NQS critical frequency, the current gain is plot for several IC values with respect to the normalized F_{norm1} frequency. Fig. 13 shows the modulus of the current gain H_{DG} as a function of the normalized frequency F_{norm1} for various IC and for a channel length of L = 1 µm. f_T is proportional to F_{crit} in MI and SI as can be expected from (6) and (2), and noting that f_T is proportional to the square root of the drain current provided velocity saturation is ignored.

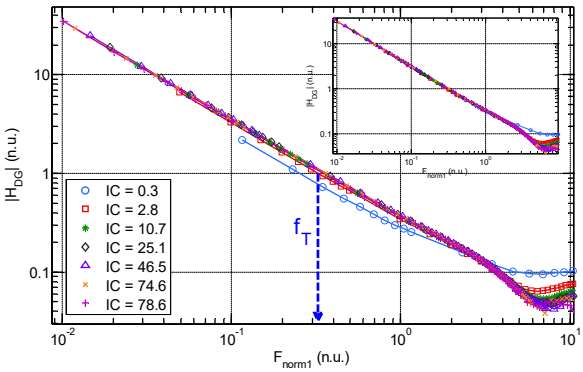

Fig. 13 Measured $|H_{DG}|$ versus normalized frequency F_{norm1} at different IC for NMOS (L = 1 µm & W = 1 µm), (V_{DS} = 1 V) and back gate voltage V_{bG} = 0 V. Inset shows $|H_{21}|$ versus F/F_{critSI} where F_{critSI} is given by (6).

However, for WI, the proportionality becomes less valid, as expected given that F_{crit} becomes constant in WI while f_T remains proportional to IC. If we use the SI approximation (6) for the frequency normalization for all the levels of inversion with L = 1 µm, all $|H_{DG}|$ plots are superimposed independently of IC as shown in inset of Fig. 13. This suggests that the transit frequency is equal to one third of the critical frequency in SI and that it remains proportional to the square root of the current all the way, from WI to SI.

Therefore, the proportionality between the onset of NQS frequency and f_T holds only in SI for long channels. In WI and practically in MI, this rules of thumb (proportionality to f_T) underestimates the critical NQS frequency. Depending on the criteria invoked, we propose to use two expressions for the onset of non-static transport:

- 10° phase shift of the transadmittance efficiency:

$$F_{NQS10°} = \frac{1}{2\pi}\frac{\tan\frac{\pi}{18}}{\frac{1}{2\pi \cdot F_{crit}} + \frac{R_g}{\eta}\cdot C_{gg}} \tag{19}$$

- 3% decrease in the transadmittance efficiency modulus from the low frequency value:

$$F_{NQS3\%} = \frac{1}{2\pi}\frac{0.25}{\frac{1}{2\pi \cdot F_{crit}} + \frac{R_g}{\eta}\cdot C_{gg}} \tag{20}$$

Note that $F_{NQS3\%}$ is practically equal to f_T in SI and, higher in WI and MI.

VI. Back gate control

In a DG UTBB MOSFET, the independent back gate voltage controls the threshold voltage and consequently IC. The back gate also influences the apparent mobility of the carriers in the silicon film thanks to the volume inversion in low electrical field condition. Therefore, as the NQS characteristic frequency F_{crit} depends on mobility and IC, the back gate should affect NQS effects. In this Section, the impact of the back gate voltage on $|y_{m2}|/I_D$ for a fixed front gate voltage is assessed using TCAD simulations. Note that due to lack of dedicated back gate RF structures, TCAD simulations are used to validate the invariant representation of transadmittances when the RF signal is applied to the back

gate. Using same normalization as in (17), we report that the different curves merge as in Fig. 4 and Fig. 5 for the front gate transadmittance efficiency $|y_{m1}|/I_D$ versus frequency while setting IC with the back gate voltage (not presented here). Interestingly, when the input signal is applied to the back gate, a back gate transadmittance efficiency $|y_{m2}|/I_D$ can also be defined.

In order to evaluate the back gate performance at high frequency, as in [3], the transadmittance efficiency of the back gate is now assessed for a fixed front gate voltage $V_{GS} = 0$, and for various inversion levels imposed by the back gate (various V_{bG}). Fig. 14 shows the phase of the transadmittance efficiency of the back gate at $V_{GS} = 0$ V. In this case, the channel is spread in the volume of the silicon film. Again, after applying the same normalization for the frequency and for the transadmittance to current ratio, a unique plot is obtained in Fig. 15. This supports that the normalization scheme used to predict non static transport in UTBB FDSOI MOSFETs is valid whatever gate is used.

VII. Discussion

The developments leading to the definition of a NQS critical frequency F_{crit} for a single gate bulk MOSFET developed in [10][11] hold for a DG MOSFET, including with asymmetric operation. In particular, the normalization of the frequency leads to almost unique charts for long channel devices allowing fast and accurate high frequency performance assessment. Moreover, the invariance is also confirmed for short channel devices with a dominant gate distributed effects provided that the related time constant is taken into consideration. The transadmittance efficiency concept defined in this paper provides a deep insight into high frequency UTBB FDSOI MOSFET behavior and gives an estimation of the limiting MOSFET characteristic frequencies. The critical channel NQS frequency depends on the device length, free carrier mobility and inversion coefficient IC. The gate distributed effect, in turn, depends on the gate resistance and capacitance.

The frequency normalization using the distributed gate time constant generalizes the normalization scheme by merging the longitudinal (gate) distributed effect with the channel NQS effect. The invariant normalized transadmittance efficiency versus normalized frequency was confirmed extensively with both measured and simulated data. This novel approach provides a way to calculate the critical frequency beyond

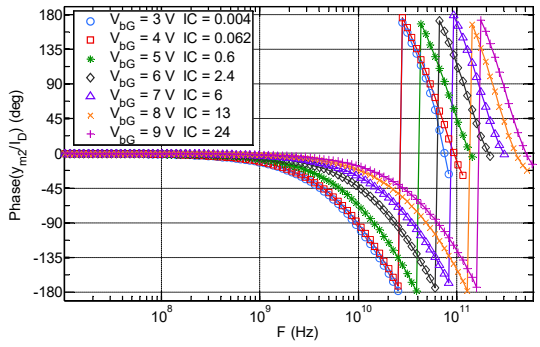

Fig. 14 Simulated phase of the back transadmittance efficiency versus frequency at different V_{bG} for NMOS (L = 1 µm) in saturation (V_{DS} = 1 V) and front gate voltage V_G = 0 V.

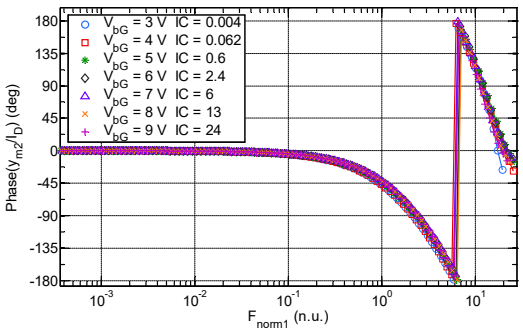

Fig. 15 Simulated phase of the back transadmittance efficiency versus normalized frequency F_{norm1} at different V_{bG} for NMOS (L = 1 µm) in saturation (V_{DS} = 1 V) and front gate voltage V_G = 0 V.

which the gain and the phase will be affected.

In Analog and RF design, oversimplified rules of thumb are commonly used, and bias the analysis. For instance, stating that operating frequency should be lower than $f_T/10$ or $f_T/3$ means that the designer will choose the shortest MOSFETs, which introduce detrimental mismatch and SCE, especially Drain Induced Barrier Lowering (DIBL). Such a rule of thumb can be overlooked using the transadmittance efficiency charts and critical frequency concepts developed in this paper based on the Inversion Coefficient exposed in [3] since knowing F_{crit} versus the channel length and DC operating point, the optimum geometry can be selected unambiguously.

VIII. Conclusion

In this work, we have shown that we can transpose the powerful normalizations derived for high frequency operation of bulk MOSFETs to the independent double gate FET in UTBB SOI technology. This ends up with very simple expressions for the phase and the magnitude for the front and back gate transadmittances versus frequency. In addition to the intrinsic channel delay, we have introduced the effect of the distributed gate thus taking into account lateral and longitudinal distributed effects in a single expression. This offers a practical insight to help high frequency performance assessments of UTBB FDSOI MOSFETs. Based on experimental results, we have shown that frequencies of interest where distributed effects occur can be predicted using the simple analytical expressions detailed in this work down to 28 nm channel length and up to 110 GHz. The normalization scheme is applicable to whatever the gates length and DC biasing, and supports the very general character of the NQS analysis proposed in this work.

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