



HAL
open science

Experimental gm/ID Invariance Assessment for Asymmetric Double-Gate FDSOI MOSFET

Salim El Ghouli, Denis Rideau, Frederic Monsieur, Patrick Scheer, Gilles Gouget, André Juge, Thierry Poiroux, Jean-Michel Sallese, Christophe Lallement

► **To cite this version:**

Salim El Ghouli, Denis Rideau, Frederic Monsieur, Patrick Scheer, Gilles Gouget, et al.. Experimental gm/ID Invariance Assessment for Asymmetric Double-Gate FDSOI MOSFET. IEEE Transactions on Electron Devices, 2018, 65 (1), 10.1109/TED.2017.2772804 . hal-03513623

HAL Id: hal-03513623

<https://hal.science/hal-03513623>

Submitted on 5 Jan 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Experimental g_m/I_D Invariance Assessment for Asymmetric Double Gate FDSOI MOSFET

Salim El Ghoul¹, Denis Rideau¹, Frederic Monsieur¹,
Patrick Scheer¹, Gilles Gouget¹, André Juge¹

¹STMicroelectronics, Crolles, France
salim.elghouli@st.com

Thierry Poiroux², Jean Michel Sallese³, Christophe
Lallement⁴

²CEA-Leti, Grenoble 38054, France

³EPFL, Lausanne 1015, Switzerland

⁴ICube-University of Strasbourg, Strasbourg 67412, France

Abstract—Transconductance efficiency (g_m/I_D) is an essential design synthesis tool for low-power analog and RF applications. In this paper, the invariance of g_m/I_D versus normalized drain current curve is analyzed in an asymmetric double gate fully depleted MOSFET. The paper studies the breakdown of this invariance versus back gate voltage, transistor length, temperature, drain to source voltage and process variations. The unforeseeable invariance is emphasized by measurements of a commercial 28 nm UTBB FDSOI CMOS technology, thus supporting the g_m/I_D based design methodologies usage in double gate FDSOI transistors sizing.

Keywords— Transconductance efficiency; Double-gate FETs; Fully Depleted Silicon-on-Insulator (FDSOI); UTBB; Analog and RF; Low-Power

I. INTRODUCTION

Double gate (DG) fully depleted MOSFETs exhibit a large inherent immunity to short channel effects, a steeper subthreshold slope and a higher drive current [1]. The independent double gate architecture is further enlarging circuit design space as the two gates can be independently controlled. These advanced structures are chosen to continue the aggressive CMOS technology down-scaling and demonstrate excellent digital and analog performances especially in low-power applications [2][3].

In recent low power and high performance circuits, it is crucial to operate MOSFET transistors all the way from weak to strong inversion levels [4]. Furthermore, moderate inversion region has been found to be a good compromise while power consumption and speed are valued equally [5][6][7]. To benefit from the full potential of recent technologies especially in deep weak and strong inversion, efficient analog first-cut designs still rely on hand calculations. The traditional hand calculations involve simplified MOSFET transistor models that are assumed to be valid in the weak and the strong inversion regimes.

Unfortunately, the usual strong and weak inversion approximations fail to predict drain current (I_D) in moderate inversion and there is no similar model that is simple enough for hand analysis and satisfactorily predictive in particular for multiple gate transistors [8][9]. The situation is becoming worse with advanced and down-scaled technologies where effective mobility, velocity saturation and series resistances are dominant at lower inversion levels. Consequently, the classical saturation

and strong inversion approximation square law is only valid near to the onset of strong inversion and inappropriate elsewhere. The transistors are therefore operated with less efficiency when traditional methods are used and this might lead to overdesign [10].

The above out-of-date hand calculations practices are preventing analog designers from taking full advantage of modern technologies (high transconductance efficiency and low V_{DSAT}). In order to address the weakness of the traditional procedures, where questionable concepts such as the early voltage, the gate voltage overdrive and the classical square law are used, the transconductance efficiency (g_m/I_D) based design methodology has been proposed [11]. The g_m over I_D approach relies on the fundamental and universal aspect of the transconductance efficiency versus normalized drain current curve in single gate MOSFETs. Such a plot is considered to be invariant regardless of threshold voltage and length considering short channel effects are negligible [11][12]. Should one be wary of taking the invariance assumption at face value while working with double gate MOSFETs?

The objective of this paper is to check the extent to which the g_m over I_D based design methodology referred to above is valid for advanced asymmetric double gate transistors such as the Fully Depleted SOI (FDSOI) Ultra-Thin Body and Box (UTBB) MOSFETs. The g_m over I_D design methodology is briefly explained in Section II. In Section III technology computer-aided design (TCAD) simulations provide first insight into the back gate effect on the front gate transconductance efficiency. The normalization of both transconductance efficiency and current for a double gate transistor is described in Section IV. In Section V the experimental setup is described and the transconductance efficiency versus the inversion coefficient (IC) chart invariance is assessed using obtained experimental data. Finally, discussion and conclusion are presented in Section VI and VII, respectively.

II. G_M OVER I_D BASED DESIGN METHODOLOGY

The concept of transconductance efficiency (g_m/I_D) was introduced by Pullen [13] and used in the context of the EKV MOST model [14][15]. The low-power design methodology using g_m over I_D versus normalized drain current was first demonstrated for an analog circuit design in [11]. The g_m over

I_D analog design procedures were promoted by Binkley and other researchers since then [10][16].

g_m/I_D is strongly related to analog circuits performances (e.g. common source amplifier gain is directly linked to g_m/I_D). It is also an indication of the device operating region as it is equal to the derivative $\partial \log(I_D)/\partial V_G$ which is constant in weak inversion and decreasing in moderate inversion (MI) and strong inversion (SI). Finally, g_m/I_D vs. normalized DC drain current curve is a tool for transistor dimensions calculation.

Using g_m over I_D based charts, the methodology allows accurate hand calculations in all MOSFET inversion levels including moderate inversion that is complex to model. The transistor geometry ratio (W/L) is determined once two values of the triplet (g_m/I_D , g_m , I_D) are calculated. I_D , g_m and Length are first chosen based on circuit design specifications (power consumption, higher gain or speed). In this first step, dedicated intrinsic gain and transit frequency versus normalized drain current charts with length as a parameter may be used as guides. Then g_m over I_D versus normalized drain current chart is used to determine the inversion level and calculate the required width. The g_m/I_D vs. gate voltage overdrive $V_G - V_T$ curve is used to confirm MOSFET is in saturation.

The optimum inversion coefficient determined using recently proposed figure of merit $g_m \cdot f_T / I_D$ can be used for an acceptable tradeoff between performance, power consumption, and speed [5][7]. The g_m over I_D methodology allows de facto the designer to consider level of inversion as an input rather than a consequence of the sizing.

III. INVARIANCE IMPREDICTABILITY USING TCAD

To assess the invariance of the transconductance efficiency versus normalized current chart, electrical $I_D - V_G$ and $C_{gg} - V_G$ characteristics have been first obtained using TCAD simulations based on constant mobility model. The simulated N-channel MOSFET device is an UTBB FDSOI MOSFET. Si body, BOX and equivalent gate oxide thicknesses are 7 nm, 25 nm and 1.3 nm, respectively. $I_D - V_G$ and $C_{gg} - V_G$ characteristics are simulated in saturation for various back gate voltages V_{bG} while source is grounded (all voltages in this paper are referred to the source). Fig. 1 shows the g_m/I_D as a function of the normalized drain current $I_D \cdot L/W$ with back gate voltage V_{bG} as a parameter (g_{m1} is the front gate transconductance, W and L are width and length of the device respectively) and a focus on MI and SI. As current increases for high forward back gate voltage ($V_{bG} = 5$ V), the back-channel inversion occurs first and results in a lower transconductance efficiency and lower subthreshold slope (i.e. higher "body effect"), corresponding to a lower equivalent front capacitance (front gate oxide capacitance in series with the silicon film capacitance). The transconductance efficiency for $V_{bG} = 5$ V tends towards the $V_{bG} = 0$ V curve at higher current (higher V_G) when the front channel inversion occurs. It should be noted that transconductance efficiency behavior at constant mobility is related to the C_{gg} capacitance (electrostatic) shown in Fig. 2. Indeed, $C_{gg} - V_G$ curve at high forward back gate voltage $V_{bG} = 5$ V reveals the two interfaces (back and front) activation corresponding to the two pronounced peaks of the C_{gg} derivative (inset in Fig. 2). The g_m/I_D versus normalized drain current curves for $V_{bG} = 5$ V and $V_{bG} = 0$ V do not superpose

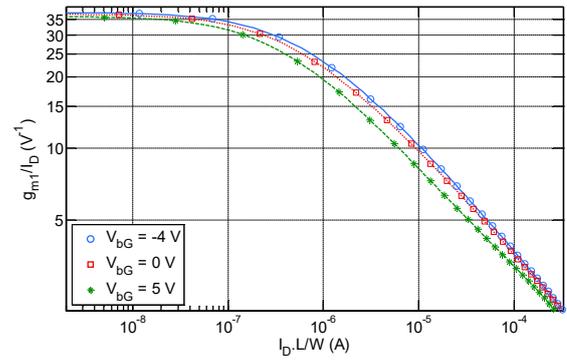


Fig. 1. g_{m1} over I_D versus normalized drain current ($I_D \cdot L/W$) of NMOS ($L = 1 \mu\text{m}$) in saturation at $V_{bG} = \{-4 \text{ V}, 0 \text{ V}, 5 \text{ V}\}$ and $T = 25^\circ\text{C}$.

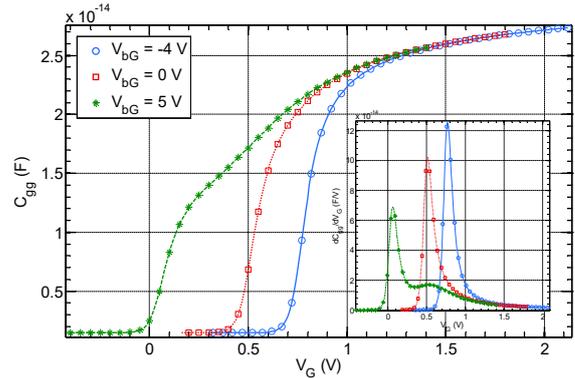


Fig. 2. C_{gg} versus front gate voltage V_G of NMOS ($L = 1 \mu\text{m}$) in saturation at $V_{bG} = \{-4 \text{ V}, 0 \text{ V}, 5 \text{ V}\}$ and $T = 25^\circ\text{C}$. Inset shows capacitance derivative $\partial C_{gg}/\partial V_G$.

(delta is greater than 15%) and hence TCAD simulations with constant mobility model do not unambiguously comfort/demonstrate the sought invariance for an asymmetric double gate MOSFET.

To gain further insight into the special behavior of the g_m/I_D for a UTBB MOSFET, experimental data will be used in Section V. The observed gradient mobility from front to back channel reported in [17][18] brings about additional ingredient to check out as g_m/I_D is linked to both electrostatic and transport according to:

$$\frac{g_m}{I_D} = \frac{\partial \ln I_D}{\partial V_G} = \frac{1}{Q_{inv}} \frac{\partial Q_{inv}}{\partial V_G} + \frac{1}{v} \frac{\partial v}{\partial V_G} \quad (1)$$

where Q_{inv} and v are the mobile charge density and mobile velocity respectively. Moreover, the invariance demonstrated using the model proposed in [19] for the case of a symmetric DG MOSFET calls for a generalization to the asymmetric DG MOSFET studied here.

IV. TRANSCONDUCTANCE EFFICIENCY AND CURRENT NORMALIZATIONS

In this work, the drain current is normalized to get an inversion coefficient (IC). The latter is defined as the square shape DC drain current I_D normalized by a technology current I_t comparable to the process dependent current defined in [16]:

$$IC = \frac{I_{\square}}{I_i} = \frac{I_D/(W/L)}{I_i} \quad (2)$$

where I_{\square} is the square shape drain current $I_D/(W/L)$, $i = 1$ for the front gate technology current and $i = 2$ for the back gate technology current. Indeed, two technology currents can be defined for an asymmetric double gate MOSFET. IC will be used as the x-axis of the normalized MOSFET transconductance efficiency plots presented in sections V, VI and VII. The inversion coefficient concept was introduced by Vittoz [14] and used in EKV model context [15]. In the transconductance efficiency versus normalized current I_{\square} chart, as depicted in Fig. 3, the technology current I_i is located at the intersection of the weak inversion asymptote (Boltzmann limit) and the saturation strong inversion square law asymptote for a long MOSFET [14]. Inversion coefficient concept is helpful to easily identify the MOSFET operating level of inversion.

An analytical expression for the technology current similar to the one given in [16] cannot straightforwardly be derived for a double gate MOSFET as mobility, subthreshold slope and gate capacitance vary significantly with front and back gate voltages. Indeed, as has been proposed in [20], the mobility is dependent on a coupling field, which in turn depends on front and back gate voltages. In the same model, the two ideality factors or namely front and back coupling factors n_1 and n_2 depend on the front or back channels activation. The explicit threshold based I_D model considers two inversion charges and a coupling charge associated to the coupling electrical field. An equivalent gate capacitance cannot be explicitly derived since two channels coexist. In [21] an equivalent gate capacitance is determined given the location of the effective conductive path, which in turn depends on front and back gate voltages. We propose to define an equivalent expression of the technology current which is related to both gates:

$$I_i = 2 \cdot \beta_i(V_G, V_{bG}) \cdot U_T^2 \quad (3)$$

where β_i ($i = 1$ or $i = 2$) are two functions of both front and back gate voltages. In saturation and in the case of front channel inversion with back channel in weak inversion the β_1 becomes equal to $n_1 \cdot C_{ox1} \cdot \mu_1$ provided that the front coupling factor n_1 in [20] is rather considered in strong inversion too. C_{ox1} and μ_1 are front oxide capacitance and front channel mobility respectively.

In asymmetric double gate transistors, two transconductance efficiencies can be defined according to the gate used for the input signal. Consequently, for a long channel, front and back transconductance efficiencies are normalized to their maximum values $1/(n_1 \cdot U_T)$ and $1/(n_2 \cdot U_T)$ respectively, which is reached in weak inversion. The analyzed figure of merit becomes: $FOM_i = n_i \cdot U_T \cdot g_{mi}/I_D$ where g_{mi} is front or back transconductance. Although g_m/I_D ratio reaches its maximum in deep weak inversion, the normalization factor (and consequently n_i value) is extracted at a higher level of current just before the onset of the moderate inversion. I_i is defined as the square shape current where the strong inversion asymptote and the weak inversion plateau intersect.

The normalization parameters for each gate I_i and n_i are taken to be intrinsic and unvarying constants for a MOSFET type. Consequently, the transconductance efficiency and I_D can

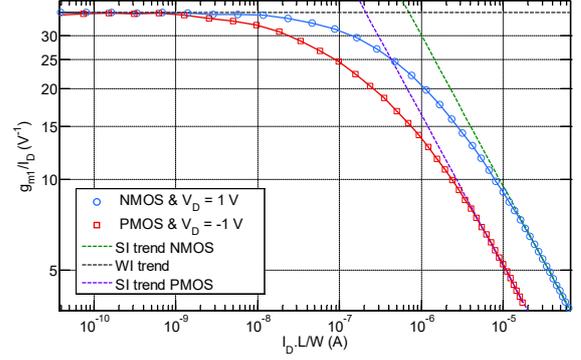


Fig. 3. Measured g_{m1} over I_D versus square shape drain current ($I_D/L/W$) of NMOS and PMOS ($L = 1 \mu\text{m}$) in saturation at $V_{bG}=0\text{V}$ and $T = 25^\circ\text{C}$.

simply be obtained from the normalized charts by multiplying the corresponding normalized quantities (values on y-axis and x-axis) by $1/(n_i \cdot U_T)$ and $I_i/(W/L)$ respectively.

V. EXPERIMENTAL RESULTS

This work was carried out using UTBB FDSOI MOSFETs implemented in a commercial 28 nm technology processed at STMicroelectronics. More details on the process can be found in [22]. The gate length and gate width of both measured N-channel and P-channel MOSFETs range from 28 nm to 4 μm and from 80 nm to 5 μm respectively. Drain current versus gate voltage I_D-V_G curves are measured at different drain voltages V_D (linear 50 mV to saturation 1 V), different back gate voltages V_{bG} (from -4V to 5V) and different temperatures (-40 $^\circ\text{C}$, 0 $^\circ\text{C}$, 25 $^\circ\text{C}$, 80 $^\circ\text{C}$ and 125 $^\circ\text{C}$).

As shown in Fig. 3, at a temperature of 25 $^\circ\text{C}$, the high subthreshold slope of the UTBB FDSOI transistors provides a maximum value of g_{m1}/I_D of about 36 V^{-1} for both NMOS and PMOS which corresponds to a near ideal subthreshold slope. The extracted n_1 and I_1 values for long NMOS and PMOS in saturation with grounded back gate are given in Table I. It should be noted that I_1 is not located in the center of the moderate inversion but rather in its upper part at one decade before the strong inversion region. The ratio of NMOS and PMOS technology currents compares to the ratio of electron and hole mobility. Both weak and strong inversion asymptotes overpredict transconductance efficiency at the technology current I_1 by more than 60%.

TABLE I. n_1 FACTOR AND I_1 FOR N-MOSFET AND P-MOSFET IN SATURATION AND AT 25 $^\circ\text{C}$

	n_1	I_1
NMOS	1.086	7.028e-7 A
PMOS	1.094	2.152e-7 A

Following the normalization explained in the previous section, Fig. 4 shows the normalized g_{m1} over I_D as a function of the inversion coefficient IC. NMOS and PMOS curves overlap in strong and weak inversion regions while a maximum of 7% difference is encountered in moderate inversion as charge carriers nature influences mobility behavior mostly in

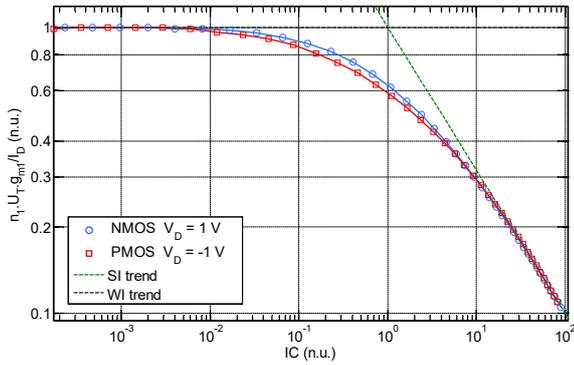


Fig. 4. Normalized transconductance efficiency versus IC of a NMOS and PMOS ($L = 1 \mu\text{m}$) in saturation at $V_{bG} = 0 \text{ V}$ and $T = 25 \text{ }^\circ\text{C}$.

this region. In the following sections, we will analyze the dependence of the normalized g_m/I_D versus inversion coefficient chart on transistor back or opposite gate voltage, temperature, geometry, drain to source voltage and process variability.

A. Back gate voltage impact

1) Front gate transconductance efficiency

It is not evident at first sight that the universal aspect of the g_m/I_D versus IC chart should be somehow conserved when setting the back gate voltage at different values, i.e. could it be that the so called g_m/I_D invariance will exhibit different shapes upon V_{bG} as observed in TCAD simulations in Section III. Fig. 5 shows normalized g_m over I_D vs. inversion coefficient curves experimentally obtained with $1 \mu\text{m}$ -long FDSOI UTBB N type MOSFET under different back gate voltage conditions.

For long channel MOSFETs, the normalized g_m over I_D behavior is within 6% from weak to strong inversion across the entire range of shown back gate voltage conditions (from -4 V to 5 V). Difference of non-zero back gate voltage cases versus the grounded back gate ($V_{bG} = 0 \text{ V}$) case are depicted in Fig. 6. Maximum transconductance efficiency is obtained for $V_{bG} = 2 \text{ V}$ in Fig. 6 corresponding to a weak transverse field, or in other words to a pronounced volume inversion shown in TCAD simulations in Fig. 7. This optimum condition takes place in the upper part of the moderate inversion region at $IC = 4$. Back gate voltage does not have great control on the volume inversion phenomena and consequently the front technology current does not vary too much. An error of less than 4 % is made in the prediction of the transconductance efficiency while assuming invariance over the wide back gate voltage range from -2 V to 2 V .

2) Back gate transconductance efficiency

In addition to the current modulation from the front gate, which is the most ‘regular’ approach, the back gate transconductance efficiency (g_{m2}/I_D) for different front gate V_G voltage conditions must also be analyzed since the IC concept should only depend on the current, independently how this current is generated, i.e. from the front or the back-gate voltage. This characteristic is shown in Fig. 8. In the case of front channel inversion with back channel in weak inversion (high front gate voltage), the extracted back gate slope factor is $n_2 = 12.6$ which agrees with the expression $n_1/(n_1-1)$ used in bulk technology

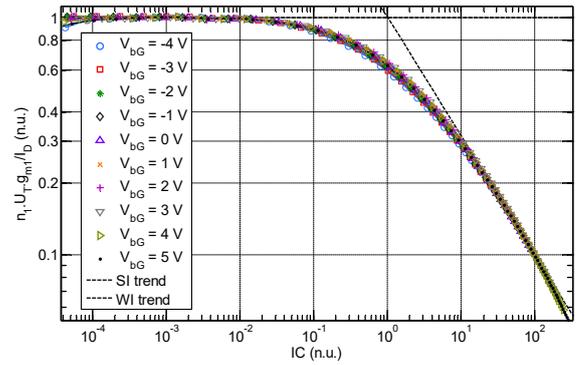


Fig. 5. Normalized g_{m1} over I_D as a function of the inversion coefficient at different V_{bG} for NMOS ($L=1 \mu\text{m}$ & $W=1 \mu\text{m}$) in saturation ($V_D = 1 \text{ V}$) at $T = 25 \text{ }^\circ\text{C}$.

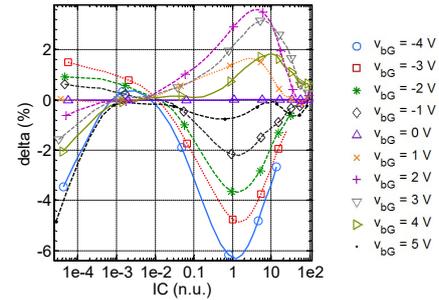


Fig. 6. Transconductance efficiency curves delta versus $V_{bG} = 0 \text{ V}$ curve.

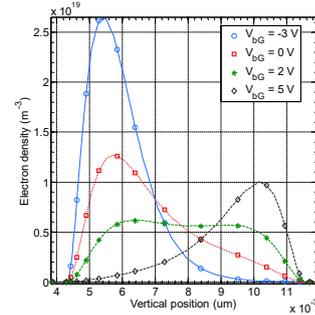


Fig. 7. Electron density in the silicon film at different V_{bG} for NMOS ($L = 1 \mu\text{m}$ & $W = 1 \mu\text{m}$) in saturation and strong inversion (at constant $V_G = 1 \text{ V}$).

except that depletion capacitance is replaced by box capacitance in series with silicon film capacitance. The extracted technology current I_2 corresponding to back channel activation (low front gate voltage) is approximately $0.35 \mu\text{A}$ which supports a rather comparable mobility between front and back channels according to:

$$\frac{\mu_2}{\mu_1} = \frac{C_{ox1} + C_{si}}{C_{ox2} + C_{si}} \cdot \frac{I_2}{I_1} \approx 2 \cdot \frac{I_2}{I_1} = 1 \quad (4)$$

where C_{si} , C_{ox2} and μ_2 are silicon film capacitance, back oxide or box capacitance and back channel mobility respectively. Unlike the front transconductance efficiency case, the front gate voltage has a considerable impact on the volume inversion and consequently on the back technology current I_2 . The technology current I_2 varies between $0.3 \mu\text{A}$ and $1.3 \mu\text{A}$ while front gate

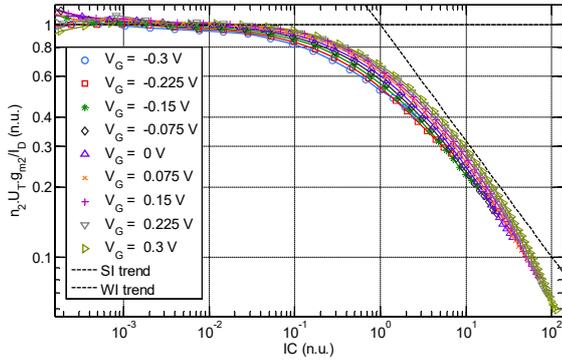


Fig. 8. Normalized g_{m2} over I_D as a function of the inversion coefficient at different V_G for NMOS ($L = 1 \mu\text{m}$) in saturation ($V_D = 1\text{V}$) at $T = 25^\circ\text{C}$.

voltage V_G is varied from -0.3V to 0.6V . Considering an invariant chart of the back transconductance efficiency g_{m2}/I_D vs. IC generates a less than 20 % error in weak and moderate inversion.

Front gate and back gate transconductance efficiency curves support that transconductance efficiency is maximized when charge carriers are not confined near the two interfaces but rather occupy the silicon film volume with a weaker transversal electrical field. This optimistic condition is obtained for certain combinations of front and back gate voltages (V_G, V_{bG}). In order to sustain this convenient state, front and back gates are swept simultaneously with a fixed voltage offset. This configuration can more easily be realized in design rather than sweeping the gates with a multiplication factor. Fig. 9 shows experimental transconductance efficiency curves where an ideal subthreshold slope is achieved for all offset values.

B. Temperature impact

The normalized g_{m1} over I_D characteristics measured at different temperatures for transistor length of 300 nm are shown in Fig. 10 and compared in the inset. In the comparison plots, most pessimistic case with regard to transconductance efficiency (i.e. $T = 125^\circ\text{C}$) is taken as a reference. Normalization is using the unique I_1 and n_1 parameters extracted at 25°C (Table I). Thermal voltage U_T considers the measurements temperature. Less than 0.06 % error per degree Celsius is expected when considering g_{m1} over I_D versus IC characteristic invariance overall inversion levels. Maximum delta is obtained in the second half of the moderate inversion where charge carriers sensitivity is higher. It can be seen from Fig. 10 that transistor length of 300 nm slightly departs from strong inversion square law trend for high IC values (deep strong inversion). Such behavior is not significant for longer devices. The short channel impact will be assessed in the following section.

C. Short channels

As shown in the previous plots for long transistors, transconductance efficiency is constant and maximum in weak inversion, decreases rather slowly in moderate inversion, and decreases as the inverse square-root of IC in strong inversion.

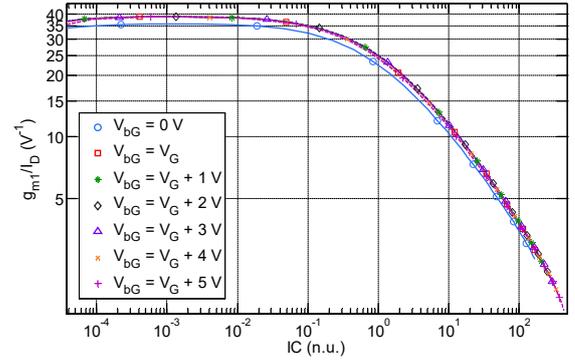


Fig. 9. Measured g_{m1} over I_D as a function of IC for fixed V_{bG} and simultaneous front and back gates sweep with an offset for NMOS ($L = 1 \mu\text{m}$) in saturation ($V_D = 1\text{V}$) at $T = 25^\circ\text{C}$.

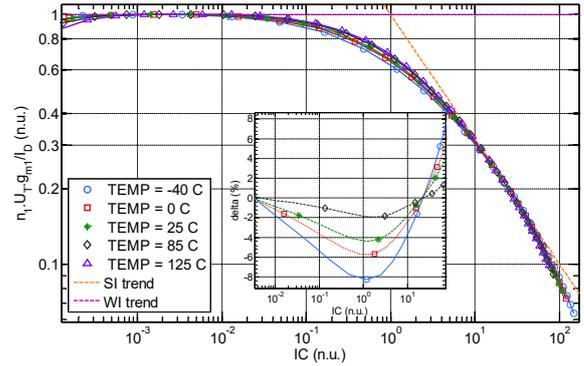


Fig. 10. $n_1.U_T.g_{m1}/I_D$ as a function of the inversion coefficient at different temperatures for NMOS ($L = 300\text{nm}$ & $W = 1 \mu\text{m}$) in saturation ($V_D = 1\text{V}$) and $V_{bG} = 0\text{V}$; inset shows delta versus $T = 125^\circ\text{C}$ case.

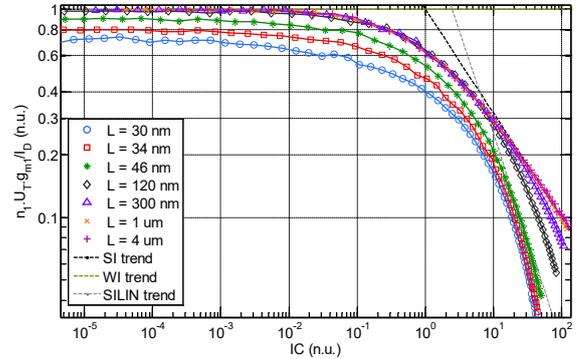


Fig. 11. Normalized g_{m1} over I_D as a function of the inversion coefficient for different lengths for NMOS ($W = 1 \mu\text{m}$) in saturation ($V_D = 1\text{V}$) at $T = 25^\circ\text{C}$.

At the onset of strong inversion, transconductance efficiency is 70 % lower than its maximum value. Fig. 11 shows normalized transconductance efficiency as a function of IC for different transistor lengths. Short channel transistors depart from the strong inversion asymptotic behavior because of mobility reduction, velocity saturation effects and series resistance. Transconductance efficiency curves overlay in weak and moderate inversion for the 120 nm to 4 μm range of channel lengths. For lengths below 120 nm, short channel effects lower subthreshold slope and enhance degradation (roll-off) of transconductance efficiency in strong inversion.

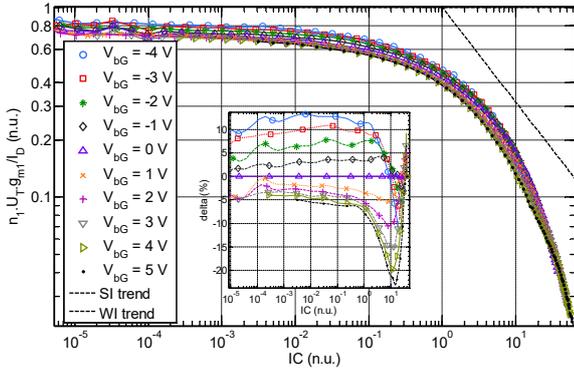


Fig. 12. Normalized g_{m1} over I_D as a function of the inversion coefficient at different V_{bg} for NMOS ($L=30$ nm & $W=1$ μ m) in saturation ($V_D=1$ V) at $T=25$ $^{\circ}$ C.

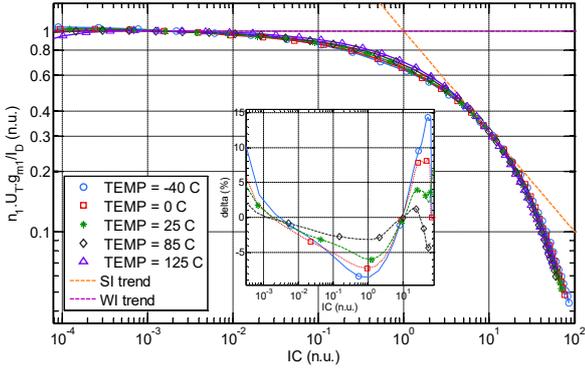


Fig. 13. $n_1 \cdot U_T \cdot g_{m1} / I_D$ as a function of the inversion coefficient at different temperatures for NMOS ($L=30$ nm & $W=1$ μ m) in saturation ($V_D=1$ V) and $V_{bg}=0$ V; inset shows delta versus $T=125$ $^{\circ}$ C case.

Strong inversion degradation ceases when carrier's velocity saturates completely and a $\sim 1/IC$ dependence is obtained. An additional degradation with respect to the linear asymptote ($\sim 1/IC$) occurs when series resistance and mobility degradation add to velocity saturation for short channel transistors.

The long transistor unique chart can be used in weak and moderate inversion to predict transconductance efficiency for all transistors with a length greater than 120 nm while error is kept lower than 5 %.

To assess back gate voltage effect for a short channel MOSFET, the normalized g_{m1} over I_D is shown in Fig. 12 for $L=30$ nm. The transconductance efficiency in weak inversion varies within 20 % across the entire range of back gate voltage conditions (from -4 V to 5 V). This spread is due to the short channel effects and the relative sensitivity of the subthreshold slope to back gate voltage. In Fig. 13, transconductance efficiency versus IC chart is measured for different temperatures. For short channel MOSFET, the chart varies with a low rate (less than 0.1 % per degree Celsius).

D. Drain to source voltage

The concept of g_{m1}/I_D invariance should only be used in saturation regime and it is worth assessing the limit of drain potential below which the invariant breaks down in the onset of strong inversion.

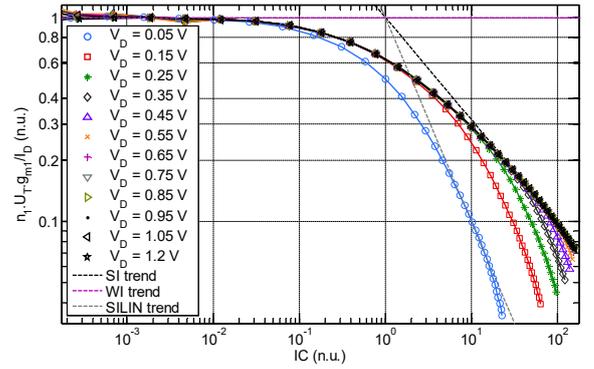


Fig. 14. Normalized g_{m1} over I_D as a function of the inversion coefficient for different V_D for NMOS ($W=1$ μ m and $L=1$ μ m) at $T=25$ $^{\circ}$ C.

This information is useful in modern low-voltage low-power design since high transconductance efficiency is obtained in moderate inversion with lower drain to source saturation voltage V_{DSAT} .

Fig. 14 shows normalized transconductance efficiency versus IC for different drain to source voltages. In linear regime, the g_{m1}/I_D curve departs from the saturation and strong inversion asymptotic behavior and follows the $1/IC$ asymptote instead (also shown in Fig. 14).

The transconductance efficiency chart defined at $V_D=1$ V can be used for lower drain to source voltages down to $V_D=250$ mV in weak and moderate inversion (with an error of less than 4%).

E. Sensitivity to manufacturing process variations

To check how sensitive transconductance efficiency versus inversion coefficient chart is to manufacturing process variations, foundry process based UTSOI model [23], has been used to plot three normalized transconductance efficiency characteristics versus IC. The characteristics correspond to the typical (TT), fast (FF) and slow (SS) corners. As shown in Fig. 15, the three corners charts practically overlay and a maximum error of 4.5 % is obtained in deep strong inversion and less than 1.6 % error is made across the range of weak and moderate inversion (inset in Fig. 15).

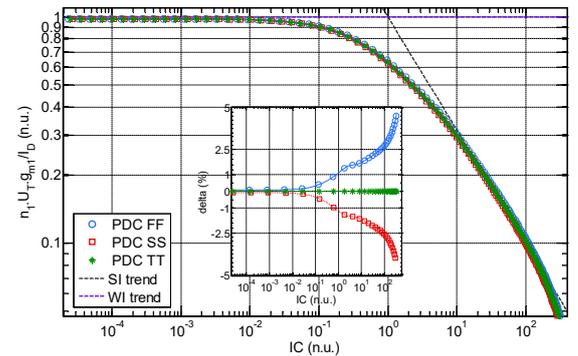


Fig. 15. NMOS transconductance efficiency as a function of the inversion coefficient for different process corners ($L=1$ μ m & $W=1$ μ m) in saturation ($V_D=1$ V) and $V_{bg}=0$ V; inset shows delta versus typical corner case.

VI. DISCUSSION

The transconductance efficiency clearly benefits from volume inversion apparent mobility comprehended as enhanced back channel mobility in [17][18]. The optimum transconductance efficiency for a double gate MOSFET is obtained thanks to an enhanced mobility at low transverse field corresponding to a pronounced volume inversion. This is characterized by a higher carrier density in the center of the silicon film and a weak transverse electrical field. In this case, both effective mobility and gate capacitance are high and the corresponding technology current is boosted. For a back gate voltage of 2 V, a maximum transconductance efficiency is obtained at $IC = 4$ in Fig. 6 where $f_{T, gm}/I_D$ figure of merit found to be optimal [5][23]. On the one hand, enhanced volume mobility helps to regain transconductance efficiency when back channel is inverted first (high V_{bG}) with lower front capacitance. On the other hand, the high capacitance, when only front channel inversion occurs, helps to partially recover the effect of degraded mobility on transconductance efficiency (low V_{bG}). Consequently, g_m/I_D vs. IC charts for different back gate voltages (from $V_{bG} = -2$ V to 2 V) can be approximated using a universal chart with an acceptable error of 4%. The back gate voltage degree of freedom offered in asymmetric double gate transistors does not prevent design using g_m/I_D vs. IC chart especially in moderate inversion.

The transconductance efficiency versus IC chart determined using a typical long channel MOSFET at 25 °C shows negligible sensitivity to temperature and process variations. The chart is invariant and rather insensitive to drain to source voltage as long as the transistor is in saturation. The minimum channel length for the chart invariance assumption is $L = 120$ nm. For NMOS, velocity saturation effects become significant in moderate inversion for $L < 100$ nm and chart cannot be used. However, a short channel chart might be considered as back gate voltage and temperature still have a relatively low impact at shorter MOSFETs. For PMOS, less subject to velocity saturation effects, shorter transistors can be sized using a unique PMOS chart.

VII. CONCLUSION

In this work, the universal aspect of the relationship between the transconductance efficiency (g_m/I_D) and the inversion coefficient (IC) has been investigated. We have shown that a unique chart can be exploited for the asymmetric double gate FDSOI transistors of the same type (N or P) with negligible errors in moderate inversion, thus of great interest for low-voltage and low-power applications. Sensitivity has been assessed in terms of back gate voltage, temperature, process corners, drain to source voltage and length.

We have experimentally shown that g_m over I_D versus inversion coefficient chart can be considered as a fundamental characteristic of UTBB FDSOI technology transistors and thus be used in g_m over I_D based analog design sizing procedures.

REFERENCES

[1] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: A

new device with greatly enhanced performance," *IEEE Electron Device Letters*, vol. 8, no. 9, pp. 410–412, Sep. 1987.

[2] J. Hartmann, "FD-SOI Technology Development and Key Devices Characteristics for Fast, Power Efficient, Low Voltage SoCs," in *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, La Jolla, CA, 2014, pp. 1–4.

[3] J.-P. Raskin, "FinFET versus UTBB SOI - a RF perspective," in *Solid State Device Research Conference (ESSDERC)*, 2015 45th European, 2015, pp. 84–88.

[4] D. M. Binkley, "Tradeoffs and Optimization in Analog CMOS Design," in *14th International Conference on Mixed Design of Integrated Circuits and Systems, 2007. MIXDES '07*, 2007, pp. 47–60.

[5] A. Mangla, C. C. Enz, and J. -M. Sallese, "Figure-of-merit for optimizing the current-efficiency of low-power RF circuits," in *Mixed Design of Integrated Circuits and Systems (MIXDES)*, 2011 Proceedings of the 18th International Conference, 2011, pp. 85–89.

[6] V. Kilchytska, M. K. Md Arshad, S. Makovejev, S. Olsen, F. Andrieu, T. Poiroux, O. Faynot, J.-P. Raskin, and D. Flandre, "Ultra-thin body and thin-BOX SOI CMOS technology analog figures of merit," *Solid-State Electronics*, vol. 70, pp. 50–58, Apr. 2012.

[7] S. El Ghoul, P. Scheer, T. Poiroux, A. Juge, J. -M. Sallese and C. Lallement, "Dynamic behavior of the UTBB FDSOI MOSFET", presented at MOS-AK Workshop, Grenoble, France, Mar. 12, 2015.

[8] Y. Taur, X. Liang, W. Wang, and H. Lu, "A continuous, analytic drain current model for DG MOSFETs", *IEEE Electron Device Letters*, vol. 25, no. 2, pp. 107–109, Feb. 2004.

[9] A. S. Roy, J. -M. Sallese, and C. C. Enz, "A closed-form charge-based expression for drain current in symmetric and asymmetric double gate MOSFET," *Solid-State Electronics*, vol. 50, no. 4, pp. 687–693, Apr. 2006.

[10] D. Foty, D. Binkley, and M. Bucher, "Starting over: g_m/I_D -based MOSFET modeling as a basis for modernized analog design methodologies," in *Proceedings of the Technical International Conference on Modeling and Simulation of Microsystems (Nanotech '02)*, 2002, pp. 682–685.

[11] F. Silveira, D. Flandre, and P. G. A. Jespers, "A g_m/I_D based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, 1996.

[12] M. Bucher, C. Lallement, C. C. Enz, F. Theodoloz, and F. Krummenacher, "Scalable G_m/I_D based MOSFET model," in *Proc. Int. Semiconductor Device Research Symp.*, Charlottesville, VA, 1997, pp. 615–618.

[13] K. A. Pullen, "Transconductance efficiency," *Proc. of the IEEE*, vol. 64, no. 9, pp. 1442–1443, Sep. 1976.

[14] E. A. Vittoz, "Micropower techniques", in *J. Franca and Y. Tsvividis (Eds), Design of analog-digital VLSI circuits for telecommunications and signal processing*, Prentice-Hall, Englewood Cliffs, NJ, 1994, Ch. 3, pp. 53–96.

[15] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integr Circ Sig Process*, vol. 8, no. 1, pp. 83–114, Jul. 1995.

[16] D. Binkley, M. Bucher, and D. Foty, "Design-oriented characterization of CMOS over the continuum of inversion level and channel length," *Proc. of the 7th IEEE ICECS*, vol. 1, pp. 161–164, Dec. 2000.

[17] A. Ohata, S. Cristoloveanu, and M. Cassé, "Mobility comparison between front and back channels in ultrathin silicon-on-insulator metal-oxide-semiconductor field-effect transistors by the front-gate split capacitance-voltage method," *Appl. Phys. Lett.*, vol. 89, no. 3, p. 032104, Jul. 2006.

[18] T. Rudenko, V. Kilchytska, S. Burignat, J. -P. Raskin, F. Andrieu, O. Faynot, Y. Le Tiec, K. Landry, A. Nazarov, V. S. Lysenko, and D. Flandre, "Experimental study of transconductance and mobility behaviors in ultra-thin SOI MOSFETs with standard and thin buried oxides," *Solid-State Electronics*, vol. 54, no. 2, pp. 164–170, Feb. 2010.

[19] J. -M. Sallese, F. Krummenacher, F. Prégaldiny, C. Lallement, A. Roy, and C. C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism," *Solid-State Electronics*, vol. 49, no. 3, pp. 485–489, Mar. 2005.

- [20] M. Reyboz, P. Martin, T. Poiroux, and O. Rozeau, "Continuous model for independent double gate MOSFET," *Solid-State Electronics*, vol. 53, no. 5, pp. 504–513, May 2009.
- [21] T. A. Karatsori, A. Tsormpatzoglou, C. G. Theodorou, E. G. Ioannidis, S. Haendler, N. Planes, G. Ghibaud, and C. A. Dimitriadis, "Analytical Compact Model for Lightly Doped Nanoscale Ultrathin-Body and Box SOI MOSFETs With Back-Gate Control," *IEEE Transactions on Electron Devices*, vol. 62, no. 10, pp. 3117–3124, Oct. 2015.
- [22] N. Planes, O. Weber, V. Barral, S. Haendler, D. Noblet, D. Croain, M. Bocat, P. -O. Sassoulas, X. Federspiel, A. Cros, A. Bajolet, E. Richard, B. Dumont, P. Perreau, D. Petit, D. Golanski, C. Fenouillet-Béranger, N. Guillot, M. Rafik, V. Huard, S. Puget, X. Montagner, M. -A. Jaud, O. Rozeau, O. Saxod, F. Wacquant, F. Monsieur, D. Barge, L. Pinzelli, M. Mellier, F. Boeuf, F. Arnaud, and M. Haond, "28nm FDSOI technology platform for high-speed low-voltage digital applications," in *2012 Symposium on VLSI Technology (VLSIT)*, Honolulu, HI, 2012, pp. 133–134.
- [23] S. El Ghouli, P. Scheer, M. Minondo, A. Juge, T. Poiroux, J. -M. Sallese, and C. Lallement, "Analog and RF modeling of FDSOI UTBB MOSFET using Leti-UTSOI model," in *MIXDES*, Lodz, Poland, 2016, pp. 41–46.



Salim EL GHOULI received the engineering degree from ENSPS and the M.S. degree in Microelectronics from Strasbourg University, France, in 2004. He joined STMicroelectronics device modeling team, Crolles, France, in 2004. From 2004 to 2010 he respectively was involved in modeling activities of two International Alliances (Crolles2 Alliance, France and ISDA, Fishkill, NY, USA). He is now working in STMicroelectronics advanced device modeling and in parallel toward the Ph.D.



André Juge received the PhD degree from Université Scientifique et Médicale de Grenoble. Starting 1988, he held positions as Modeling Engineer and Team leader in STMicroelectronics R&D, to support development of BICMOS and CMOS technologies. In 2002, he became Modeling manager for Crolles2 Alliance, France. Since 2007, his activities are devoted to Advanced modeling

solutions through cooperative projects with Academia, Compact Model Council (CMC), and EDA tool suppliers.

Patrick Scheer received the engineering degree in electronics from the ENSERG, and the M.S. degree in optics, optoelectronics and microwaves from the INPG, Grenoble, France, in 1993. He received the Ph.D. degree in optics and optoelectronics from the ENSAE, Toulouse, France, in 1998. He joined STMicroelectronics in Crolles, France, in 1998 to develop models for RF CMOS technologies. He is now working on modeling solutions for analog & RF designs.



Thierry Poiroux received the M.S. degree from Ecole Centrale Paris, France, in 1995 and the Ph.D. degree from the University of Nantes, France, in 2000. In April 2000, he joined CEA-Leti and, since 2012, he is working on the development of the second version of Leti-UTSOI compact model, dedicated to fully-depleted SOI technology. He has authored or coauthored five book chapters and more than 160 papers and communications.



Jean-Michel Sallese received the Ph.D in physics from the University of Nice-Sophia Antipolis. He joined the Ecole Polytechnique Fédérale de Lausanne and was appointed Maître d'Enseignement et de Recherche. His current research concerns modeling of emerging electron devices and high energy radiation effects in integrated circuits and sensors.



Christophe Lallement received the Ph.D. in engineering from Télécom ParisTech, in 1993. From 1994 to 1997, he was a Postdoctoral Researcher in Swiss Federal Institute of Technology, Lausanne, in the EKV model team. He joined the University of Strasbourg, France, in 1997. Since 2003, he is Professor in Télécom Physique Strasbourg. As a team leader in ICube, Strasbourg, his current research focuses on the modeling of advanced devices, mixed-signal systems, and biosystems.