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Imane Malass, Wilfried Uhring, Jean-Pierre Le Normand, Norbert Dumas, Foudil Dadouche. Evaluation of size influence on performance figures of a Single Photon Avalanche Diode fabricated in a 180 nm standard CMOS technology. Analog Integrated Circuits and Signal Processing, 2016, NEWCAS 2014-2015, 89 (1), pp.69 - 76. 10.1007/s10470-016-0763-8 . hal-03513621

HAL Id: hal-03513621

<https://hal.science/hal-03513621>

Submitted on 14 Apr 2023

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I. INTRODUCTION

Single Photon Avalanche Detectors or SPAD are PN junctions biased in Geiger Mode i.e. beyond their breakdown voltage, as a result the electric field in the multiplication region is so intense that a single photon carrier, ideally due to photon generation, is enough to start a self-maintained avalanche by impact ionization, thus generating a high current pulse signaling the detection of a photon to the associated electronic circuitry. SPADs are capable of detecting individual photon arrivals with tens of picoseconds time of arrival resolution [1], they offer many advantages in comparison to the traditional photomultiplier tubes (PMT) as they allow low noise and low jitter photon detection without requiring high reverse bias voltage and are more cost-effective, less bulky and compatible with standard CMOS technology. In the last 10 years many works have been done to optimize the SPAD technology and numerous SPADs have been implemented in both dedicated and standard CMOS technologies [2], and while SPADs manufactured using dedicated technologies have been able to reach great performances in term of noise and detection efficiency, SPADs fabricated in standard CMOS technologies allows the highest level of miniaturization and integration with lower power consumption and a reduced overall cost [3] making them very appealing to integrate in single photon applications such as Fluorescence Life Time Imaging (FLIM) [4] [5] Positron Emission Tomography (PET) [6] and Time of Flight (TOF) measurements [7]. In this paper we present a SPAD structure fabricated in a standard 0.18 μm CMOS technology with the characterization results of its main performance parameters; the remaining of this paper is thus structured as follows: in section II we represent the implemented SPAD structure, in section III we describe the characterization setup, the characterization results are shown in section and we conclude in section IV.

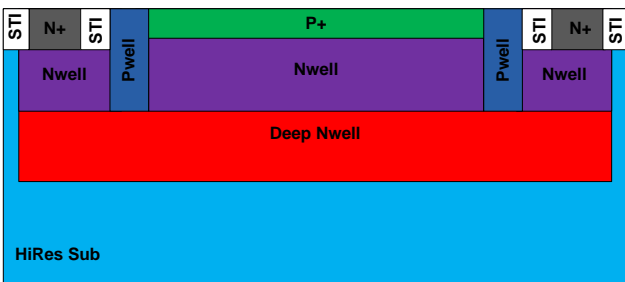


Fig. 1 - Cross section of the presented SPAD structure

II. SPAD DESIGN

A high quality SPAD should offer a low dark noise and a high Photon Detection Probability (PDP). This requires a structure design that allows a uniform high electric field in the multiplication region and limits the premature edge breakdown effect [8]. The proposed SPAD cross section is illustrated in Fig.1, the active area is a P+/Nwell junction in a retrograded Deep Nwell on a high resistivity P-substrate. To avoid premature edge breakdown a double Pwell/STI guard ring was implemented. The low doped Pwell guard ring was added to separate the multiplication region from the STI implant to reduce high dark noise due to faulty detections triggered by carrier injections from the STI interface into the multiplication Area.

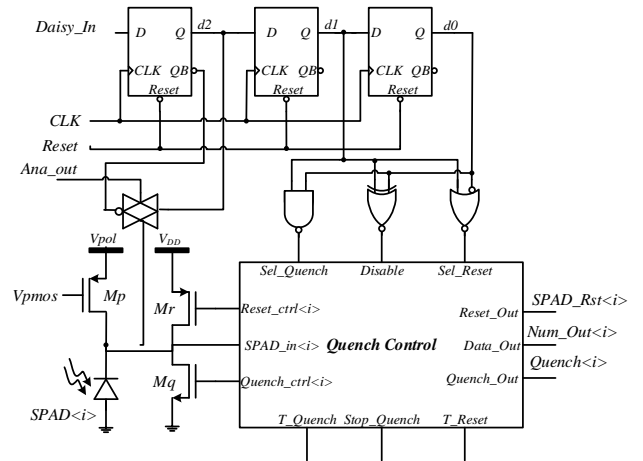


Fig.2 – Versatile pixel architecture for SPAD characterization

III. PHYSICAL IMPLEMENTATION AND CHARACTERISATION SETUP

Eight devices with the presented SPAD structure were implemented using a 180 nm standard CMOS image sensor technology, the devices have 8 different active area diameters ranging from 5 μm to 40 μm . The eight sensors were implemented in an integrated circuit that uses the approach, described in [9], that allows a quick prototyping and characterization of SPAD structures implemented in any CMOS process. The large and versatile array makes it possible to test a large number of different structures in a single chip thus limiting the number of iteration to find the best SPAD. Each SPAD was integrated with its quenching circuit in a characterization pixel (Fig.2) and can be individually activated and characterized without any interference of the other devices. The quenching circuit (Fig.2) includes a voltage controlled PMOS transistor for passive quenching, a NMOS transistor (Mq) for active quenching and a PMOS transistor (Mr) for active reset. The quenching and reset transistors are switched on and off by the quench control block [9] which also allows to set the quenching mode (passive, active, mixed) and the durations of the quenching phase and the reset phase. Due to the use of the additional Pwell guard ring that imposes restrictions on the minimum active area diameter [10], the 5 μm diameter SPAD was not functional but the remaining 7 devices showed an abrupt avalanche around a measured reverse bias of 11.4 V (Fig.3).

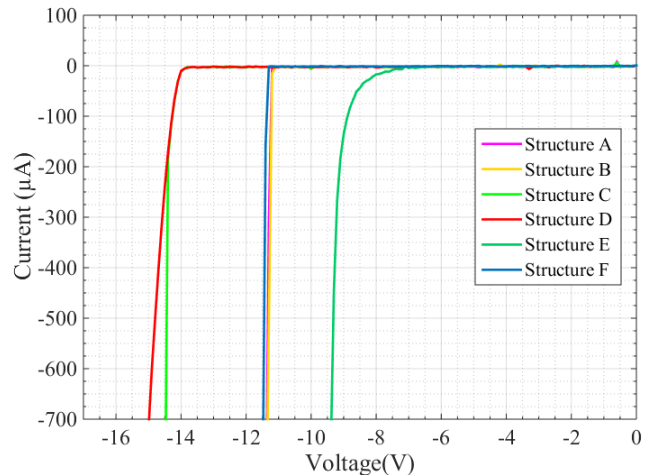


Fig.3 - I-V Characteristics of the 7 SPAD devices

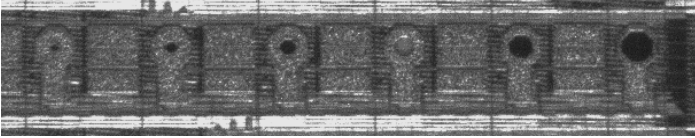


Fig.4 – Electroluminescence light emission test performed over the 25 μm SPAD (third device from the right) at a reverse excess bias of 300 mV

Furthermore the electroluminescence emission test performed on these devices showed a uniform avalanche process over all the surface of the active region. Fig.4 shows the electroluminescence light emission of the 25 μm SPAD at a reverse excess bias of 300 mV. The other visible devices with diameters of 10, 15, 20, 30 and 40 μm are switched off.

IV. CHARACTERISATION RESULTS

A. Dark Count Rate

Dark Count Rate (DCR) represents the measure in the dark of spurious avalanche events which are not the result of a photon interaction. The DCR is triggered by several generation mechanisms: thermal generation, trap assisted generation and band to band tunneling; it is strongly dependent on the SPAD design as well as the used CMOS technology process. Primary DCR is random and statistically uncorrelated but SPADs also display secondary avalanche pulses statistically correlated to primary events known as afterpulsing. Afterpulsing is due to trapping and de-trapping of charges flowing through the multiplication region during the primary avalanches, it is dependent of the current amplitude, the associated electronics as well as temperature and can be reduced by increasing the SPAD hold-time to allow the releasing of the trapped charges before activating the SPAD again. The probability of the afterpulsing for the 7 SPAD implementations was measured at room temperature for an excess bias of 300mV with a dead time of 30 ns which is the minimum achievable dead time by the associated quenching circuit. Fig.5 shows the afterpulsing probability measurement results using the inter-arrival time histogram method [11] for the 20 μm SPAD with an excess bias of 300mV. The afterpulsing probability of the 7 SPAD devices are illustrated as a function of their active area diameter in Fig.6, the measured probability was around $\sim 0.21\%$ at 300mV for the 7 devices, indicating that the afterpulsing probability is not related to the surface of the device. Furthermore the inter-arrival time histograms obtained from the measurements by calculating time durations between 2 consecutive avalanche events showed that the undesirable afterpulsing can be eliminated by increasing the dead time to 1 μs .

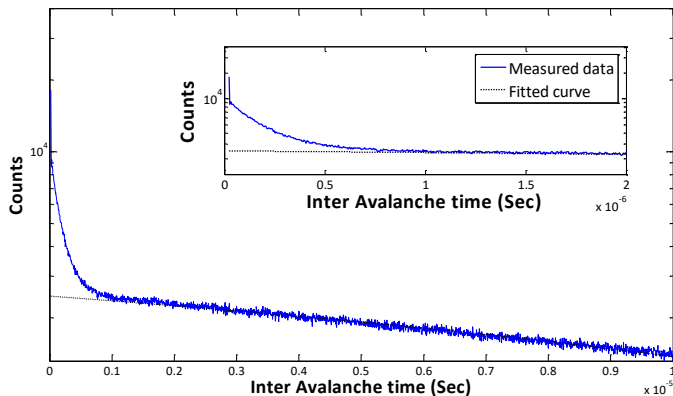


Fig. 5 – Afterpulsing measurement results for a dead time of 30 ns and an excess bias of 300 mV

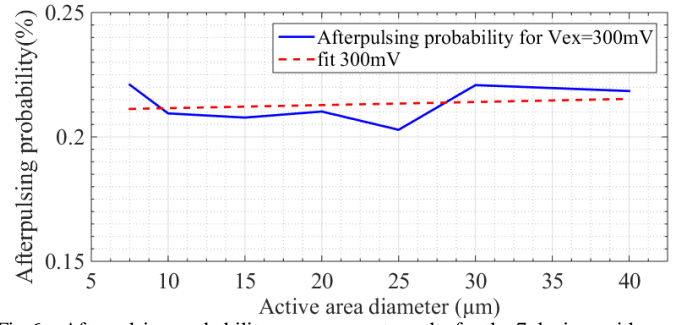


Fig.6 – Afterpulsing probability measurement results for the 7 devices with an excess bias of 300 mV

The total DCR was measured for the 7 devices at different excess bias values and with a temperature ranging from -30°C to 60°C . The DCR variation against temperature for an excess bias of 100 mV and 400 mV is represented in Fig.7 which shows that the measured DCR increases with the SPAD active area, at 15°C it is lower than 5 kHz for SPADs with an active region diameter below 30 μm and lower than 10 kHz for the 30 μm and 40 μm SPADs. Raising the excess bias from 100 mV to 400 mV increases the DCR value with a mean factor of 2.2 over the whole range of considered temperatures for all the SPAD diameter variations, which proves that the effect of the excess bias on the DCR do not depend of the device area.

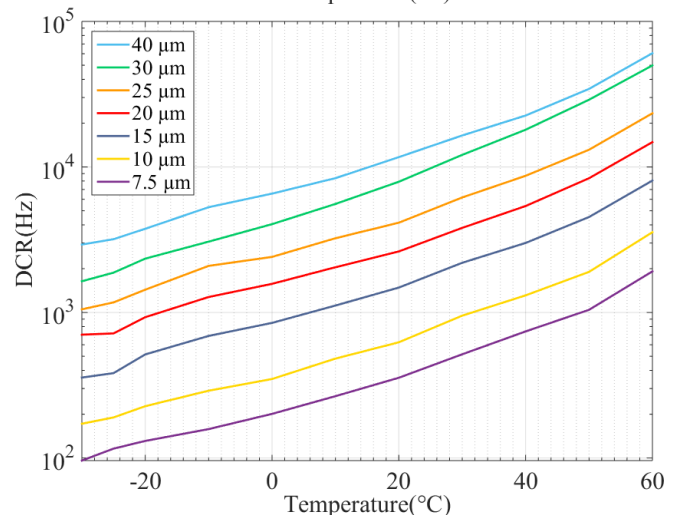
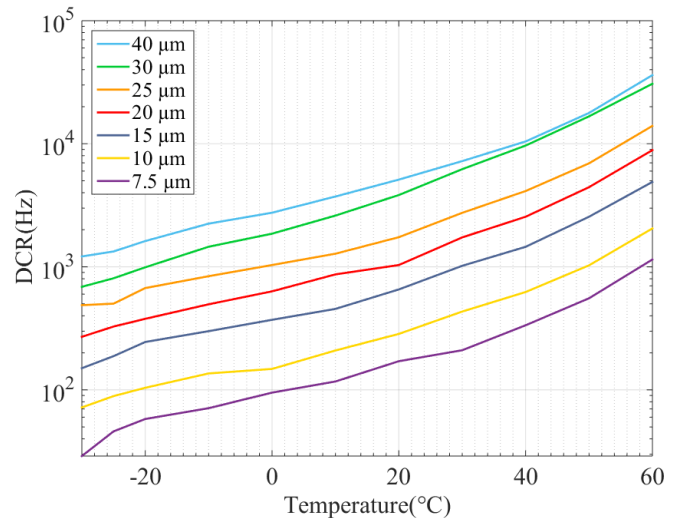


Fig.7 - DCR of the 7 devices versus temperature at an excess bias of 100 mV (top) and 400 mV (bottom)

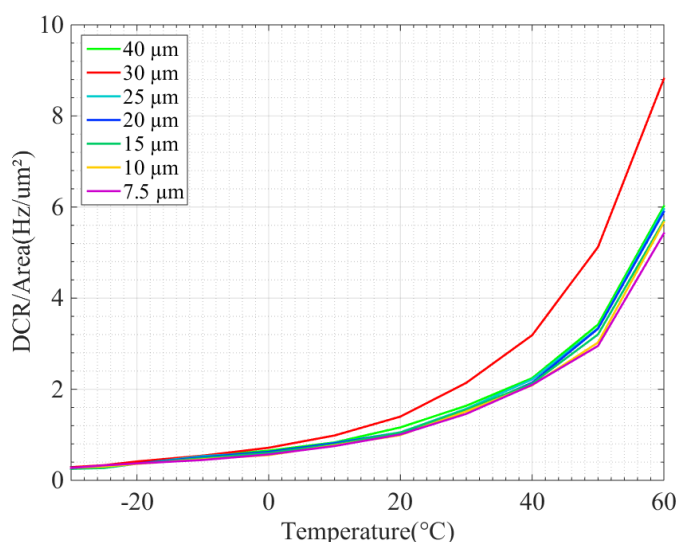


Fig.8 - The DCR /Area variation against temperature for the 7 devices at an excess bias of 400 mV

To better illustrate the effect of SPAD diameter on the measured DCR, the ratio DCR/Surface variation against temperature for the 7 devices at an excess bias of 400 mV is plotted in Fig.8. The SPADs showed the same DCR/Area value with the exception of the 30 μm SPAD that generated more noise/ μm^2 most likely due to a higher defects concentration compared to the rest of the SPADs. The results also show a linear variation below 20 $^{\circ}\text{C}$ with the DCR doubling every 10 $^{\circ}\text{C}$ thus suggesting that it is mostly dominated by the tunneling mechanism. Above 20 $^{\circ}\text{C}$ the DCR increases exponentially and the thermal generation becomes the dominating mechanism.

B. Photodetection probability

Photon Detection Probability (PDP) represents the ratio of the number of detected photons over the number of incident photons; it represents the sensitivity of the SPAD to incident photons. PDP is the result of the absorption probability and the triggering probability [2] [12], it depends of doping levels [13], noise, excess bias [2] and the area of the active region.

We measured the PDP of the 7 devices over a wavelength range between 350 nm and 1000 nm at room temperature for various excess biases between 100 mV and 400 mV and a dead time of 30 ns. Fig.9 shows the PDP of the 7 devices with an excess bias of 300mV. The measurements showed that the PDP peaks around 430 nm for the 7 devices, the maximum PDP value for a given active area increases with the excess bias (Fig.10) and the maximum PDP value for a given excess bias value increases with the active area although the amount of PDP enhancement tends to decrease as the active area diameter increases and it becomes very minor for active area diameters higher than 20 μm (Fig.9). The measured peak PDP is equal to 11% for the 7.5 μm SPAD and 19% for the 40 μm SPAD. This probably results from a smaller active area really formed during the CMOS process for the SPAD below 20 μm . The difference of the PDP for the 7.5, 10 and 15 μm can be explained by a real diameter reduced by 1.35, 1.15 and 0.9 μm respectively. In general, the measured PDP values are quite good giving the relatively low excess bias which was due to limitations imposed by the associated quenching electronics

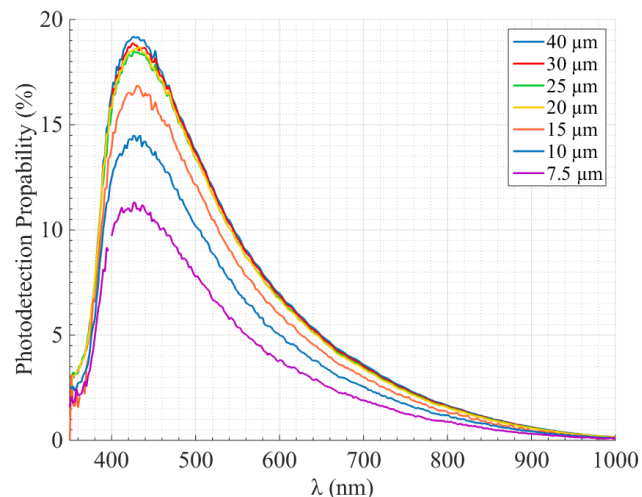


Fig.9 - Photodetection probability of the 7 SPADs for an excess bias of 300 mV

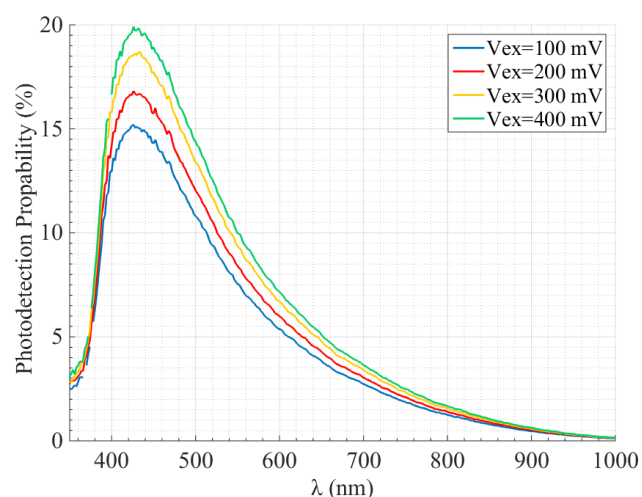


Fig.10 – Photodetection probability of the 20 μm SPAD for various excess bias values

C. Timing Jitter

Timing jitter represents the timing incertitude due to statistical variation of delays between photon absorption and the subsequent avalanche detection by the SPAD's associated electronics. It decreases with bias voltage and increases with the active area [14]. The timing jitter values of the 7 devices were characterized using a TCSPC setup with a 20 MHz picoseconds laser diode source [15] with an excess bias ranging between 200 mV and 500 mV, and a dead time of 30 ns. The timing response of the 7 SPADs are shown in Fig.11 for 2 wavelength values $\lambda=450$ nm and $\lambda=808$ nm at an excess bias of 300 mV. The pulse widths (*Pulsewidth*) of the light emission have been measured with the streak camera described in [16] to 67 ps FWHM and 99 ps FWHM for the 450 and the 808 nm laser diode respectively. The distributions show a sharp Gaussian peak and an exponential tail. The sharp Gaussian peak is due to photons absorbed in the multiplication area while the tail is due to minority charge carriers diffusion and photons absorbed below the multiplication region and is more marked for higher wavelengths [3]. In general, the timing response FWHM for a giving excess bias increases with the active area diameter due to lateral and vertical dependence of timing uncertainty on photon absorption location thus better timing resolutions are obtained with the smaller SPADs for the 2 laser source wavelength values.

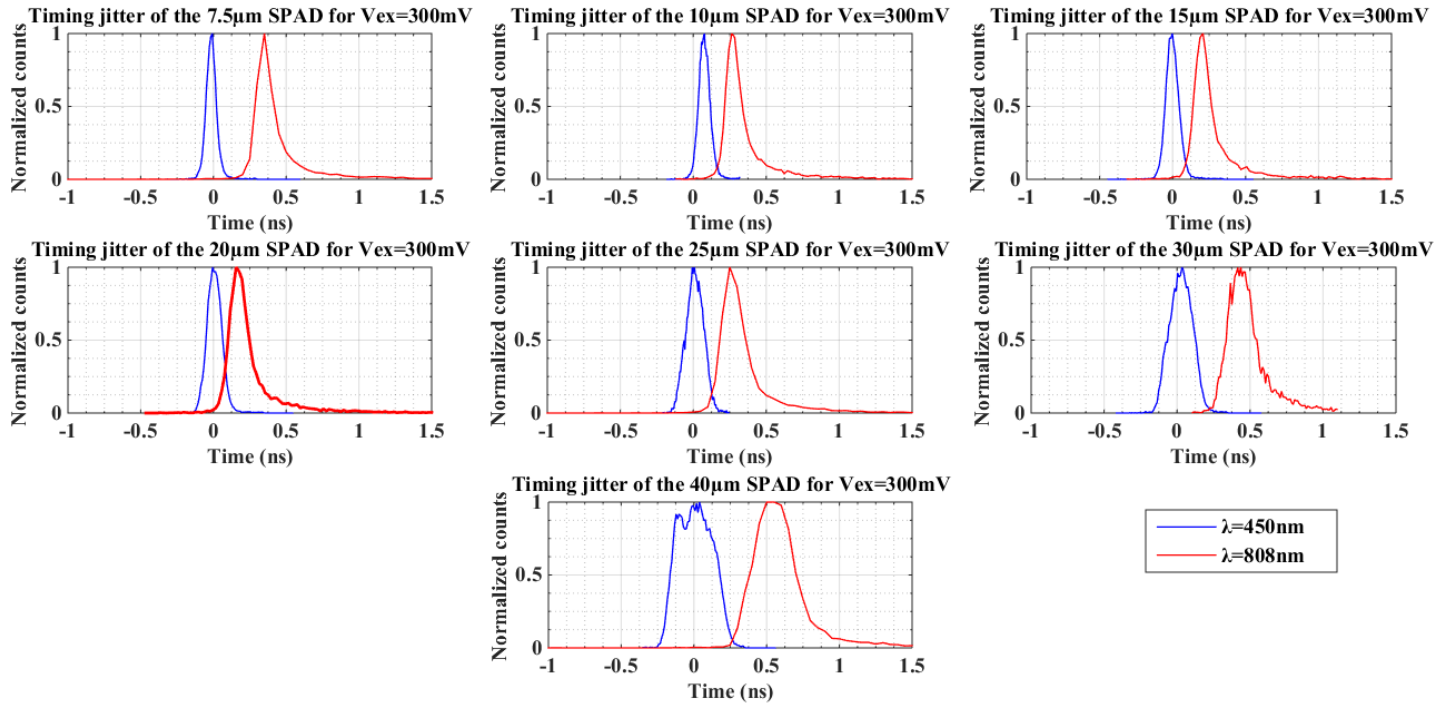


Fig.11 - Normalized timing response measurement results using a 450 nm and a 808 nm laser with an excess bias of 300mV for the 7 SPAD diameters

Furthermore the 450 nm laser yields better timing resolutions due to the fact that photons with higher wavelength can go deeper into the neutral region thus requiring more time before reaching the multiplication region and triggering the avalanche process. This is better illustrated in Fig.12 which shows the raw measured jitter ($Jitter_{Measured}$) values (solid line) of the 7 SPADs for the 2 wavelength values and for an excess bias of 300 mV. The effect of the optical pulse width have been decorrelated to the measured jitter to obtain a value closer ($Jitter_{Real}$) (dotted line) to the real device performances according to the equation

$$Jitter_{real} = \sqrt{(Jitter_{Measured})^2 - (Pulse_{width})^2} \quad (1)$$

At 300 mV the best measured timing resolution is equal to 34 ps and was achieved using the SPAD with an active area of 7.5 μm for $\lambda=450$ nm. The maximum jitter for $\lambda=450$ nm is obtained using the 40 μm SPAD and it is equal to 300 ps. Similarly for $\lambda=808$ nm, the minimum measured jitter is equal to 67 ps and the maximum jitter is equal to 350 ps and was measured using the 40 μm SPAD. Fig.13 shows the timing jitter variation of the 7.5 μm to 25 μm SPADs as a function of the excess bias for $\lambda = 405$ nm. Unsurprisingly the timing jitter At 300 mV the best measured timing resolution is equal to 34 ps and was achieved using the SPAD with an active area of 7.5 μm for $\lambda=450$ nm. The maximum jitter decreases as the excess bias increases, as it leads to an increase of the electric field strength in the multiplication region thus reducing the time needed for a photodetection to generate a reverse current high enough to be detected by the SPAD's associated electronics. For $\lambda=450$ nm (Fig.13), the measured timing jitter of 7.5 μm device is around 100 ps at 200 mV and decreases to 65 ps at an excess bias of 500 mV. Similarly the measured jitter for the 25 μm is 166 ps at an excess bias of 200 mV and decreases to \sim 130 ps at an excess bias of 500 mV.

V. CONCLUSION

In this paper we presented and characterized 7 implementations of a SPAD structure fabricated in a 180 nm Standard CMOS image sensor technology with active area diameters between 7.5 μm and 40 μm . Despite a limited excess bias value, the reported SPAD compares relatively well with several reported SPADs fabricated in standard CMOS process (c.f. TABLE I). The measurements showed a DCR below 5 kHz at 15 $^{\circ}\text{C}$ with a highly suspected strong band to band tunneling and field-enhanced generation effects due to the relatively low breakdown voltage (11.4 V). The afterpulsing probability of the device was characterized using the inter-arrival time histogram method and the measurements yielded a probability of 0.2% for a hold time of 30 ns. The PDP measurements showed a peak at 20% around 430 nm and the measured timing resolution was less than 100 ps FWHM for $\lambda=450$ nm at an excess bias of 500 mV.

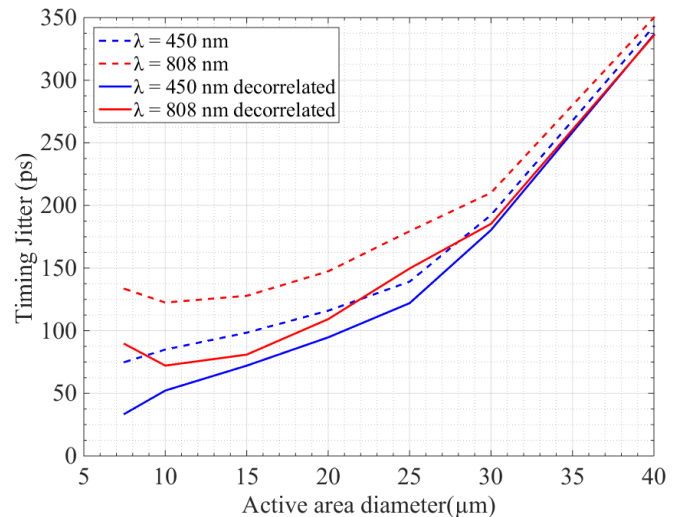


Fig.12 – Timing jitter results for $\lambda = 450$ nm and $\lambda = 808$ nm at an excess bias of 300 mV

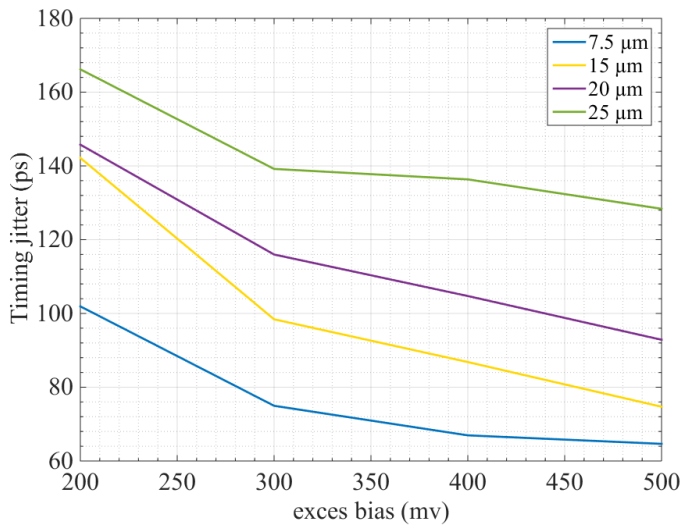


Fig.13 - Timing jitter variation of the 7.5 μm to 25 μm SPADs as a function of the excess bias for $\lambda = 405 \text{ nm}$.

SPADs characterization is known to be a very delicate process as their performances is sensitive to many variables (excess bias, temperature, size, etc.) and the importance of the active area value was very obvious in the results of our measurements as it affected all the SPAD parameters except for the afterpulsing probability. The DCR was proportional to the devices area, the jitter was improved when the diameter is reduced whereas the PDP decreased for SPAD diameter below 20 μm .

In our case, the tradeoff between all the SPAD performance parameters yields the conclusion that the best compromise was obtained with SPADs that have an active area diameter between 15 μm and 25 μm as they showed a reasonable DCR (less than 5 kHz), a good PDP probability ($\sim 18\%$) and a timing jitter lower than 100 ps.

TABLE I. PERFORMANCES FIGURES OF SEVERAL SPADs FABRICATED IN STANDARD TECHNOLOGIES

	Performance figures			
	DCR	Afterpulsing	PDP	Jitter
This work	<10 kHz	0.2%	20%	100 ps
(5)	1 kHz			
(10)	100 kHz		5.5%	
(14)	<43 Hz		40%	77 ps 120 ps
(18)	13 kHz		17.4%	
(19)	1 MHz			
(20)	<100 kHz			55ps
(21)	600 Hz	2.6%	45%	
(22)	100 Hz	2.1%	30%	170 ps

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