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Sub-Nanosecond Gated Photon Counting for High Spatial Resolution CMOS Imagers

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Abstract—Ultra-fast photon counting in standard CMOS imagers can become very challenging at sub-nanosecond temporal resolutions. This is due to the delay and skew of signal propagation along large pixel arrays. A new edge-based solution is presented, circumventing these limitations. This solution is applied to a Single Photon Avalanche Diode based pixel with an embedded analog counter for time gating photon counting. The analog counter has an adjustable sensitivity ranging from 0.1 mV/photon up to 100 mV/photon. This concept was applied to an image sensor with a row length of approximately 15 mm and 330 pixels per row. The pixel counts 55 transistors with a pitch of 45 μm .

Keywords—ultra-fast gating; SPAD; CMOS image sensor; imager array; photon counting; skew; line delay

I. INTRODUCTION

In recent years, the field of ultra-fast imaging has experienced many key breakthroughs. The ability to push past the sub-nanosecond barrier shown in [1] is particularly interesting as it enables the counting of photons at a very high rate. Several works report Time Correlated Single Photon Counting Systems (TCSPCS) integrating a Time to Digital Converter (TDC) [2][3]. The main advantage of TCSPCS is the high sensitivity, except during its dead time, the Single Photon Avalanche Diode (SPAD) is sensitive to all photons able to trigger the SPAD. The drawback of the TCSPCS is the need to extract the measured data before being able to measure a new photon. This operation generates a high data rate while the number of detected photons is increasing, leading to a possible saturation of the sensor. In some specific cases, the data extraction can be optimized by means of an embedded FIFO and/or an event driven readout [4] [5] but this approach is more suitable for the sensors limited to a one-dimensional spatial information, called a streak sensor (i.e. a sensor with a single row of photo detectors). In the general case of a 2D image sensor, the sensitivity of the high spatial resolution TCSPCS is bottlenecked by the sensor's digital IO. Generally, at least 10 bits per photon are generated in a TCSPCS. The state of the art high speed video sensors generate a data rate up to 40 Gb/s [6]. Based on this, the expected maximal number of photons/s for TCSPCS will be restricted to 4 Giga photons/s.

Time information can also be acquired by time gated operation. Several time windows are used to sample the signal

at different times. Regardless of some saturation or pile up effects, the maximal number of detected photons for a time gated pixel with an embedded photon counter is equal to the product $X \times Y \times F$, where X and Y are the number of columns and rows of pixels of the sensor and F is the gating rate, or $F=1/P$ where P is the minimal dead time of the SPAD sensor. For instance, a 330×330 pixel sensor array and a gating rate of 10 MHz leads to a maximum photon rate of more than 1 Tera photon/s (i.e. an order of magnitude above the TCSPCS). Thus, thanks to an internal counting process, the time gated sensors can be much more sensitive than TCSPCS as the sensor's I/O bottleneck is avoided.

However, a high time resolution requires a short gating time. Sub-ns gating of a single SPAD down to 300 ps has already been reported in [7]. Nevertheless, ensuring a sub-ns gating time is quite challenging in a large sensor array as both the skew and the limited bandwidth of a long line across the sensor alter the time precision. Binary trees can be used in streak imagers to insure a low skew along the sensor. For instance, a 700 ps gate width has been reported in a 1024×8 (24.6mm long) array sensor with a 100 ps skew variation across the entire chip [8]. With 2D image sensors, this method is only applicable to the row (or column) signal buffers with a clock tree beside the sensor [9]. However, the skew along the row (or column) can be as high as the temporal window's width. In [1], we proposed a method for a dedicated row driver and in-pixel fast signal generation for a sub-ns gating operation that maintains the skew below 20 ps rms along an entire row of 20 mm. This technique is used in this work in combination with an in-pixel photon counting unit in order to design a sub-ns Time Gated Single Photon Counting Systems (TGSPCS).

Digital counters are cumbersome and better suited for streak TGSPCS [10]. In order to preserve the fill factor, an analog counter architecture employing a small number of transistors and a capacitor is used [11]. It has already been successfully integrated within a pixel of a 2D SPAD image sensor [12]. Most of the works report counters with a fixed step size around a few tens of a mV. In this work, we present a versatile analog counter architecture suitable for sub-ns operation with an externally adjustable step size for a commutable high sensitivity or high dynamic measurement mode.

II. ULTRA-FAST GATING

Due to the well-known RC distributed effect and signal skew challenges on propagating sub-nanosecond pulses across a long pixel row (greater than 1 cm), conventional techniques involving pulse propagation are inadequate.

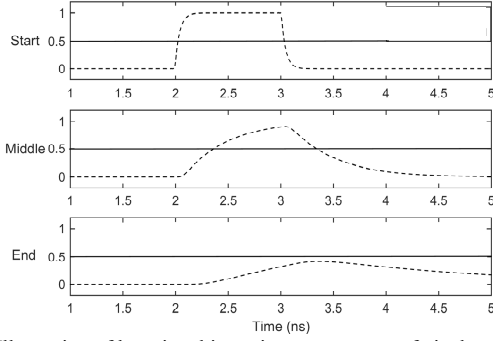


Fig. 1. Illustration of lost signal integrity across a row of pixels.

In Fig. 1, the effect of the RC delay is shown at the beginning, middle and end of a 20 mm image sensor. Evidently, at the end of the row, the pulse no longer crosses half of the supply voltage, thus still seen as a logical zero. A more robust approach using the edge-based technique as described in [1] is more appropriate. It consists of generating two delayed signals instead of one to produce the fast pulse inside the pixel. A signal generator based on this approach can be used to drive the sensitive signals for each row (Fig. 2).

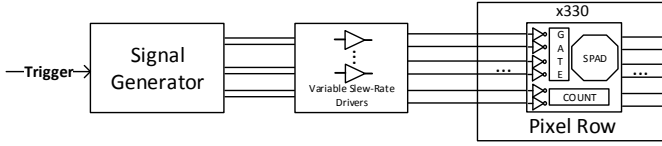


Fig. 2. Schematic of signal generator driving each pixel row.

The signal skew is compensated using a sensor row split into 10 segments with tuned-threshold inverters. This way, using the techniques developed in [1], we ensure that the pulses are generated locally in each pixel with minimal skew.

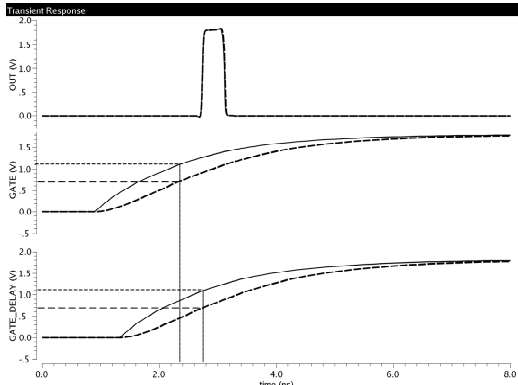


Fig. 3. Simulation of nearly skew-less 330 ps pulse across 20 mm sensor. The solid line represents the signal at the beginning of the sensor and the dotted line the signal at the end.

Due to signal skew, the switching threshold is lowered in each segment across the line so that each segment switches at the same time as the preceding segment. This approach is

validated by the simulation in Fig. 3. While the signal skew is not entirely eliminated, it only measures approximately 10 ps between the beginning and end of a 20 mm long imager array. It is greatly reduced and no longer has a fatal effect on the gating operation of each pixel.

However, certain discrepancies are expected to appear due to fabrication mismatches. Monte-Carlo simulations on the statistical dispersion show that this approach incurs an expected dispersion of 18.42 ps rms [1]. Moreover, the skew compensation approach is based on the slew rate of the two delayed signals, thus it is mandatory to use a variable slew rate driver (Fig. 4), to compensate for its mismatch.

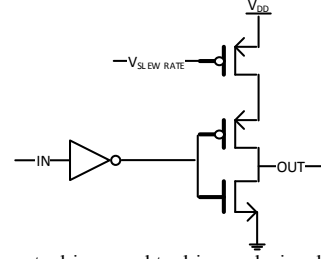


Fig. 4. Variable slew-rate driver used to drive each signal across pixel row.

In Fig. 5, the SPAD's control circuit is controlled by ultra-fast signals (*SPAD RST* and *GATE*). The approach is applied by adding *SPAD RST DELAY* and *GATE DELAY* for edge propagation. Its operation is further detailed in [1]. The tuned-threshold inverters used for skew elimination are added for each ultra-fast signal. This approach is integral in driving sensitive ultra-fast signals used for the gating of a photon counting CMOS image sensor.

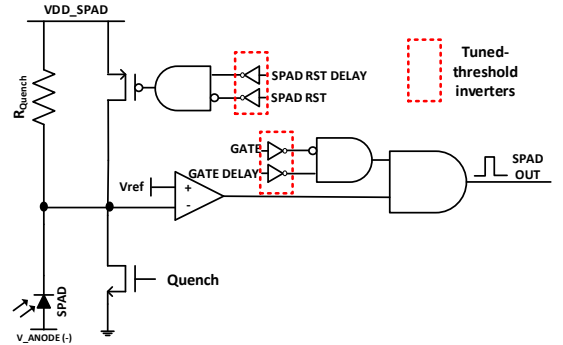


Fig. 5. SPAD Edge-triggered circuit with active quench, reset and gating.

III. PHOTON COUNTING

A. Analog Counter Circuit

A compact, analog photon counting circuit is preferred to a digital one for fill factor considerations. Using a signal generator as in Fig. 2, an ultra-fast TGSPCS can be embedded in each pixel using the analog accumulation technique detailed in [13]. In Fig. 6, this analog counter circuit is detailed. It uses the low integrated capacitance of a floating node C_{INC} , a charge transfer and reset circuit and an integrating capacitor C_{INT} to count the number of detected photons. This system is highly flexible as it can count anywhere between 10 and 10 000 photons by adjusting the V_{Gain} biasing voltage.

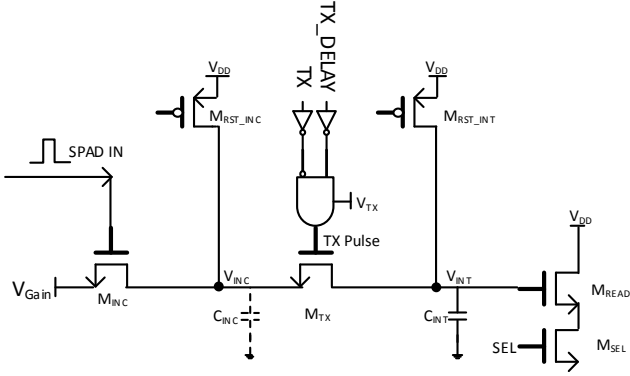


Fig. 6. Analog counter circuit based on charge transfer dependent on the ratio between C_{INC} and C_{INT} .

The timing diagram in Fig. 7 shows two cases, first with a *SPAD IN* pulse arriving between the *RST INC* and *TX PULSE* signals, causing the counter circuit to count and second without the *SPAD IN* pulse, therefore not counted.

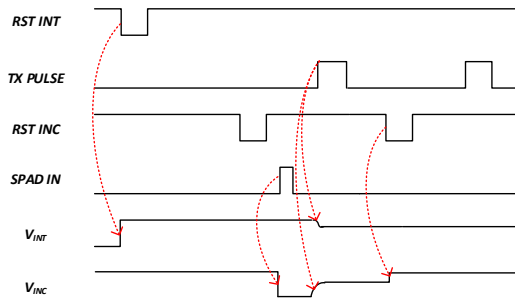


Fig. 7. Timing diagram of analog counter circuit showing the increment caused by the *SPAD IN* pulse.

The M_{TX} can transfer charges as long as its V_{GS} is greater than its threshold voltage. This positive excess voltage is given by:

$$V_{ex} = V_{GS_{TX}} - V_{TX} \quad (1)$$

The total transferable charge, initially stored in C_{INC} , is given by:

$$Q_{ex} = C_{INC} \times V_{ex} \quad (2)$$

The transferable charges flow from C_{INC} to C_{INT} leading to the following voltage variation:

$$\Delta V_{INT} = \frac{Q_{ex}}{C_{INT}} = \frac{C_{INC}}{C_{INT}} \times V_{ex} \quad (3)$$

C_{INT} is typically several times greater than C_{INC} (10 fF and 2 fF respectively in our case). The count step size can be set by three variables: V_{Gain} , V_{TX} and the *TX PULSE* duration. By changing V_{Gain} or V_{TX} , V_{ex} is varied. As V_{Gain} increases, V_{ex} becomes smaller; hence there is less charge to transfer. This results in a smaller step size and larger counting range up to 50 000. However, once V_{Gain} gets too high, using (3), the transferred charge becomes too close to the single electron range and it is statistically unreliable. Furthermore, for a *TX PULSE* duration of a few ns, the charge transfer is not completed entirely and can be increased with larger pulse widths.

B. Analog Counter Simulation Results

The analog integration circuit has been simulated to show a versatile photon counting range (10-10 000) which is suitable

for ultra-fast imaging applications using SPADs. The simulation window in Fig. 8 shows that the analog counter is capable of reaching a pre-determined threshold of 1 V in a wide range of step sizes.

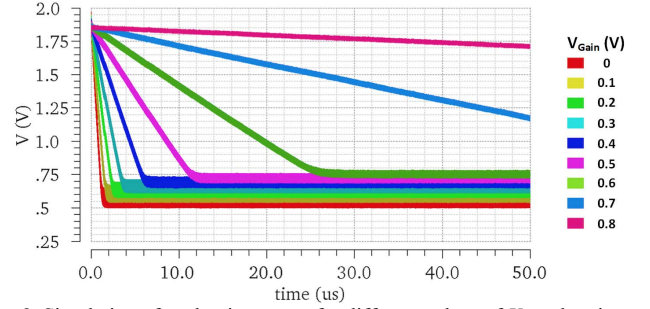


Fig. 8. Simulation of analog integrator for different values of V_{Gain} showing versatile counting range reaching 1 V in 10 to 10000 steps.

As each photon is counted, the counter circuit steps down its output voltage. Remarkably, the response is highly linear. Furthermore, in Fig. 9, it can be seen that the response of the analog counter circuit is linear with an R^2 of 0.9982 and a 2 quantum maximal error.

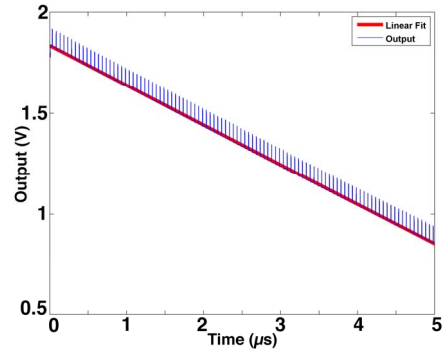


Fig. 9. Analog counter output simulation for $V_{Gain} = 0.4$ V with fit curve showing a linear response at 99.98%.

IV. SIMULATION RESULTS

Using the edge-gating technique, SPAD imager arrays can be gated using ultra-fast signals. Moreover, using the analog counter circuit for photon counting applications, we are able to count up to 10 000 photons for each pixel. Furthermore, as the edge-gating technique used for this application can reach sub-nanosecond temporal resolutions, a system can be designed to obtain a gating of 200 ps. The previous simulations show that this approach is ideal for time gated photon-counting large CMOS image sensors.

A. Ultra-fast Gating

Ultra-fast gating has been simulated using the test bench setup seen in Fig. 2 and Fig. 10. The simulated pixel uses the SPAD model seen in [15]. A simulation of the photon arrival in function of the temporal position of the gating window was performed. A total skew of 25 ps peak-to-peak across the 10 33-pixel segments was obtained for a total row length of 15 mm. This solidifies that sub-ns gating is possible on large imager arrays.

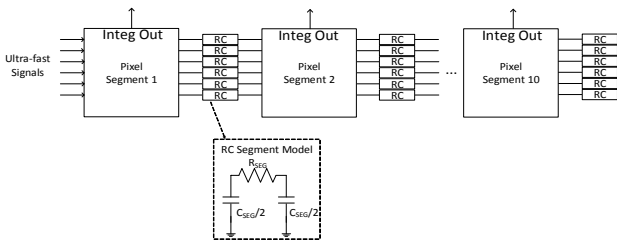


Fig. 10. Test bench used for simulating a gating window across a 15 mm sensor where each ultra-fast signal is injected into 10 segments for skew compensation.

The simulation in Fig. 11 shows the integration quantum at the output before and after the arrival of a photon. This simulation does not take into account the SPAD jitter. Generally, SPAD jitter is approximately 100 ps FWHM (Full Width at Half Maximum) [14]. In practice, the jitter will further smooth the gating window. This shows that the temporal resolution is limited by the SPAD's characteristics rather than the surrounding electronics.

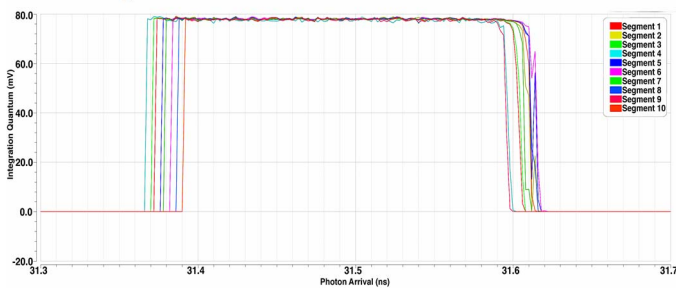


Fig. 11. Simulation of a single photon counting voltage change with a 220 ps gating window showing a near simultaneous results across all 10 segments of the imager.

B. Monte-Carlo Simulations

For sub-ns resolutions, it is important to consider the expected dispersion due to fabrication process mismatches. This approach is highly sensitive to transistor size variations, such as those used for skew compensation. The expected dispersion between the first two segments is 38.32 ps and between the first and last, 31.47 ps. Therefore, the dispersion is constant throughout an entire row and similar to previous works [8][12].

V. CONCLUSION

This paper presents an application of a sub-nanosecond ultra-fast gating technique of a SPAD applied to large imager arrays in conjunction with a versatile analog photon counter. The analog counter offers a wide counting range from several photons to tens of thousands. The gating obtained for this pixel can go as short as 200 ps FWHM with a 38 ps rms skew across the entire array. Contrarily to the streak imaging sensors (1D) in [8] and [12], our approach does not require a signal distribution tree and it is applicable to 2D imagers with a shorter gating time. To our knowledge, it is the first large size sub-ns gated 2D image sensor reported. CMOS ultra-fast gated image sensors could be an alternative for the current state of the art, ultra-fast gated intensified cameras using vacuum tube technology [16].

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