



HAL
open science

Analog and RF modeling of FDSOI UTBB MOSFET using Leti-UTSOI model

Salim El Ghouli, Patrick Scheer, Michel Minondo, André Juge, Thierry Poiroux, Jean-Michel Sallese, Christophe Lallement

► **To cite this version:**

Salim El Ghouli, Patrick Scheer, Michel Minondo, André Juge, Thierry Poiroux, et al.. Analog and RF modeling of FDSOI UTBB MOSFET using Leti-UTSOI model. 23rd International Conference Mixed Design of Integrated Circuits and Systems (MIXDES), Jun 2016, Lodz, Poland. 10.1109/MIXDES.2016.7529697 . hal-03513616

HAL Id: hal-03513616

<https://hal.science/hal-03513616>

Submitted on 5 Jan 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Analog and RF modeling of FDSOI UTBB MOSFET using Leti-UTSOI model

Salim El Ghoul¹, Patrick Scheer¹, Michel Minondo¹,
André Juge¹

¹STMicroelectronics, Crolles, France
salim.elghouli@st.com

Thierry Poiroux², Jean Michel Sallese³, Christophe
Lallement⁴

²CEA-Leti, Grenoble, France

³EPFL, Lausanne, Switzerland

⁴ICube-University of Strasbourg, Strasbourg, France

Abstract— Ultra-Thin Body and Box (UTBB) Fully-depleted Silicon-on-Insulator (FDSOI) MOSFETs exhibit very high transit frequency granting advantageous RF and low-power circuits design. This requires accurate models describing transistor behavior in all operating regimes including low levels of MOSFET channel inversion. In this paper, Leti-UTSOI based RF model will be compared against electrical measurements from 28nm FDSOI devices operating down to low bias conditions. The outcome demonstrates the accuracy and efficiency of Leti-UTSOI for low-power and RF applications design.

Keywords— FDSOI; UTBB; Leti-UTSOI; Analog and RF; Compact Model; low-power

I. INTRODUCTION

Both FinFET and planar Fully Depleted SOI (FDSOI) technologies fulfill the International Technology Roadmap for Semiconductors (ITRS) requirements for device downscaling. The two architectures allow excellent channel control for high digital performances [1][2][3]. However, analog and RF performances are affected unevenly.

It has been demonstrated that planar FDSOI technology with ultra-thin Body and BOX (UTBB) transistors exhibits excellent analog and RF performances and outperforms bulk and FinFET technologies on various RF aspects [4][5]. Furthermore, FDSOI is claimed to outperform FinFET in terms of cutoff frequencies [6]. In recent low power and high performance circuits such as those implemented in FDSOI for IoT market, one needs to operate MOSFET transistors from weak to strong inversion levels [7]. It is worth pointing that moderate inversion region has been found to be a good compromise while power consumption and speed are valued equally [8][9][10].

In order to fully benefit from the advantages of the FDSOI technology, MOSFET compact models should accurately reproduce transistor behavior in all regions of operation especially in low inversion. Leti-UTSOI is the first available independent double-gate compact model able to describe accurately the UTBB MOSFET in all bias conditions, including strong forward back bias [11].

Leti-UTSOI model was validated against numerical simulations and measurements for DC operation showing excellent predictability and scalability properties [12]. However, its RF capabilities have been only highlighted in [13] and clearly

ask for more in depth analysis. This paper will focus on the ability of Leti-UTSOI model to describe the small signal RF behavior of UTBB MOSFET at low voltage biases. The paper will first focus on the DC operation of the Leti-UTSOI model, especially for low inversion levels, introducing electrical parameters normalization process. Secondly, RF figures of merit will be compared versus measurements with emphasis on moderate inversion.

II. DC AND LOW FREQUENCY OPERATIONS

A. Leti-UTSOI model

Leti-UTSOI (UTSOI) is a surface potential based compact model describing the ultra-thin fully depleted SOI MOSFET with a lightly doped silicon film [14]. UTSOI physical core is suitable for any independent double gate transistor with low-doped channel, and in particular for UTBB-FDSOI architectures as depicted in Fig. 1. The device parameters are $T_{Si} = 7$ nm (silicon film thickness), $T_{ox2} = 25$ nm and $T_{ox1} = 1.3$ nm (equivalent back and front gates oxide thicknesses respectively), and a Well-type implantation is used for the ground-plane or back gate region under the BOX [15].

Explicit formulations of the front and back surface potentials (ψ_{s1} , ψ_{s2}) are used to calculate the drain current (I_D) and the intrinsic mobile charge (Q_{inv}). Short and narrow channel effects, series resistance, overlap capacitance, fringing capacitance and backplane related parasitic capacitances are all accounted for.

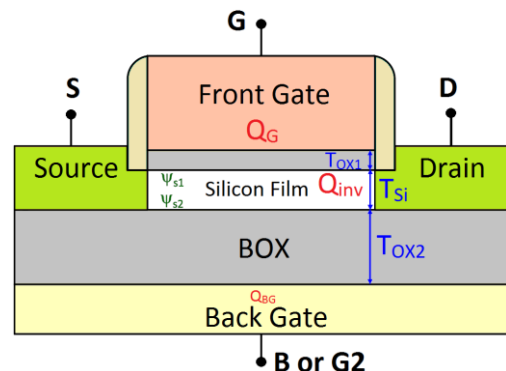


Fig. 1. UTBB transistor architecture (cross-section) with modeled charges as well as front and back surface potentials.

UTSOI small-signal equivalent schematic valid in low-frequency operation is depicted in Fig. 2. It includes intrinsic MOSFET components and extrinsic elements such as source and drain series resistances (R_s and R_d respectively). Even though explicit resistances are shown in Fig. 2, UTSOI takes series resistances effect implicitly. Gate-to-source (C_{gs}), gate-to-drain (C_{gd}) and front-to-back gates (C_{gb}) capacitances are also included as shown in Fig. 2.

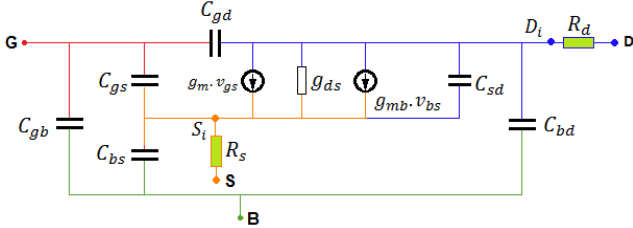


Fig. 2. UTSOI equivalent schematic for small signal and low-frequency operation including series resistances R_s and R_d .

The UTSOI satisfies continuity requirements for currents and capacitances as well as for their higher order derivatives. It is compliant with all MOSFET standard models criteria such as DC and AC symmetry and robustness in all operating conditions [16].

B. DC Model extraction and normalization

DC and CV operations accuracy is a prerequisite for RF modeling. External connections related resistances are extracted before proceeding to a standard extraction flow similar to the one described in [17]. Parasitic series resistances are extracted using dedicated RF “SHORT” structures DC and S-parameters measurements. The SHORT structure represents the measured Device Under Test (DUT) where gate, drain and common source and back gate are all shorted (Fig. 3).

Several gate lengths and widths are measured and used for DC parameters extraction purpose. Long and wide structures are first used to extract main model parameters such as front oxide and BOX thicknesses, gates work-functions, effective and saturated mobility parameters and gate leakage. Short and narrow devices are then used to extract small geometry effects parameters. In saturation, fine tuning requires an estimate of the structure environment thermal resistance.

In the following, measured and simulated quantities are normalized as described in Table I.

TABLE I. NORMALIZATION

Quantity	Normalization
Drain Current: I_D	$I_d = I_D / (W/L)$
Capacitance: C	$C / (C_{ox} \cdot W \cdot L)$
Gate Voltage: V_G	Overdrive: $V_{gt} = \text{TYPE} \cdot (V_G - V_{T0})$
Transconductance: G_m	$g_m = G_m / G_{m_max}$
Cutoff frequency: F_x	$f_x = F_x / F_{x_max}$

where C_{ox} is the oxide capacitance density, V_{T0} is the threshold voltage, TYPE is 1 for NMOS and -1 for PMOS, V_{gt} is the gate overdrive voltage, G_{m_max} is the maximum transconductance and F_{x_max} is the maximum value of the related cutoff frequency.

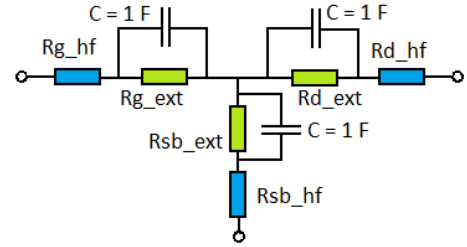


Fig. 3. SHORT structure equivalent schematic used to extract parasitic external resistances R_{g_ext} , R_{d_ext} and R_{sb_ext} (gate, drain and common source and back gate terminals series resistances respectively, source and back gate being shorted).

C. DC model assessment

In this section DC and CV UTSOI operation is compared against measurements of short and long ($L = 30$ nm and 2 μm respectively) NMOS and PMOS devices. To be consistent with RF operation assessment, multi-finger structures are used (with a number of fingers of $N_f = 10$). NMOS convention gate voltage overdrive $V_{gt} = \text{TYPE} \cdot (V_G - V_{T0})$ is used for current, transconductance and capacitance plots.

1) IV operation

Accurate transfer characteristic $I_d(V_G)$ simulation is a critical condition for rigorous analog and RF modeling. Not only is the drain current accuracy required but also its first (transconductance) and second derivatives to estimate parasitic signal distortions in RF operation. Fig. 4 shows the transfer characteristic for NMOS and PMOS considering short and long channels. The normalized drain current in logarithmic scale is convenient to capture weak and moderate inversion behaviors while the linear scale highlights the strong inversion region, see Fig. 5. Subthreshold slope is accurately captured in weak inversion for both long and short channels. In strong inversion, series resistance impact, length modulation as well as mobility saturation effects (noticeable even at low $|V_{Dl}|$) are correctly reproduced. UTSOI is also correctly describing the complex moderate inversion region.

Normalized transconductance g_m is shown in logarithmic and linear scales in Fig. 6 and Fig. 7 (inset being the second order derivative of the current) respectively vs. overdrive voltage (linear scale) for short and long channel NMOS and PMOS.

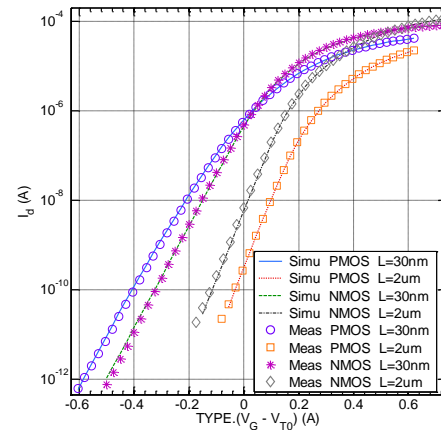


Fig. 4. I_d vs. gate voltage overdrive in linear operation $|V_{Dl}| = 0.3$ V for two NMOS and PMOS lengths ($L = 30$ nm and 2 μm), $W_f = 2$ μm and $N_f = 10$ at $T = 25^\circ\text{C}$.

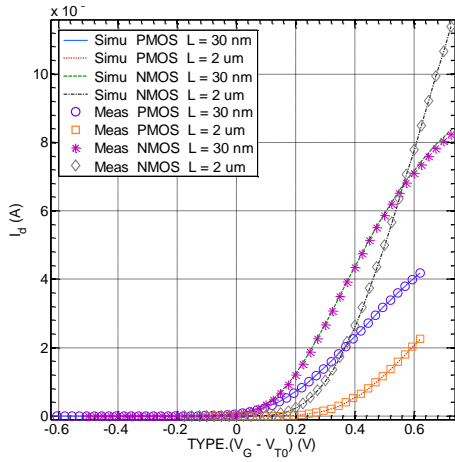


Fig. 5. I_d vs. $\text{TYPE} \cdot (V_G - V_{T0})$ in linear operation $|V_D| = 0.3$ V for two NMOS and PMOS lengths ($L = 30$ nm and $2 \mu\text{m}$), $W_f = 2 \mu\text{m}$ and $N_f = 10$ at $T = 25^\circ\text{C}$.

An excellent matching with the transconductance and its derivative in weak, moderate and strong inversion is observed. The normalized transconductance efficiency FOM is depicted in Fig. 8 vs. the normalized drain current. This FOM is important for low-power analog and RF design [18]. Transconductance efficiency chart allows accurate hand calculation in all MOSFET inversion regions including moderate inversion that is complex to model and no analytical model is required. The results show UTSOI capability to accurately reproduce the UTBB DC behavior.

2) CV operation

For accurate low-voltage analog and RF modeling, MOSFET capacitances should be predicted in all operating conditions including moderate and weak inversion regions. In Fig. 9 and Fig. 10 normalized total gate capacitance C_{gg} and C_{gd} capacitance are displayed vs. gate voltage overdrive at $|V_D| = 0.3$ V and Source and Back Gate terminals grounded. C_{gg} and C_{gd} capacitances are correctly captured using UTSOI despite possible strong fringing capacitances impact.

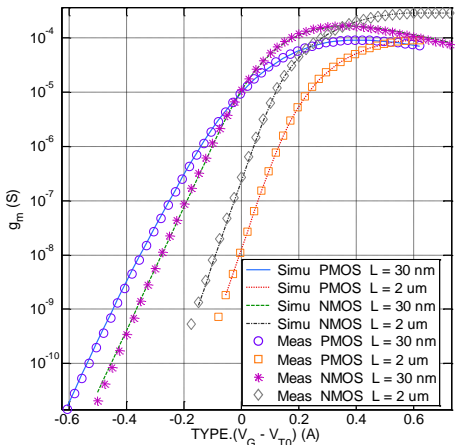


Fig. 6. Transconductance (g_m) vs. overdrive $\text{TYPE} \cdot (V_G - V_{T0})$ in linear operation $|V_D| = 0.3$ V for two NMOS and PMOS lengths ($L = 30$ nm and $2 \mu\text{m}$), $W_f = 2 \mu\text{m}$ and $N_f = 10$ at $T = 25^\circ\text{C}$.

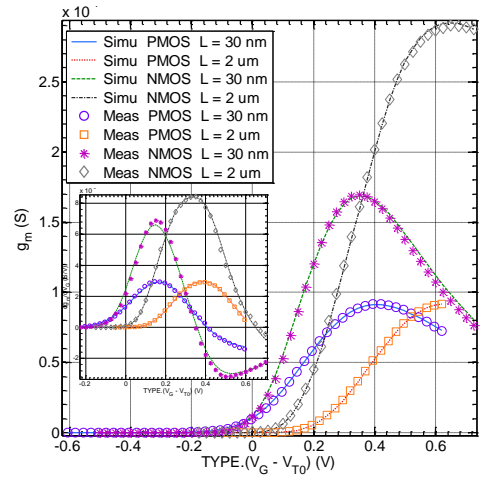


Fig. 7. g_m'' vs. $\text{TYPE} \cdot (V_G - V_{T0})$ in linear operation $|V_D| = 0.3$ V for two NMOS and PMOS lengths ($L = 30$ nm and $2 \mu\text{m}$), $W_f = 2 \mu\text{m}$ and $N_f = 10$ at $T = 25^\circ\text{C}$. Second I_d derivative is in the inset plot.

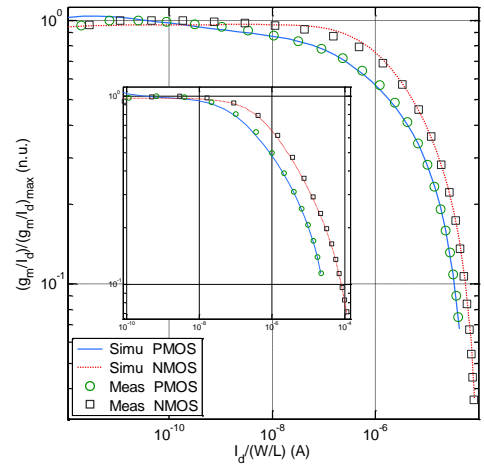


Fig. 8. Normalized Transconductance efficiency vs. I_d in linear operation $|V_D| = 0.3$ V for NMOS and PMOS ($L = 30$ nm, $W_f = 2 \mu\text{m}$ and $N_f = 10$ at $T = 25^\circ\text{C}$). NMOS and PMOS for $L = 2 \mu\text{m}$ is included in inset figure.

III. RF AND HIGH FREQUENCY OPERATION

Only DC-based extraction leads to RF performance overestimation therefore RF extraction is required to mitigate high frequency operation real performances. To this purpose, Multi-finger MOSFET structures are embedded in Coplanar Waveguide (CPW) pads for RF characterization. Multi-finger and wide structures are used to obtain higher RF gain since $g_m \sim N_f \cdot W/L$. S-parameters are measured in a frequency range from 100 MHz up to 110 GHz in linear, saturation and for all channel inversion levels: weak, moderate and strong. A standard 2-port measurement setup shown in Fig. 11 is used where Gate and Drain represent port 1 and 2 respectively, source and back gate being shorted and grounded.

A. RF extraction and equivalent schematic

Capacitive and resistive extrinsic contributions (outside MOSFET channel) must be characterized and excluded carefully. In order to get rid of these parasitic contributions, RF

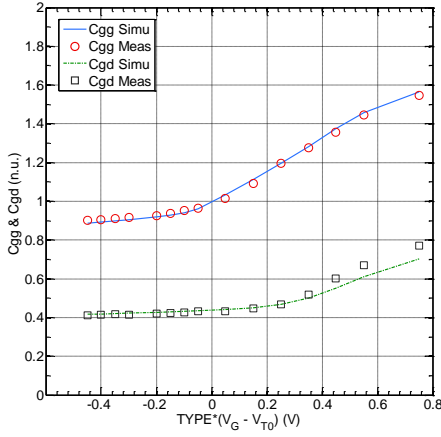


Fig. 9. C_{gg} and C_{gd} vs. gate voltage overdrive $TYPE \cdot (V_G - V_{T0})$ in linear operation $|V_D| = 0.3$ V for NMOS ($L = 30$ nm, $W_f = 2$ μ m and $N_f = 10$) at $T = 25^\circ\text{C}$ and frequency = 100 MHz. W_f and N_f refer to one finger width and number of fingers respectively.

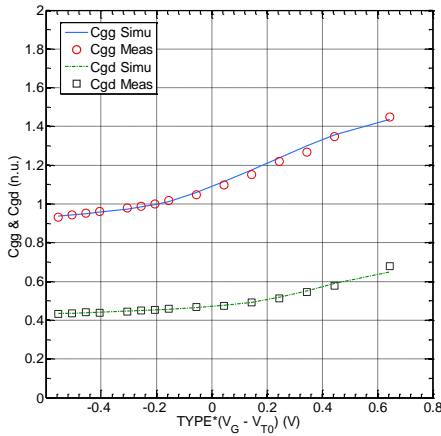


Fig. 10. C_{gg} and C_{gd} vs. gate voltage overdrive $TYPE \cdot (V_G - V_{T0})$ in linear operation $|V_D| = 0.3$ V for PMOS ($L = 30$ nm, $W_f = 2$ μ m and $N_f = 10$) at $T = 25^\circ\text{C}$ and frequency = 100 MHz.

measurements are de-embedded using dedicated OPEN and SHORT structures for each measured device. DC-extraction flow undergone in the previous section is a prerequisite for RF extraction. No fine-tuning is required for UTSOI DC extracted capacitances and series resistances, SHORT structure being used for parasitic resistances extraction before DC-extraction flow.

For high frequency operation, UTSOI requires the addition of a distributed front gate resistance R_g similar to the PSP standard model one [17] and a back gate resistance R_b . The final equivalent schematic is shown in Fig. 12 (right) where series resistances R_s and R_d are included in UTSOI and already extracted in previous DC related section. Front gate resistance R_g takes into account several contributions shown in Fig. 12 (left): (a) the contact resistances, (b) the horizontal gate sheet resistance and finally (c) the vertical gate resistance related to the processed gate stack. R_g is calculated as:

$$R_g = \frac{1}{N_f} \left(R_{contact} + R_{sh} \cdot \frac{W_f}{3 \times L} + R_{int} \cdot \frac{1}{L \times W_f} \right) \quad (1)$$

where $R_{contact}$ is the unitary contact resistance, R_{sh} is the horizontal sheet resistance and R_{int} is the interface vertical resistance.

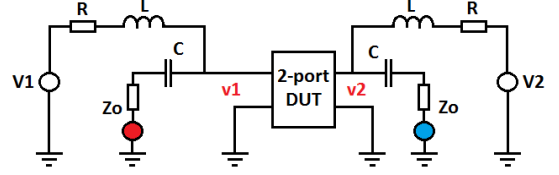


Fig. 11. 2-port RF structures S-parameters measurement setup.

Back gate resistance R_b describes the resistive access to the ground plane underneath the BOX. R_b resistance takes into account the structure layout in a simple manner using access perimeter P_{bgate} . In the following R_b expression, the horizontal resistive path under the box is considered to be negligible in comparison to the vertical strap access.

$$R_b = R_{bsh} \times \frac{1}{P_{bgate}} \quad (2)$$

In order to extract R_b and R_g related parameters, deembedded S-parameters are transformed into Y-parameters and following two expressions are fitted in high frequency operation:

$$R_g = \frac{Re[Y_{11}]}{(Im[Y_{11}])^2} \quad (3)$$

This expression is used to calculate the effective high frequency gate resistance. The second expression is the well-known Mason's Unilateral Gain that is sensitive to R_b :

$$U = \frac{|Y_{21} - Y_{12}|^2}{4 \cdot (Real(Y_{11}) \cdot Real(Y_{22}) - Real(Y_{12}) \cdot Real(Y_{21}))} \quad (4)$$

Transconductance is extracted in DC using drain current derivative and also in RF using $Re(Y_{21} - Y_{12})$ expression. It is important to point out that in low-frequency, the two quantities must be equal and should diverge at high frequency operation as the effective transconductance and consequently gain decreases with frequency increase.

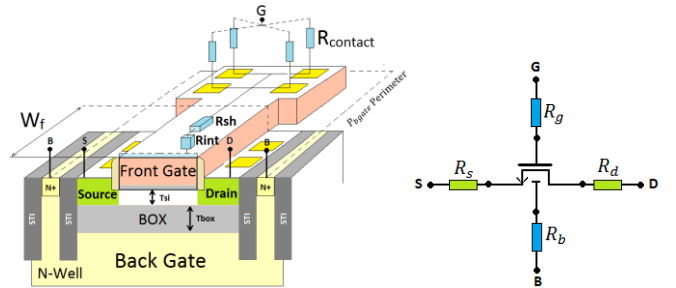


Fig. 12. Left: UTBB transistor architecture (3D). Right: RF equivalent schematic proposal with additional front-gate (R_g) and back-gate (R_b) resistances.

B. f_T and f_{max} figures of merit

Two important RF Figures of Merit (FOMs) are the transit frequency of the current gain and the cut-off frequency of the

Mason's unilateral power gain. The first quantity denoted f_T is an interesting FOM for high-speed digital applications where speed and high swing are required. It is extracted at 0 dB current gain $|H_{21}|_{dB}$ (or $|H_{21}| = 1$). Fig. 13 shows the current gain plots for several inversion levels. We notice that gain becomes practically constant for low levels of inversion. This occurs at higher frequencies and f_T extraction at $|H_{21}| = 1$ is still valid provided a suitable -20 dB asymptote is used. Current gain $|H_{21}|$ vs. frequency presented in Fig. 13 as well as f_T vs. I_d shown in Fig. 14 are accurately reproduced with UTSOI model.

f_T alone is not sufficient to assess MOSFET performance at high frequency operation as it does not account for the impact of some important parasitic elements such as the gate resistance. f_{max} however, defined as the frequency at which the extrapolated Mason's gain given by expression (4), is a more suitable FOM for RF analog applications such as microwave amplifiers. Both front gate and back gate resistances impact is accounted for using f_{max} FOM vs. I_d .

Fig. 15 shows the simulated and measured f_{max} vs. I_d demonstrating the enhanced UTSOI RF model accuracy at high frequency operation. At weak inversion, Mason's gain slope increases with frequency and this behavior is captured with R_b resistance [19]. Back gate resistance R_b impact is revealed and correctly reproduced in the frequency dependence of f_{max} vs. I_d curves particularly in weak inversion up to 80 GHz (Fig. 16).

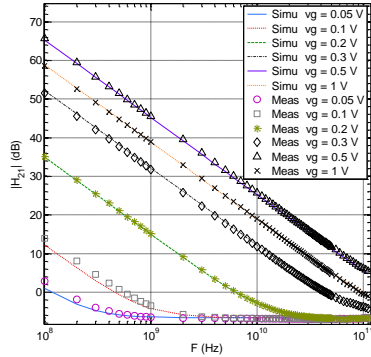


Fig. 13. Small signal current gain ($|H_{21}|$) vs. frequency (F) in linear operation $|V_D| = 0.3$ V for NMOS ($L = 30$ nm, $W_f = 2$ μ m and $N_f = 10$) at $T = 25^\circ\text{C}$.

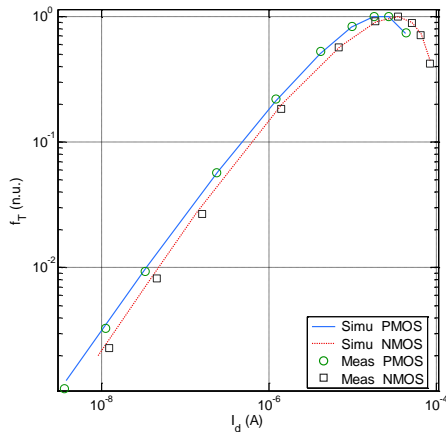


Fig. 14. Transit frequency (f_T) vs. I_d in linear operation $|V_D| = 0.3$ V for NMOS and PMOS ($L = 30$ nm, $W_f = 2$ μ m and $N_f = 10$) at $T = 25^\circ\text{C}$.

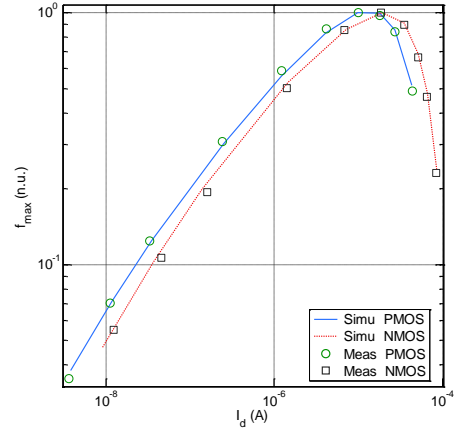


Fig. 15. f_{max} vs. I_d in linear operation $|V_D| = 0.3$ V for NMOS and PMOS ($L = 30$ nm, $W_f = 2$ μ m and $N_f = 10$) at $T = 25^\circ\text{C}$.

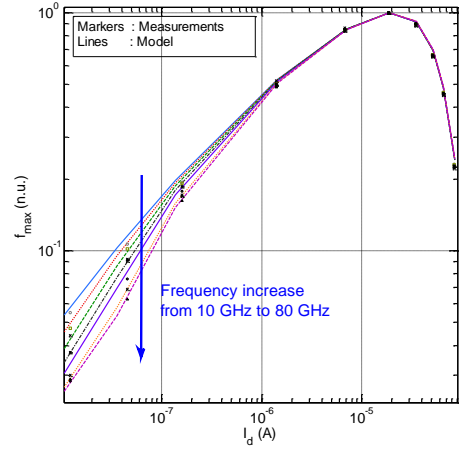


Fig. 16. f_{max} vs. I_d in linear operation $|V_D| = 0.3$ V for NMOS and for following frequencies: 10 GHz, 20 GHz, 30 GHz, 40 GHz, 50 GHz, 70 GHz and 80 GHz ($L = 30$ nm, $W_f = 2$ μ m and $N_f = 10$) at $T = 25^\circ\text{C}$.

C. Performance and consumption tradeoff FOM

f_T and f_{max} figures of merit are suitable for applications where only speed/performance is valued. The maximum value of these FOMs is obtained in strong inversion where transconductance efficiency (g_m/I_d) is low. Consequently, these FOMs are not suitable for low-voltage RF applications where performance and consumption are valued equally. The more convenient FOM for such low-consumption and high speed applications is the one introduced in [20] and given as:

$$FOM_{RF} = f_T \cdot \frac{g_m}{I_d} \quad (5)$$

This FOM captures both the transconductance efficiency and RF performance. It is also convenient as it allows to keep the noise factor in sight [21]. The maximum value of this RF FOM represents the best tradeoff between power consumption and speed.

In Fig. 17, FOM_{RF} vs. I_d is shown for NMOS and PMOS. Both MOSFET types present a maximum and consequently an optimum trade-off in moderate inversion region. UTSOI model is accurately reproducing this RF FOM measurements too.

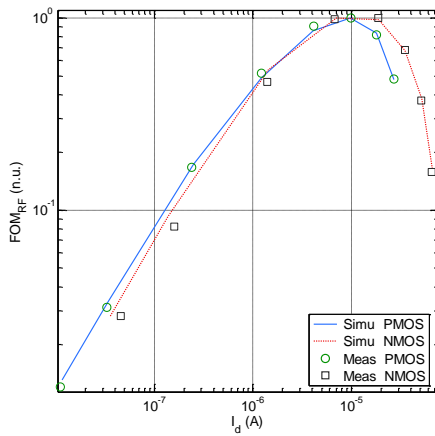


Fig. 17. FOM_{RF} vs. I_d in linear operation $|V_D| = 0.3$ V for NMOS and PMOS ($L = 30$ nm, $W_f = 2$ μ m and $N_f = 10$) at $T = 25^\circ$ C.

IV. CONCLUSION

In this work we demonstrate that Leti-UTSOI based model is well-suited for modeling 28 nm UTBB FDSOI NMOS and PMOS RF devices. Characterization conditions include length scaling down to nominal value, a wide frequency range up to 110 GHz, and operation under different channel inversion levels down to low current and low voltage regime. An excellent agreement is shown over more than eight decades of current density for DC and four decades for RF. The optimum operating point for low-power RF lies in the moderate inversion where UTSOI model is very well-suited. In particular, this work demonstrates the accuracy of Leti-UTSOI based RF models to enable RF and Low Power circuit design applications in UTBB FDSOI technology.

ACKNOWLEDGMENT

The authors would like to thank Clément Charbuillet, Vincent Quenette, Gilles Gouget, Frederic Dauge, Michel Buczko, Sebastien Jan and Hervé Jaouen from STMicroelectronics for their collaboration, support and advice.

REFERENCES

- [1] N. Chevillon, J. M. Sallese, C. Lallemand, F. Prégaldiny, M. Madec, J. Sedlmeir, and J. Aghassi, "Generalization of the Concept of Equivalent Thickness and Capacitance to Multigate MOSFETs Modeling," *IEEE Transactions on Electron Devices*, vol. 59, no. 1, pp. 60–71, Jan. 2012.
- [2] A. Yesayan, F. Prégaldiny, N. Chevillon, C. Lallemand, and J.-M. Sallese, "Physics-based compact model for ultra-scaled FinFETs," *Solid-State Electronics*, vol. 62, no. 1, pp. 165–173, Aug. 2011.
- [3] J. Hartmann, "FD-SOI Technology Development and Key Devices Characteristics for Fast, Power Efficient, Low Voltage SoCs," in *Compound Semiconductor Integrated Circuit Symposium (CSICs)*, 2014 IEEE, 2014, pp. 1–4.
- [4] D. Flandre, J. P. Colinge, J. Chen, D. D. Ceuster, J. P. Eggermont, L. Ferreira, B. Gentinne, P. G. A. Jespers, A. Viviani, R. Gillon, J. P. Raskin, A. V. Vorst, D. Vanhoenacker-Janvier, and F. Silveira, "Fully-Depleted SOI CMOS Technology for Low-Voltage Low-Power Mixed Digital/Analog/Microwave Circuits," *Analog Integrated Circuits and Signal Processing*, vol. 21, no. 3, pp. 213–228, Dec. 1999.
- [5] V. Kilchytka, S. Makovejev, M. K. Md Arshad, J.-P. Raskin, and D. Flandre, "Perspectives of UTBB FD SOI MOSFETs for Analog and RF Applications," in *Functional Nanomaterials and Devices for Electronics, Sensors and Energy Harvesting*, A. Nazarov, F. Balestra, V. Kilchytka,

- and D. Flandre, Eds. Cham: Springer International Publishing, 2014, pp. 27–46.
- [6] J.-P. Raskin, "FinFET versus UTBB SOI - a RF perspective," in *Solid State Device Research Conference (ESSDERC)*, 2015 45th European, 2015, pp. 84–88.
- [7] D. M. Binkley, "Tradeoffs and Optimization in Analog CMOS Design," in *14th International Conference on Mixed Design of Integrated Circuits and Systems*, 2007. MIXDES '07, 2007, pp. 47–60.
- [8] A. Mangla, C. C. Enz, and J. M. Sallese, "Figure-of-merit for optimizing the current-efficiency of low-power RF circuits," in *Mixed Design of Integrated Circuits and Systems (MIXDES)*, 2011 Proceedings of the 18th International Conference, 2011, pp. 85–89.
- [9] V. Kilchytka, M. K. Md Arshad, S. Makovejev, S. Olsen, F. Andrieu, T. Poiroux, O. Faynot, J.-P. Raskin, and D. Flandre, "Ultra-thin body and thin-BOX SOI CMOS technology analog figures of merit," *Solid-State Electronics*, vol. 70, pp. 50–58, Apr. 2012.
- [10] S. El Ghouli, P. Scheer, T. Poiroux, A. Juge, J.M. Sallese and C. Lallemand, "Dynamic behavior of the UTBB FDSOI MOSFET", MOS-AK Workshop, Grenoble, France, March 2015.
- [11] T. Poiroux, O. Rozeau, P. Scheer, S. Martinie, M. A. Jaud, M. Minondo, A. Juge, J. C. Barbé, and M. Vinet, "Leti-UTSOI2.1: A Compact Model for UTBB-FDSOI Technologies - Part I: Interface Potentials Analytical Model," *IEEE Transactions on Electron Devices*, vol. 62, no. 9, pp. 2751–2759, Sep. 2015.
- [12] T. Poiroux, O. Rozeau, P. Scheer, S. Martinie, M. A. Jaud, M. Minondo, A. Juge, J. C. Barbé, and M. Vinet, "Leti-UTSOI2.1: A Compact Model for UTBB-FDSOI Technologies - Part II: DC and AC Model Description," *IEEE Transactions on Electron Devices*, vol. 62, no. 9, pp. 2760–2768, Sep. 2015.
- [13] J. C. Barbé, L. Lucci, A. Siligaris, P. Vincent, and O. Faynot, "4-port RF performance assessment and compact modeling of UTBB-FDSOI transistors," in *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2015, pp. 355–358.
- [14] T. Poiroux, O. Rozeau, S. Martinie, P. Scheer, S. Puget, M. A. Jaud, S. El Ghouli, J. C. Barbé, A. Juge, and O. Faynot, "UTSOI2: A complete physical compact model for UTBB and independent double gate MOSFETs," in *2013 IEEE International Electron Devices Meeting*, 2013, pp. 12.4.1–12.4.4.
- [15] N. Planes, O. Weber, V. Barral, S. Haendler, D. Noblet, D. Croain, M. Bocat, P. Sassoulas, X. Federspiel, A. Cros, and others, "28nm FDSOI technology platform for high-speed low-voltage digital applications," in *VLSI Technology (VLSIT)*, 2012 Symposium on, 2012, pp. 133–134.
- [16] X. Li, W. Wu, A. Jha, G. Gildenblat, R. van Langevelde, G. D. J. Smit, A. J. Scholten, D. B. M. Klaassen, C. C. McAndrew, J. Watts, C. M. Olsen, G. J. Coram, S. Chaudhry, and J. Victory, "Benchmark Tests for MOSFET Compact Models With Application to the PSP Model," *IEEE Transactions on Electron Devices*, vol. 56, no. 2, pp. 243–251, Feb. 2009.
- [17] G.D.J. Smit, A.J. Scholten, D.B.M. Klaassen and R. van der Toorn, PSP 103.3 User's manual.
- [18] F. Silveira, D. Flandre, and P. G. A. Jespers, "A g m/I D based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *Solid-State Circuits*, *IEEE Journal of*, vol. 31, no. 9, pp. 1314–1319, 1996.
- [19] B. Dormieu, P. Scheer, C. Charbuillet, S. Jan, F. Danneville, "4-Port isolated MOS modeling and extraction for mmW applications", *Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, ISSN1930-8876, September 2012, pp.54–57.
- [20] A. Shameli and P. Heydari, "Ultra-Low Power RFIC Design Using Moderately Inverted MOSFETs: An Analytical/Experimental Study," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2006, pp. 470–473, 2006.
- [21] A. Mangla, M.-A. Chalkiadaki, F. Fadhuile, T. Taris, Y. Deval, and C. C. Enz, "Design methodology for ultra low-power analog circuits using next generation BSIM6 MOSFET compact model," *Microelectronics Journal*, vol. 44, no. 7, pp. 570–575, Jul. 2013.