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► **To cite this version:**

Kotb Jabeur, Gregory Di Pendina, Fabrice Bernard-Granger, Guillaume Prenat. Spin orbit torque non-volatile flip-flop for high speed and low energy applications. *IEEE Electron Device Letters*, 2014, 35 (3), pp.408 - 410. 10.1109/led.2013.2297397 . hal-03506992

HAL Id: hal-03506992

<https://hal.science/hal-03506992>

Submitted on 12 Jan 2022

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Spin orbit torque non-volatile flip-flop for high speed and low energy applications

K. Jabeur, G. Di Pendina, F. Bernard-Granger, G. Prenat

Abstract—A novel non-volatile flip-flop based on spin-orbit torque magnetic tunnel junctions (SOT-MTJ) is proposed for fast and ultra-low energy applications. A case study of this non-volatile flip-flop is considered. In addition to the independence between writing and reading paths which offers a high reliability, the low resistive writing path performs high speed and energy-efficient write operation. We compare the SOT-MTJ performances metrics with the spin transfer torque (STT-MTJ). Based on accurate compact models, simulation results show an improvement which attains 20× in terms of write energy per bit cell. At the same writing current and supply voltage, the SOT-MTJ achieves a writing frequency 4× higher than the STT-MTJ.

Index Terms— Spin orbit torque, Spin transfer torque, MRAM, Spintronic, spin hall effect, three-terminal

I. INTRODUCTION

Spin transfer torque magnetic random access memory (STT-MRAM) [1] is a giant step toward a “universal memory” which could replace all conventional memory types while gathering their most merits; speed, high density, cost benefits, endurance and Non-Volatility. However, two main shortcomings are still limiting the reliability and endurance of STT-MRAMs; i) The high current density required for writing can occasionally damage the MTJ barrier, ii) It remains a challenge to fulfil a reliable reading without ever causing switching. Because writing and reading operations share the same path (through the junction), more constraints limit the designer to achieve high speed and reliable MRAM architectures. The SOT-MRAM is a promising alternative for the STT-MRAM. Thanks to its three-terminal architecture, authors in [2-5] claim that SOT-based devices can be built with independent reading and writing paths and so avoid challenges encountered with the state of the art of conventional STT-MRAMs, while keeping competitive switching currents. A thrilling debate is in progress between research groups inquiring about the exact origins of the SOT switching mechanism. It is still unobvious whether the Rashba effect has a significant role associated to the Spin Hall Effect SHE to achieve the switching [2-3] or it is only due to the SHE [4-5]. That’s why we use the abbreviation “SOT” to design this innovative device, since this term reveals the spin-orbit-torque responsible for switching with taking into account both phenomena, Rashba and SHE.

In this letter, we highlight the capability of the SOT device to design low energy and high speed MRAM architectures.

The work and results reported were obtained on the framework of the spOT project (grant agreement n°318144) funded by the European Commission under the Seventh Framework Programme. All authors are with SPINTEC Lab, CEA Grenoble, France (17 rue des Martyrs 38054 Grenoble Cedex 9).

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An example of a non volatile flip flop (NVFF) is studied. NVFF can provide a more efficient use of energy in systems on chips for standby-power-critical and quick-startup applications such as battery operated appliances and also improve performance of VLSI circuits [6]. Simulation results emphasize the improvement achieved with the SOT-MTJ when compared to the STT-MTJ. Both technologies considered in this letter are perpendicular magnetic anisotropy (PMA) materials-based. For simulation results, spice-like compact models -developed in Verilog-A language- have been used for each technology. Both STT and SOT compact models are developed in SPINTEC Lab according to the same magnetic assumptions.

II. SOT-MTJ STRUCTURE

A representative geometry of a 3-terminal memory cell with the perpendicular switching of the magnetized ferromagnetic layer using the SOT writing mechanism is shown in figure 1. Figures 1(b) and 1(c) represent the independent writing and reading paths, respectively. The structure consists of a free layer nanomagnet on the top of a writing stripe (metal electrode). For clarity reasons, we present only the main layers of the MTJ stack. Additional layers and materials combination could be considered to increase the robustness of the whole structure and mitigate undesirable effects (e.g. dipole fields around the free layers, etc). For instance, a more complex and complete structure has been proposed in [5]. The writing electrode materials existing in literature to fabricate the sample device are: β -Tantalum (β -Ta), β -Tungsten (β -W) or Pt [2-5]. The magnetic cell is written by applying a charge current via the write line. The orientation of the storage layer magnetization is controlled by the direction of the applied charge current. Positive currents (along +x) produce a spin injection current with transport direction (along +z) and spins pointing to +y direction. The injected spin current in-turn produces spin torque to align the magnet in the +y or -y direction. An external magnetic field is permanently applied to complete the switching operation. More details about the SOT-MTJ behavior are available in [2-5] [7-8].

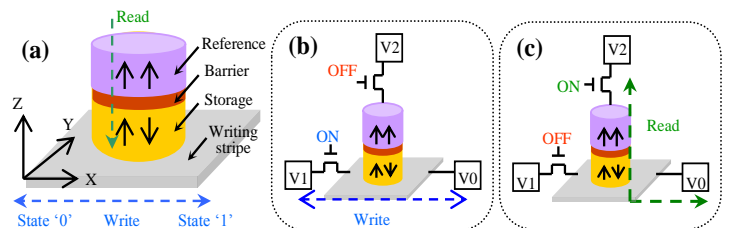


Fig. 1. (a) Schematic of the three-terminal SOT device and the two independent paths for (b) write and (c) read operations. In-plane current injection through the write line (writing stripe) induces the perpendicular switching of the storage layer.

III. SOT-MTJ MODELING AND SIMULATION

For the design of “hybrid CMOS” integrated circuits (ICs) including magnetic devices, it is important to use an accurate compact model of the SOT-MTJ. In [7], a compact model written in Verilog-A of a SOT device has been described and two writing schemes have been discussed in [8]. The model is developed under macrospin approximation and describes straightforward, high-speed and precise electrical representation of the physical behavior of the SOT-MTJ. Based on experiments and characterization of the device samples [2-3], a number of associated parameters were fed into these equations. The simulation parameters are listed in table I.

The model describes the memory cell as a three-terminal logic device and includes the dynamic behavior described by the Landau–Lifshitz–Gilbert model (LLG) given in equation (1) [9]. A special interest has been given to Rashba effect and SHE torques integrated in the effective magnetic field in equation (2) inside the LLG model to highlight the impact of these two factors on the dynamic of magnetization switching intensively argued in [2-5].

$$\frac{\partial \vec{m}}{\partial t} = -\frac{\gamma_0}{1+\alpha^2}(\vec{m} \times \vec{H}_{eff}) - \alpha \frac{\gamma_0}{1+\alpha^2} \vec{m} \times (\vec{m} \times \vec{H}_{eff}) \quad (1)$$

$\vec{H}_{eff} = \vec{H}_R + \vec{H}_{SHE} + \vec{H}_k + \vec{H}_a + \vec{H}_d$ (2), H_R is the Rashba field, H_{SHE} is the SHE field, H_k is the magnetocrystalline anisotropy field, H_a is the external bias magnetic field and H_d is the demagnetizing field. Expressions of each magnetic field are:

$$\vec{H}_R = C_R J_{app} \vec{y}, \quad H_{SHE} = -C_{SHE} J_{app} \vec{m} \times \vec{y}, \quad \vec{H}_k = \frac{2K_u}{\mu_0 M_s} m_z \vec{z}, \quad \vec{H}_a = H_a \vec{x},$$

$$\vec{H}_d = -M_s (n_{xx} \vec{m}_x + n_{yy} \vec{m}_y + n_{zz} \vec{m}_z)$$

To follow the variation of the SOT-MTJ resistance, Julière’s model [10] as well as Simmons’s model [11] were used in the expression describing the conductance through the junction. Moreover, for an improved accuracy, we integrated the dynamic conductance given by Brinkman model [12] and we took in consideration the dependence of magneto-resistance on bias voltage. By combining formulas given by these complementary models, we can assume that the total tunnelling conductance can be expressed according to the

TABLE I
DEVICE MODEL PARAMETERS

Parameter	SOT device	STT device
Permeability μ_0	$4\pi \times 10^{-7} \text{ H}\cdot\text{m}^{-1}$	$4\pi \times 10^{-7} \text{ H/m}$
Storage layer volume	$40 \times 40 \times 2 \text{ (nm}^3\text{)}$	$40 \times 40 \times 2 \text{ (nm}^3\text{)}$
Writing stripe :dimensions[5]	(100nm, 50nm, 2.5nm)	-
Resistivity(W, Ta, Pt) [5][13]	(200, 190, 20) $\mu\Omega\cdot\text{cm}$	-
SH angle (W, Ta, Pt) [5][13]	(0.3, 0.12, 0.08)	-
Sat. magnetization ,Ms	$1.1 \times 10^6 \text{ A/m}$	$1.1 \times 10^6 \text{ A/m}$
Bias magnetic field [3]	$H_a = 5 \times 10^{-3} / \mu_0$	-
Thermal stability factor	104	104
Parallel resistance R_P	$\sim 5 \text{ K}\Omega$	$\sim 5 \text{ K}\Omega$
Tmr0	100%	100%
CMOS technology/Vdd	40 nm / 1V	40 nm / 1V
Ic	60 μA (250ps)	60 μA (1ns)
V_{write}	1V	1V
Writing transistors width	220 nm	480 nm

equation(3):

$$g(V, m_x, m_z) = \frac{G_{P0}(1 - 2\beta V + 3\delta V^2)}{1 + \left(\frac{1 - (m_x \cos \theta_{mhl} + m_z \sin \theta_{mhl})}{2} \right)^2 \left(\frac{tmr_0}{1 + \frac{V^2}{V_h^2}} \right)} \quad (3)$$

Figure 2(a) describes the theoretical switching of the magnetization m_z from parallel ‘P’ to ‘AP’ and vice versa depending on the current direction applied during the time. Figure 2(b) shows the simulation results of the SOT-MTJ model which obviously corresponds to the theoretical behavior of the device and where we clearly observe the oscillations (from the LLG equations) during the switching (write phase).

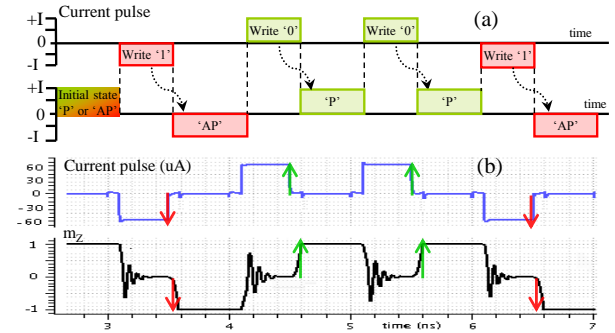


Fig. 2. SOT-MTJ model validation (a) Theoretical behavior (b) model behavior

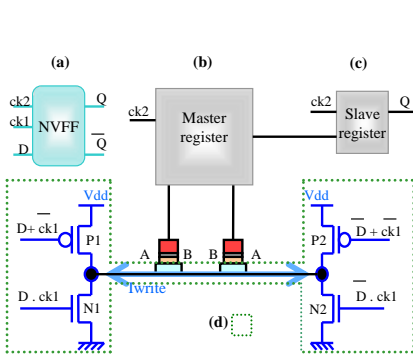


Fig. 3. NVFF structure (a) symbol, (b) master register architecture (c) slave register, (d) writing circuit

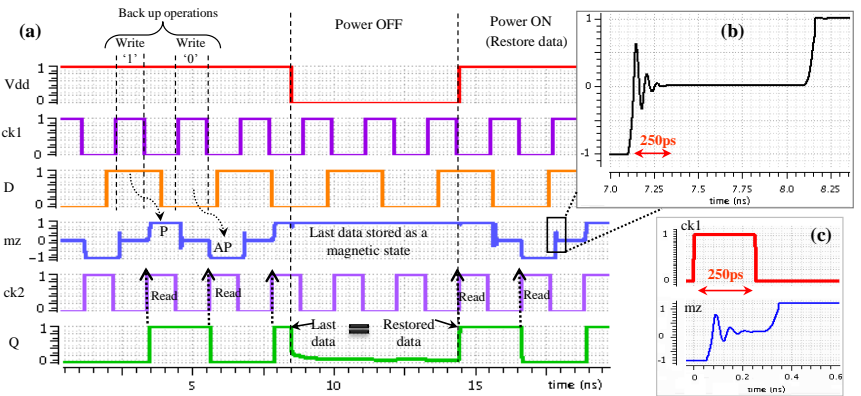


Fig. 4. NVMFF simulation results (a) store and restore operations (b) perpendicular magnetization ‘mz’ behavior of the SOT-MRAM during a current pulse of 1ns to switch from ‘AP’ ($m_z=-1$) to ‘P’ ($m_z=1$) (c) Switching with a 250ps pulse (exactly after oscillations stabilization)

IV. RESULTS AND DISCUSSION

In order to highlight the wide interest of using SOT-MRAM, we describe the integration of such device in the architecture of a non volatile magnetic flip flop (NVMFF). This flip flop can be used as a primitive cell into the ASIC design library allowing non volatility, high speed and low power. Figure 3 (a) shows the symbol of the NVMFF. The master register, shown in figure 3(b), is a conventional two-inverters-based non volatile latch based on the same structure in [14]. Its output is connected to the slave latch in figure 3(c). A non-overlapping two-phase clock [15] is used for the design of the NVMFF. The first phase ‘ck1’ is the writing phase which writes the input data ‘D’. It is correlated with the signal ‘D’ to write its value in the two SOT-MRAMs in a differential way; For instance, when P1 and N2 are ON, a path from V_{dd} to g_{nd} is created and the current flows from A to B for the 1st device and from B to A for the 2nd device. While the differential structure is achieved by placing two SOT devices side by side, it is possible to realize a differential structure by stacking them in the same manner in [13]. The second phase clock ‘ck2’ is the reading phase which reads the magnetic data stored during the writing phase. As shown in figure 4, the output value ‘Q’ of the slave register loads the magnetic data at each rising edge of the phase clock ‘ck2’.

Using the parameters in table I, the critical current required to write an STT-MRAM during a current pulse of 1ns is $I_C = 60\mu A$. Simulation results show that for the same I_C it is possible to write the SOT-MRAM with only a 250 ps current pulse. Figure 4(b) shows that after 250ps the magnetization m_z of the free layer gives up the oscillation phase and switching becomes possible. This is validated through simulations, as shown in figure 4(c). Thus, the SOT-MRAM is 4X faster than the STT-MRAM in term of possible writing speed.

In addition, the writing path of the SOT-MRAM is greatly less resistive than the STT-MRAM writing path (through the junction). For example, in our case the equivalent writing path resistance of the two differentials SOT-MRAM is $R_{eq}(SOT) = 2 \times 1.5 \text{ K}\Omega = 3 \text{ K}\Omega$, while for the STT-MRAM it is $R_{eq}(STT) = R_P + R_{AP} = 5 \text{ k}\Omega + 10 \text{ k}\Omega = 15 \text{ K}\Omega$. That’s why, to drive a writing current of $60\mu A$ through the STT-MRAM pair, we needed a 480 nm width for writing transistors compared to only 220 nm width in the case of the SOT-MRAM pair. Here, we suppose that we used the same transistor width for n and p type transistors of the writing circuits (figure 3(d)). Moreover, for a 1ns write time, the SOT-MRAM achieves write energy of 10.8 fJ, which is $5\times$ smaller than that of the STT-MRAM (54 fJ). Since it is possible to write during only 250ps, the write energy can attain a further improvement of $20\times$. These orders of magnitude are consistent with the predictive study of SOT-MRAM performance in [5]. More performance improvement can be attained with dimensional scaling thanks to a higher spin injection and a lower resistive write path. While, we run our simulation with a supply voltage of 1V, authors in [5] claim that at low voltage an improvement of more than $100\times$ can be achieved in term of energy-delay. In the case of the NVMFF, there is not any penalty in term of area when we use the SOT device instead of the STT. The writing operation is differential, so the two SOT-MTJs share the same write line and the ‘B’ terminal (figure 3.d) is common. Thus, the two SOT devices could be considered as two-terminal devices during the writing operation. However, in applications such as

TABLE II
TECHNOLOGIES COMPARISON

	SRAM	FeRAM	STT-MRAM	SOT-MRAM
Non volatility	No	Yes	Yes	Yes
Speed	Fastest	Medium	Fast	Very fast
Endurance	$>10^{15}$	$<10^{12}$	$>10^{15}$	$>10^{15}$
Density	Medium	High	High	High
Scalability	Good	Limited	Good	Good
Standby current	Low/high	Zero	Zero	Zero
Process compatibility	High	Low	High	High
Maturity	Product	Product	Advanced development	Early development

memory arrays, SOT based architecture could be less efficient in term of density because it requires more transistors to separate the reading and the writing operations. In table II, we give an overview about the SOT technology features compared to current technologies and the STT-MRAM.

V. CONCLUSION

We propose a NVMFF as a memory application of a three terminal SOT-MRAM where non volatility is achieved with an increased reliability thanks to a separated write/read paths. In addition, the write operation performs $4\times$ faster than the STT-MRAM with an improvement of $20\times$ in term of writing energy. Therefore, 3-terminal SOT-MRAM is suitable for high speed and low energy applications in addition to its intrinsic reliability and robustness.

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