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Abstract

This paper presents a parameter identification tool for SiC-MOSFET Spice models for the purposes of studying the impact of parameter's spread on series-connected devices. A SiC-MOSFET model available in literature is adapted. A set of 30 commercial SiC-MOSFETs is characterized. The extration tool is used to generate Spice model file for each device, which are validated by comparison to double pulse measurement results. Generated SiC-MOSFET models are employed to perform simulation of switches made of two series-connected devices. The simulation results reveal that a difference of almost 0.2 V in V_{TH} produces 21 % of V_{DS} voltage unbalance during turn-off.

1 Introduction

In the context of developing converters in the range of MW for grid applications with voltage ratings up to tens of kV, SiC-MOSFETs are considered as a promising option. Since 10 kV SiC-MOSFET are not yet commercially available, series-connection of available 1.7 kV SiC ones is a sensible approach [1], [2]. The main issue faced by series connected devices is voltage unbalancing between components which can cause damage in case of over-voltage. Several causes have been identified in literature: a delay mismatch of gate-drivers and a difference in threshold voltage produce the behavior represented in Figure 1 (a). In addition, common mode current paths [3] inherent to layout and gate driver isolation along with components characteristics spread result in modulation of voltage switching speed between devices. This leads to voltage unbalancing as represented in Figure 1 (b). Furthermore, in the case of high switching speed, voltage balancing is highly sensitive to those imperfections.

Numerical transient simulations are necessary to evaluate the impact of parameters mismatches first before making real prototypes in order to save time and reduce costs. Many different SiC MOSFET's models exist in the literature and parameters extraction platforms for series connected devices [4] have been proposed based on McNutt/Hefner model [5]. The main objective of this paper is to provide a tool that can carry out quick parameters extractions corresponding to each MOSFET based on static and capacitance characteristics for the purpose of supporting the design of the series connection. In order to do so, 30 commercial devices are characterized to have a realistic representation of the parameter's

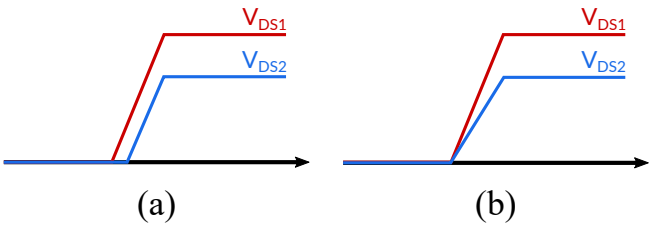

Fig. 1: Unbalanced voltage at turn OFF due to (a) an activation delay and (b) due to different voltage rising speed.

spread. Afterwards a model is adapted to accurately simulate the electrical behavior. The obtained model is validated through double pulse tests by comparing simulation and measurement results. Thanks to theses models, numerical simulations are provided with series-connected SiC-MOSFETs to compare the impact of different parameters spread on the voltage balancing performances.

2 SiC MOSFETs characterization

To obtain an accurate model for each component, the electrical characteristics are individually measured. Devices used in this paper are SiC-MOSFETs manufactured by Wolfspeed, which are 1.7 kV - 72 A with 45 mΩ ON state resistance (C2M0045170P). A total of 30 devices have been characterized to obtain a representative sample of components. A B1506A curve plotter coupled with a N1265A Ultra High Current Unit from Keysight is used to obtain static characteristics and capacitance curves at ambient temperature. A custom-build PCB (Fig. 2) is used to measure 4 pin TO-247-4 packaged devices. Calibration is done taking care that the wires are in a fixed position.

Fig. 2: Connection on the B1506A of a custom-built board for TO-247-4 packages

Figure 3 gives the threshold voltage (V_{TH}) spread which influences the switching timing, the spread of the leakage current at 1.7 kV which causes static OFF-state voltage unbalance and also the spread of the parasitic capacitances which defines the dynamic behavior. V_{TH} measurement preconditioning procedure proposed in [6] is used to ensure repeatably. In a first approach, we can observe a dispersion of these parameters for which the average values correspond to the data-sheet information. In a second step, we are going to investigate impacts of these disparities on the voltage balancing performances in case of series-connected devices.

To conclude on the importance of the parametric dispersion, electrical simulations are required. In order to obtain correct results, an electrical model of SiC-MOSFET that properly fits the behavior of the devices must be chosen. The parameters of this model must be adjusted so that the static and capacitive behavior corresponds to each one of the 30 MOSFETs. The parameters have to be extracted from the I_D-V_{GS} curves. I_D-V_{DS} is obtained at V_{DS}=5 V, 10 V, 15 V and 20 V and the I_D-V_{GS} is measured with V_{DS}=20 V. Pulsed measurements are employed to avoid DUT self-heating. The presence of a protective resistance (150 mΩ) on B1506A device, gives a different result regarding the I_d-V_{GS} curve. This resistance value has to be considered when model curves are fit into these measured curves. Input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitance are also measured up to 1000V of V_{DS} at 100 kHz.

3 Model parameter identification

3.1 SiC-MOSFET model

The tool presented in this paper is coded in Python language and is designed to work with many MOSFET models. In this paper a temperature dependent SPICE model for SiC MOSFET with technology-dependents parameters [7] is adapted. The chosen model is based on level 1 SPICE model of MOSFET and channel/drift regions are accurately modeled in and out of the safe operation area (SOA). The following work is restricted to the SOA and room temperature, but could be extended in future studies. The simplified model is implemented in LTSpice™ as shown in Figure 4.

At the core of the model the SPICE MOSFET level 1 model can be found. The Equation (1) is the simplified level 1 SPICE model that is implemented with Python language.

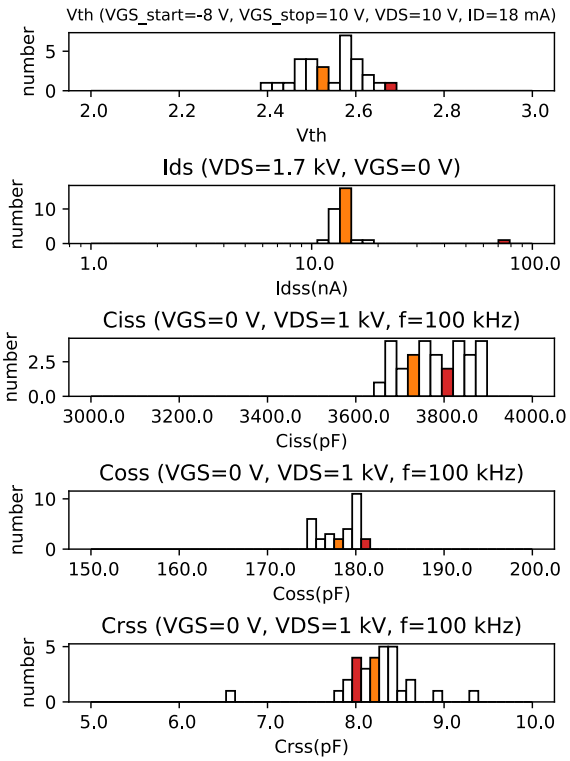

Fig. 3: Dispersion of key parameters in a series of 30 MOSFETs characterized under the same conditions.Colors highlight two distinct MOSFETs.

$$I_{M1} = \begin{cases} 0 & \text{for } V_{G_1S} < V_{TH} \\ K_p \cdot & \left((V_{G_1S} - V_{TH}) \cdot V_{D_1S} - \frac{1}{2} V_{D_1S}^2\right) \\ & \text{for } V_{D_1S} <= (V_{G_1S} - V_{TH}) \\ \frac{1}{2} K_p \cdot & (V_{G_1S} - V_{TH})^2 \\ & \text{for } V_{D_1S} > (V_{G_1S} - V_{TH}) \end{cases} \quad (1)$$

The I_{MOS} equation Eq. (2) expresses the current of the M_1 MOSFET.

$$I_{MOS} = \frac{I_{M1}}{\left[1 + \theta_1 \cdot (V_{G'S} - V_{TH0})\right](1 + \theta_2 \cdot V_{D_2S})}(1 + \lambda \cdot V_{D_2S}) \quad (2)$$

The voltage V_{D_1S} of the MOSFET is the image of V_{D_2S} weighted by the coefficient K_F. This structure will allow us in a future study to add the avalanche and bipolar effects as described in [7] . Equation (3) and Equation (4) allow to precisely model the variation of the resistance of the accumulation and JFET zone.

$$R_D(V_{G'S}, V_{drift}) = R_{AJ}(V_{G'S}, V_{drift}) + R_{EPI} \quad (3)$$

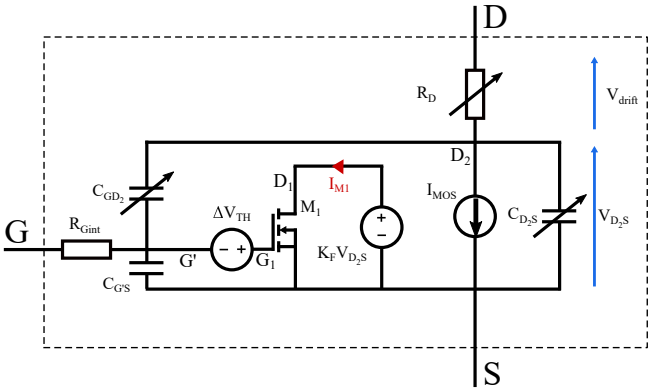

Fig. 4: Sub-circuit implemented in LTspice to modelled the behaviour in SOA

$$R_{AJ}(V_{G'S}, V_{drift}) = \frac{V_{drift}}{V_1 + V_{drift}} \left[R_{AJ10} + R_{AJ20} \cdot \left(1 + \frac{V_{G'S}}{V_2}\right)^{-\eta}\right] \quad (4)$$

MOSFET capacitances are mainly responsible of the dynamic behavior. Since their values are dependent on the V_{ds} voltage, it is essential to properly model this dependency. $C_{G'S}$ is considered as constant. Gate-to-drain capacitance C_{GD2}, which is connected between the gate and I_{MOS} current source (Fig. 4), is the most crucial because it forms a feedback loop between input and output. The following Equation (5) is therefore used to model the $C_{G'D_2}$ variation as a function of voltage. $C_{G'D_20}$ is the value at zero voltage and $C_{G'D_2MIN}$ is the minimum value at high voltage. Drain-to-source C_{D_2S}, which is connected on I_{MOS} current source, is modeled by Equation (6).

$$C_{G'D_2} = (C_{G'D_20} - C_{G'D_2MIN}) \cdot \left(1 + \frac{V_{G'D_2}}{V^*_{G'D_2}}\right)^{-0.5} + C_{G'D_2MIN} \quad (5)$$

$$C_{D_2S} = (C_{D_2S0} - C_{D_2SMIN}) \cdot \left(1 + \frac{V_{D_2S}}{V^*_{D_2S}}\right)^{-0.5} + C_{D_2SMIN} \quad (6)$$

It should be noted that the model is completed with the parasitic inductive elements of the TO247-4 package. Since it is not possible to measure it, values are retrieved from the Wolfspeed model [8].

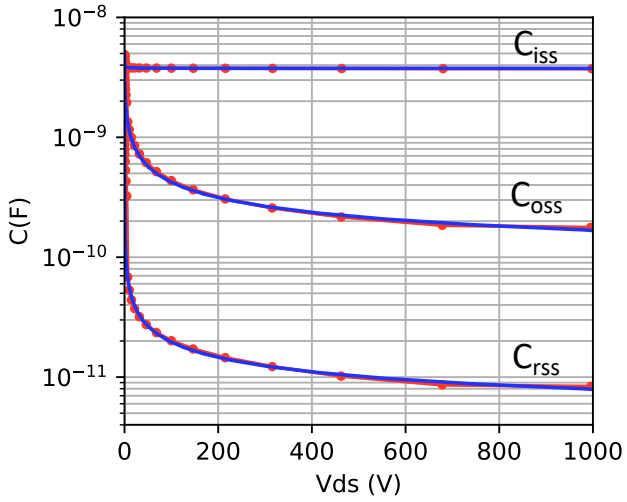

Fig. 5: Measured MOSFET capacitances up to V_{ds} = 1 kV (red) and model (blue)

3.2 Parameter identification

A strategy to identify the model parameters that match each component in our possession is presented in this section.

The objective is to fit the I_d-V_{DS} and I_d-V_{GS} curves of the model on the measurements. One of the possibilities is to use a circuit simulation software. LTspice™ or PSpice™ for the Aalborg University platform [4] can be used. The advantage is to be able to simulate the whole model with all its parasitic elements. Nevertheless, it is required to run the simulation numerous times by varying the model parameters. Each simulation takes about ten seconds. Which limits us in the number of optimization algorithm iterations to stay within a reasonable time. Knowing that the algorithm aims to be executed for each component, another approach is considered. Since we are concerned with only fitting the static characteristics and capacitance, we can dispense with using simulation software and the curves can be calculated directly using the equations of the model coded in Python language and calculated thanks to different libraries. Such computations will be considerably faster and will make it possible to compare hundreds of combinations of parameters in a around one minute.

To achieve this, equations have to be written in a "function format" into Python language so the system of equations can be solved with fslove() function of the SciPy library. The system of equations Equation (7) is formed by Eq. (3) and Eq. (2) and is solved to obtain i_D as a function of V_{DS} and V_{GS}. Current values have to be calculated in the same conditions as the measurement ones.

$$\begin{cases} 0 = R_D(V_{G'S}, V_{drift}) \cdot i_D - V_{drift} \\ 0 = I_{MOS} \cdot (V_{G'S}, V_{D_2S}) - i_D \end{cases}$$
$$\text{where } V_{drift} = V_{DS} - V_{D_2S} \tag{7}$$

Once the equations are coded in Python, an optimization algorithm is set up to identify the parameters of the model that match the static measurements. The objective cost function is based on the weighted sum of square errors. Those errors are calculated as the mean absolute error between model and experimental data.

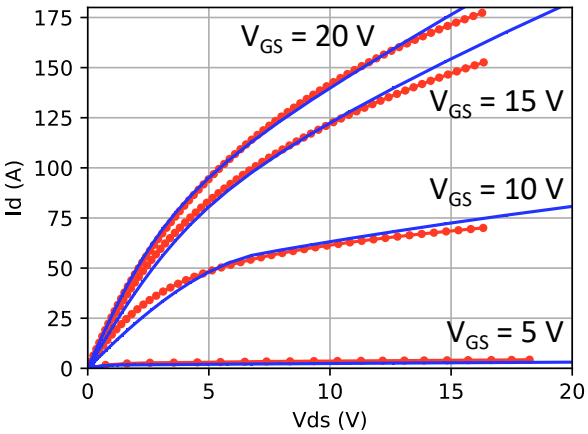

Fig. 6: I_d-V_{ds} at T_j=300 K model (blue) measure (red)

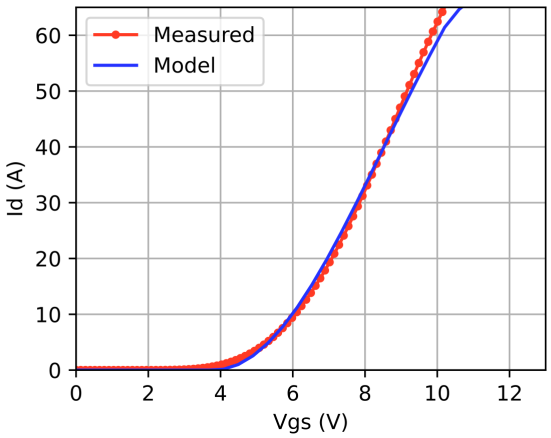

Fig. 7: I_d-V_{gs} at T_j=300 K model (blue) measure (red)

LMFIT interface to non-linear optimization and

curve fitting problems for Python enables us to try out multiple minimization strategies adapted to equations. The Nelder-Mead simplex algorithm is used since it is efficient for the search of unconstrained parameters. The search for parameters can be split into two steps to accelerate the convergence of the algorithm. The first one, to find the Kp, V_{TH} and λ parameters by minimizing the I_D-V_{GS} error. The second, to find R_{EPI0}, R_{AJ10}, R_{AJ20}, V_1, V_2, η by minimizing the I_D-V_{DS} error. This task takes less than 1 min on 2.6 GHz Intel core i5 processor. Once the parameters are calculated from the identification process, Spice-like files models are generated and can be run into LTspice™ software.

Figure 6 and Figure 7 present the curves of the model that precisely fit the measurements from the curve tracer , which are plotted with dotted red lines. The parameters of this model are given in the Table 1. The initial values given to the algorithm are on the left column and the optimized values are on the right column. These same initial values are used to fit all characterized components.

Tab. 1: Extracted parameters

Parameter	Initial values	Identified	Unit
Kp	4	2.497	A/V^2
Vth	4	3.834	V
λ	10	6.376	mV^{-1}
θ_1	10	6.151	mV^{-1}
θ_2	10	14	mV^{-1}
R_{EPI0}	7.7	8.1	$m\Omega$
R_{AJ10}	0.18	0.10	Ω
R_{AJ20}	0.57	0.14	Ω
V_1	0.30	12.66	V
V_2	0.074	7.41	V
η	1.80	1.8	
K_F	0.87	0.99	
$C_{G'S}$	3.05	3.74	nF
$C_{G'D_20}$	2	2.6	nF
$C_{G'D_2MIN}$	10	4.54	pF
$V^*_{G'D_2}$	10	14.86	mV
C_{D_2S0}	2	1.7	nF
C_{D_2SMIN}	60	95.98	pF
$V^*_{D_2S}$	10	1.983	V

Values of the capacitances are identified separately from the other model parameters. The constant value of $C_{G'S}$ is considered to be the measured value of C_{rss} at 1000 V. Parameters of Equation (5) and Equation (6) are identified thanks to SciPy library to fit C_{iss} and C_{oss} measures (Fig. 5) for V_{DS} above 25V.

4 Dynamic model validation

To validate the proposed identification methodology and tool, a double pulse test bench is build. The switching behavior of one of the characterized SiC-MOSFET is evaluated in a circuit (schematic on Fig. 8 and realization on Fig. 9) consisting of a SiC Schottky diode (C3D25170H) as freewheeling diode, an inductive load of 160 μ H and a DC bus designed on PCB with 44 μF of film capacitors. To simulate the circuit, the corresponding diode model provided by CREE is used [8].

Tests are performed at 1 kV bus voltage and current up to 60 A. Gate driver is optically isolated and is made of a integrated push-pull circuit. This driver is able to apply 20 V and –5 V thanks adjustable voltage regulators. The external gate resistor is set to 6.7 Ω. Considering the length of the gate trace, a small stray inductance of 2 nH is added into the simulation. Voltage measurement are performed thanks to a passive probe Textronix (TPP0850) and the DUT current is measured with a Rogowski coil current sensor (CWT6R from PEM).

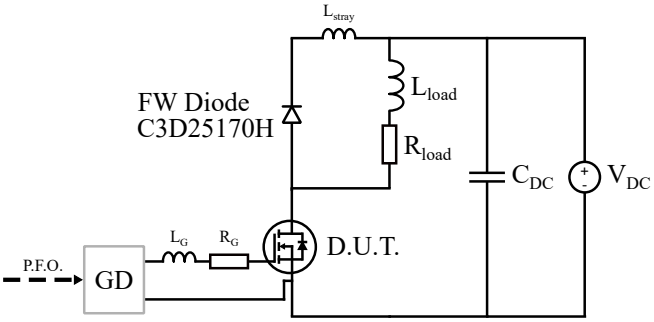

Fig. 8: Double pulse test platform for model validation.

Experimental measures and time-simulation are plotted on the Figure 10 showing the first turn OFF after load inductor current reaches 60 A and the following turn ON switching. The switching speed being very high, the slightest parametric variation lead to a strong variation on the voltages and currents. Here the measured switching speed

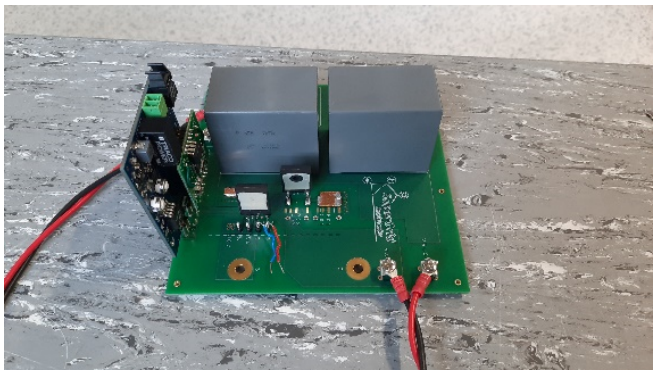

Fig. 9: Double pulse test platform for model validation.

is 60 V/ns and the simulation gives 87 V/ns at turn OFF. This difference can be explained by the absence of some parasitic elements in the simulation. The current waveform in the simulation seem to not accurately fit the measurement, however it should be noted that the Rogowski coil current sensor has a limited bandwidth of 16 MHz that filters out high frequency oscillations. Finally, the simulation results match well enough the switching behavior in order to study the voltage balancing of series connected SiC-MOSFETs.

5 Simulation of series connected MOSFETs

The goal of this section is to demonstrate the need for a MOSFET parameter identification tool. Since the whole series of MOSFETs has been characterized, it is possible to select similar or different components in order to observe the impact of parameter's spread on the V_{DS} voltage balancing. For this simulation two components are connected in series as shown in Figure 11. The configuration is similar to the previous setup. The bus voltage is increased to 2000 V. Each MOSFETs withstands 1000 V when the voltages are balanced. This choice ensures that the voltages are not clamped by the MOSFET breakdown voltage even in case of severe unbalance. Since the voltage is doubled, the value of the inductance is also doubled in order to obtain the same switching current 60 A, L_{load} = 320 μH. The stray inductance is arbitrarily increased to 55 μH since the series connection necessarily increases the layout dimensions. Static balancing resistors of 100 kΩ are added so that the voltages are balanced when MOSFETs are turned ON.

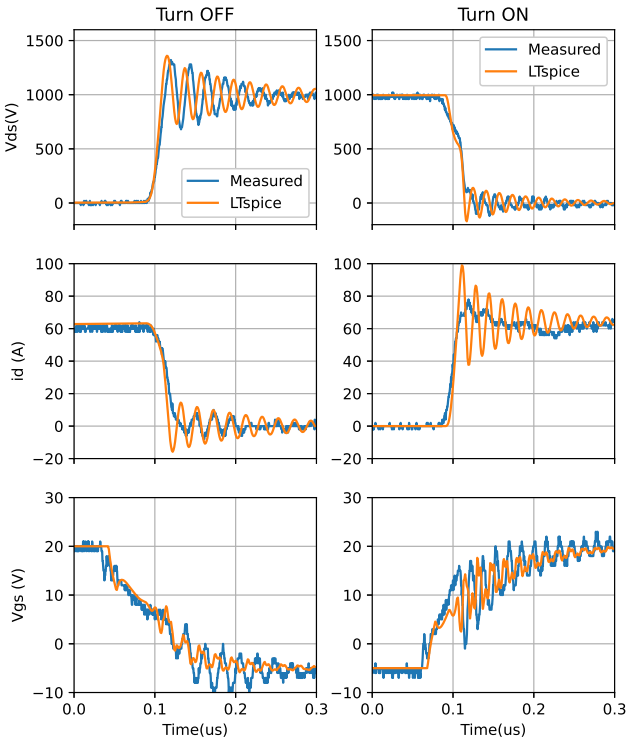

Fig. 10: Double pulse test platform for model validation (C_{bus}=44 μF, L_{load} =160 μH, current of 60 A, T_j = 300 K) – V_{ds} at turn OFF switch.

For this demonstration three cases are compared. First a double pulse test is performed with two similar MOSFETs. In Figure 3 their characteristics are highlighted in orange color. The two corresponding models are obtained using the tool and integrated in the LTspice™ simulation. The unbalance percentage is calculated as described in the Equation (8) and the table 2 sum up results of three different cases. In this first case with similar MOSFETs an unbalance value of 1.4% is obtained. As expected the voltages are well balanced.

$$\text{Unbalance} = \frac{\frac{V_{DC}}{N} - V_{DSOFF_i}}{\frac{V_{DC}}{N}} \cdot 100\% \quad (8)$$

Where : N is the number of MOSFET

V_{DSOFF_i} is V_{DS} at OFF state of i^{th} MOSFET

Then the M2 MOSFET is replaced by a MOSFET model which has the most different characteristics within the set (highlighted in red in the Figure 3). The unbalance obtained in simulation is 21%. Figure 12 shows the unbalance of the V_{ds} voltages between the two MOSFETs. It can be seen that the

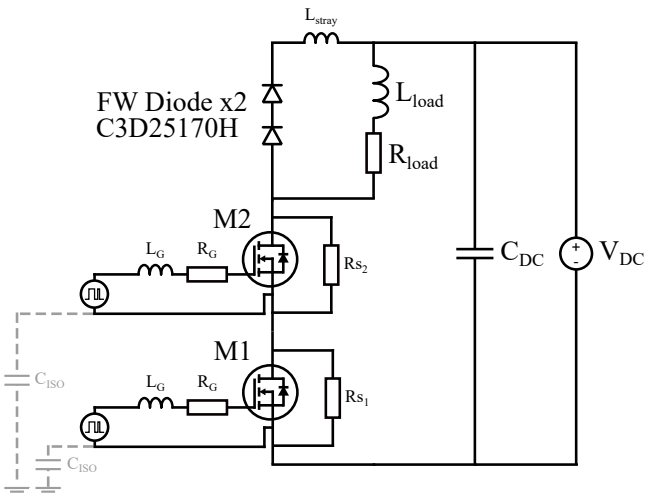

Fig. 11: Double pulse simulation test platform for simulation of 2 MOSFETs series connected

Tab. 2: Impact of MOSFET on balancing

case	M1 and M2	C_{ISO}	unbalance
1	Similar	no	$\pm$ 1.4%
2	Very different	no	$\pm$ 21%
3	Similar	20 pF	$\pm$ 7.5%

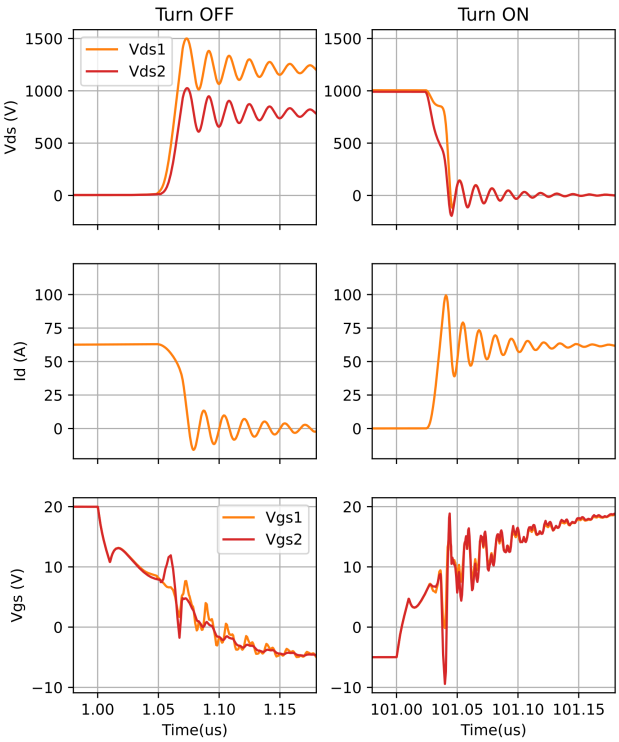

Fig. 12: Simulation of 2 MOSFETs series connected

MOSFET with the higher V_{TH} switches later. The switching speeds are also different.

This simulation gives the ability to compare the impact of SiC-MOSFET parametric spread in comparison to other causes of imbalance. For example the impact of the parasitic capacitance of isolated gate driver power supplies. In the simulation a capacitance has been added to each gate driver and the ground. In this situation an unbalance of 7.5% is obtained.

6 Conclusion and Perspectives

A model parameter identification tool is deployed in order to quantify the impact of the parameter spread of series connected SIC-MOSFETs. It is possible to generate the models corresponding to the numerous components characterized in a reasonable time. The results obtained with the 1.7 kV - 45 mΩ components demonstrates a sufficient accuracy to model the electrical behavior. The first simulation results of series connection are promising for the continuation of the studies. Many situations will be possible to study. Furthermore, these models will allow us the design of a high-performance balancing solutions.

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