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Design of a Novel Hybrid CMOS Non-Volatile SRAM Memory in 130nm RRAM Technology

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Abstract— Static Random-Access Memories (SRAMs) are an integral part of the chip industry, occupying a noticeable share of the memory market due to their high performance and compatibility with CMOS technology. Traditional SRAMs lack the capability to retain data after power-off, restricting their availability in applications such as battery-powered mobile devices where non-volatility associated with zero-leakage currents is needed. This paper presents a novel Non-Volatile SRAMs (NVSRAMs) device based on Resistive RAM (RRAM) technology. A comparison between SRAM and NVSRAM performances is proposed at both cell and memory array level. The comparison covers several metrics such as power consumption, area and design complexity. The presented circuits are implemented in a 130-nm high voltage CMOS technology from STMicroelectronics.

Index Terms— Static Random-Access Memories (SRAMs), Non-Volatile SRAM (NVSRAM), Resistive RAM (RRAM), Power Consumption.

I. INTRODUCTION

For modern high-performance technologies, the memory subsystem directly affects the performance of computing systems [1]. The memory subsystem includes Static Random-Access Memory (SRAM), Dynamic Random-Access Memory (DRAM), and Flash memories. All these memories are charge-based. In SRAM, the data is stored as charges at the nodes of the cross-coupled inverters [2,3]. Static random-access memory (SRAM) has been widely used in the memory market. This rapid growth is backed by SRAM appealing characteristics, including fast operations and low power consumption in standby mode [4]. Moreover, SRAM cell uses the same fabrication process as logic, thus no extra cost is needed. These properties are unique for SRAM when compared to other memories such as DRAM or Flash memories. However, lowering of supply and threshold voltages leads to a degradation in SRAM cell performances with an increase of leakage currents in the standby mode [5].

Power supply reduction and the down scaling in CMOS technology have been the main trends driving the rapid growth of emerging memories, such as Ferroelectric RAM (FeRAM) [6], Spin Torque Transfer RAM (STT-RAM) [7], Phase-change RAM (PCRAM) [8], Conductive Bridge RAM (CBRAM) and Oxide based-RAM Memories (OxRAMs) [9] [10]. In this regard, SRAM technology faces new challenges as the increase of its leakage currents, results in a

considerable increase of power consumption not compatible with battery-powered applications [11]. To overcome these issues, RRAM is considered as a promising solution that can elevate SRAMs to the next level in memory technologies [12]. Due to its relatively small access latency, high density and analog feature [13,14], ReRAM is considered as a promising candidate for designing neuromorphic applications [15] and non-volatile logic gate [16] and novel SRAM architectures [17,18] beyond storage applications. Hybrid Non-Volatile SRAM (NVSRAM) based on emerging memories are expected to replace traditional SRAM in SoC applications [19]. Smart cards and microcontrollers (MCU) will likely adopt new resistive switching memories as a substitute to conventional memories [20]. In this paper, conventional SRAM and novel Non-Volatile SRAM (NVSRAM) memory cells implemented in a 130-nm high voltage CMOS technology from STMicroelectronics [21] are presented and compared at cell and memory array level.

In section II, the traditional SRAM cell and the proposed NVSRAM memory cell are presented. In section III, memory arrays designs based on elementary SRAM and NVSRAM cells associated with all peripheral circuits are proposed. In Section IV, SRAM and NVSRAM performances are compared based on electrical simulations. Section V presents some concluding remarks.

II. CELL LEVEL : SRAM & NVSRAM

The combination of SRAM and RRAM technology forms a new hybrid structure called Non-Volatile SRAM (NVSRAM). The proposed NVSRAM cell is designed to be electrically stable at the low supply voltages. To design the NVSRAM, SRAM data nodes are connected to an OxRAM resistive element allowing data backup operations in standby or power-off mode while SRAM normal mode operation is preserved (i.e. HOLD, WRITE and READ operations).

A. OxRAM technology

An OxRAM device consists of three layers including two metal electrodes, and an insulator layer [22]. OxRAM is based on a structure known as a Metal-Insulator-Metal (MIM) as shown in Fig. 1(a). This structure can be integrated in the Back End Of Line (BEOL) of CMOS technology as depicted in Fig. 1(b), presenting important advantages in term of area and data transfer latency.

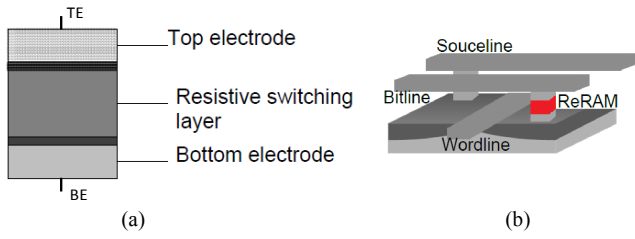


Fig. 1. (a) Basic RRAM structure and (b) its integration in the BEOL

Fig. 2 (a) and (b) show OxRAM I-V characteristics in linear and logarithmic scale respectively, extracted from actual OxRAM devices [23]. The first step in the OxRAM programming operation is FORMING where a high voltage is applied across the memory cell to switch the cell from HRS (high resistive state) to LRS (low resistive state). FORMING operation is performed once in the OxRAM device life. After FORMING, SET and RESET operations are executed by applying specific voltage on the electrodes of OxRAM cell (i.e. V_{SET} and V_{RESET}) [24]. Based on the linear curve presented in Fig. 2 (a), the V_{SET} value needed to switch to LRS state is equal to 0.57 V, while the V_{RESET} value required to switch back to HRS state is equal to -0.7 V [25]. Note that log curve is the classical representation of the OxRAM I-V hysteresis as it amplifies low current values.

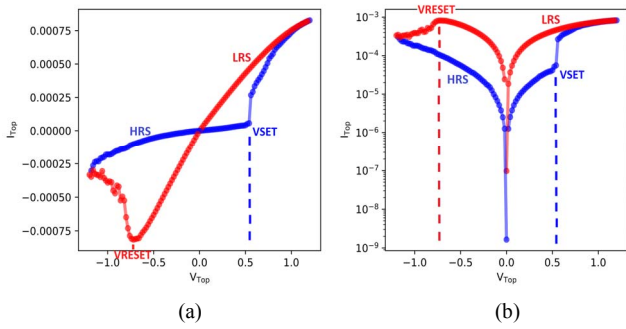


Fig. 2. I-V characteristic of the OxRAM model in (a) linear and (b) log scale

B. 6T SRAM memory cell

SRAM structure is built on the cross coupled inverters structure presented in Fig.2. In SRAM memory cell, HOLD, READ and WRITE are the main operations executed through Word Lines (WLs) and Bit Lines (BLs). Each SRAM cell has the capability of storing “0” or “1”. WLs are connected to the gates of the select transistors (M5 and M4), and BLs are connected to the transistors’ terminals. BLs are disconnected from the SRAM core during HOLD stage by deactivating the WLs. Data is retained in the latch structure on data nodes Q and Q_b [26]. READ and WRITE operations are completed by activating WL to sense or update the stored data respectively. Fig. 3 shows the 6T SRAM cell layout with an area occupancy equals to $34 \mu\text{m}^2$.

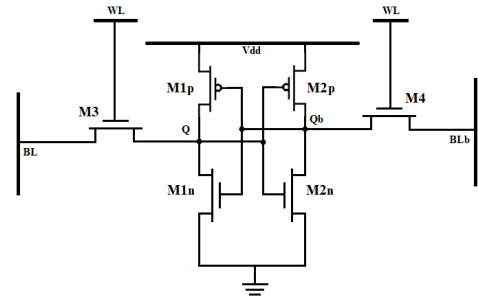


Fig. 2. 6T SRAM cell

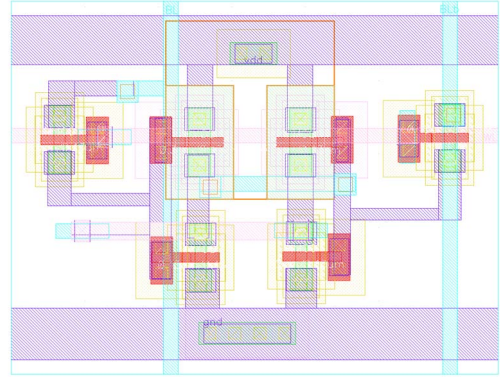


Fig. 3. 6T SRAM Cell layout

C. 8T1R NVSRAM memory cell

Fig. 4 depicts the proposed 8T1R structure. This novel cell has a minimal number of control signals compared to state of the art NVSRAMs [27-29]. The OxRAM device [30] is connected to M5 transistor (TE) and to the node Q_b (BE). M3 and M4 are the conventional access transistors and M5 and M6 are additional transistors used for the non-volatile storage operations referred to as STORE and RESTORE. STORE consists in two operations: SET and RESET. SET stores ‘1’ and RESET stores ‘0’ in the OxRAM device.

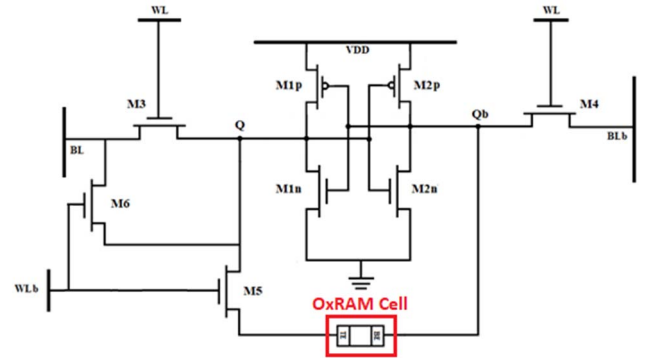


Fig. 4. 8T1R NVSRAM Cell

During FORMING, BL and WL_b are set high, WL and BL_b are set low. During this stage, the OxRAM can be formed in one step (M6 is ON: direct connection between BL and the OxRAM). BL is set to 5 V while BL_b is grounded and the access transistors (M5 and M6) are activated by applying a pulse on WL_b . STORE operation is preceded by a WRITE

operation. During WRITE “0” operation, BL and WL_b are set low, WL and BL_b are set high. RESET is the next stage after WRITE “0”, where WL and BL are set low.

In Precharge stage, BL and BL_b are precharged to $V_{DD}/2$ (0.9V). In general, READ operation is executed through WL which is set high. After STORE (SET/RESET) and READ operations, all the signals are turned OFF including V_{DD} . RESTORE operation is required to retain the data after the power is down. RESTORE is performed by enabling V_{DD} , and WL_b is set high. All other signals are kept low. Precharge and READ after RESTORE follow the conventional operation, where WL is set high and WL_b is set low. Fig. 5 shows the 8T1R NVSRAM cell layout with an area occupancy equals to $53 \mu\text{m}^2$.

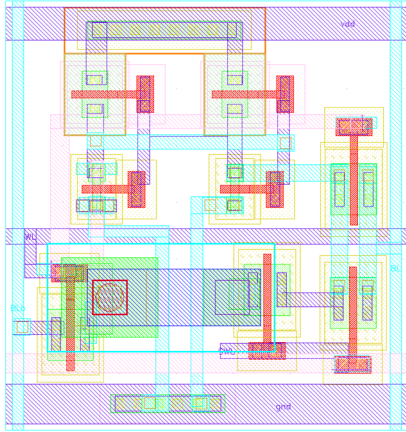


Fig. 5. 8T1R NVSRAM Cell layout

III. MEMORY ARRAY LEVEL

In this section, a conventional SRAM memory array is tested and compared with the proposed NVSRAM array structure. The peripheral circuits used in both structures are similar but some additional blocks are required for the NVSRAM array for proper operation (logic circuits) to assure the stability of the programming operations.

A. SRAM Array Design

SRAM array consists of multiple SRAM cells arranged to share connections in horizontal rows and vertical columns. In this regard, an elementary 4x8 bytes memory array is proposed with a total size of 256 cells. The horizontal lines are the WLs, while the vertical lines along which data flow into and out of cells are the BLs. A cell is accessed for reading or writing by selecting its row and column [31]. To be fully functional, the memory array has to be associated with additional circuits as illustrated in Fig. 6. A word decoder selects one WL based on the selected address. Column decoder circuits consist in numerous peripheral circuits including precharge circuits, column multiplexers, sense amplifiers and write amplifiers. Circuits delivering the logic levels are located at the edge of the BLs (write and sense amplifiers). The BLs are connected to the output of the precharge circuits as well as the write drivers and to the sense amplifiers used to complete WRITE and READ operations.

Note that the data inputs are fed directly to the write drivers to perform WRITE operations. The WLs are controlled by the row decoder to activate the access transistors and the enable the selected cells. The column decoder is used to select a group of columns, where the programming operations are executed. The column multiplexer role is to connect the sense amplifier to the BLs and disconnect the precharge and write circuit drivers to insure that READ operation is completed properly. Hence, READ operation is initiated by addressing a specific word when SE signal is activated. Before reading, the precharge circuit increases the BL voltage to V_{DD} or $V_{DD}/2$. READ operation is finalized by turning off the WL [32-33].

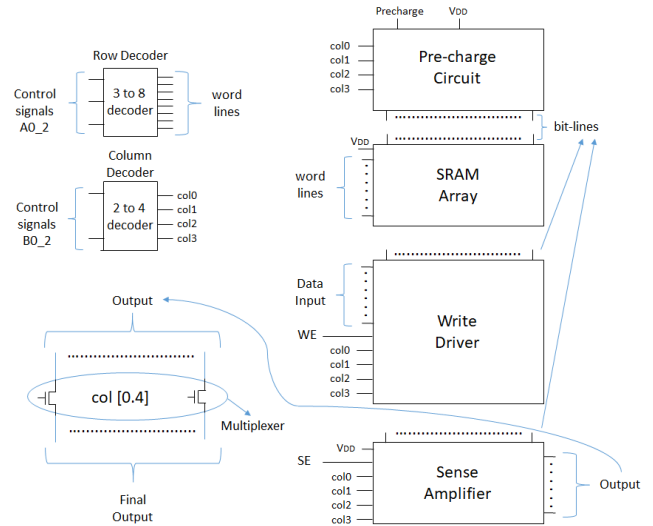


Fig. 6. SRAM Array Design

B. NVSRAM Array Design with Novel 8T1R Cell

The proposed NVSRAM array structure follows the proposed 8T1R cell presented in Fig. 4 which is the core cell of the memory array. The design includes all the peripheral circuits associated with a classical memory array with some marginal modifications as illustrated in Fig. 7.

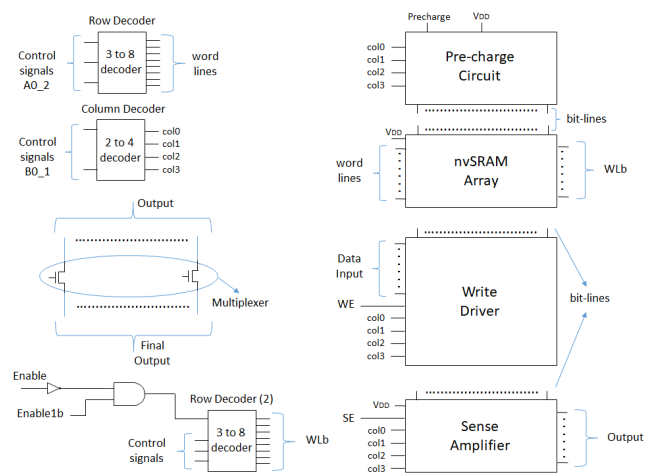


Fig. 7. NVSRAM Array Design

The NVSRAM array has additional logic circuits to handle the STORE (SET & RESET), and RESTORE operations that follows a power-off or standby operation. Note that, WL_b has its own decoder to have a direct control over the STORE operations.

IV. SIMULATION RESULTS AND COMPARISON

SRAM and 8T1R NVSRAM arrays simulations results are proposed in this section. Voltage pulses levels are set to be compliant with the available voltage supply V_{DD} (1.8V and 3.3V).

A. SRAM memory cell simulation results

Fig. 8 presents the timing waveforms obtained after the simulation of the SRAM array. During Precharge, the precharge circuit is enabled (Precharge signal is “0”) since the select transistor in the Precharge circuit is a PMOS and write drivers (WE) and sense amplifiers (SE) that are kept OFF. The row decoder (ENABLE) is also kept off as memory cells are not selected in this stage. The column decoder (ENABLE2) is turned ON to select the BLs that should be precharged. During WRITE, precharge circuits is disabled (Precharge SET high), and sense amplifier circuits are still kept OFF (SE “0”). Write driver is turned ON (WE “1”), and the row decoder is enabled (ENABLE “1”) to access the cells. The column decoder is kept ON (ENABLE2 “1”) to allow the precharged BLs to feed the addressed cells. During HOLD state, all the signals are OFF (except V_{DD}) in order to maintain the data inside the cross coupled inverters. The next stage is Precharge before READ, where the same conditions are used as the Precharge before WRITE. During READ, precharge circuit is disabled, and write driver circuit is turned OFF. The column decoder is kept ON (ENABLE2 “1”) allowing the BL sensing path to reach the selected sense amplifiers. The output out “0” is the result of WRITE “0” operation, where out “1” is the result of WRITE “1” operation in another SRAM cell.

Fig. 9 presents the transient simulations results of the decoders. A0 and A1 signals of the row decoder are set high, thus WL3 is selected. For the column decoder, B0 is high and B1 is low, thus col1 is selected.

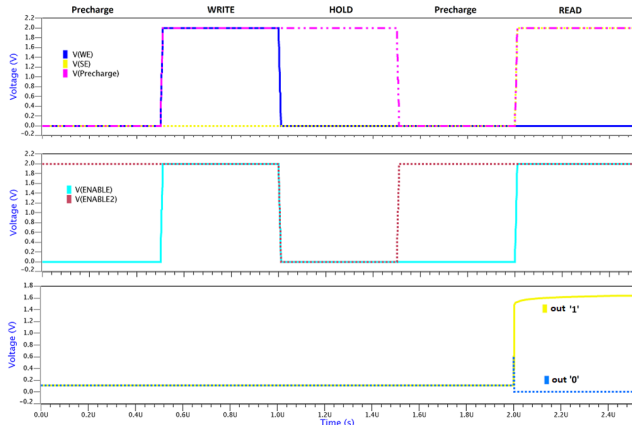


Fig. 8. SRAM array timing waveforms

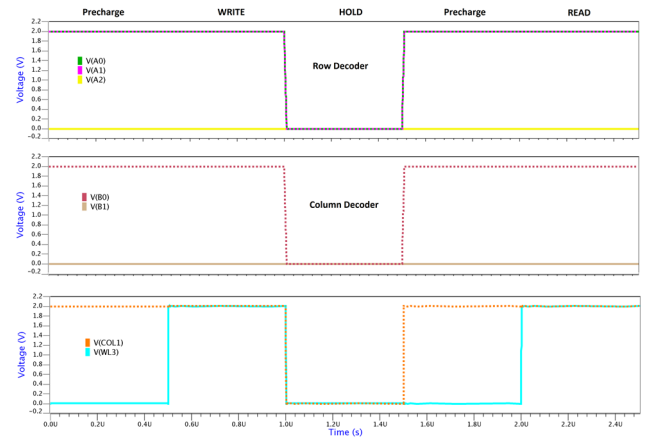


Fig. 9. Decoders Control Signals

B. 8T1R memory array simulation results

Fig. 10 presents the timing waveforms obtained after the NVSRAM array simulation. The Forming stage is preceded by a precharge and a WRITE “1” operation. During WRITE “1”, the precharge circuit and the sense amplifier are kept OFF (Precharge “1” & SE “0”). The write driver is ON (WE “1”), and the data bus is set to “0”. Also, the second row decoder (ENABLE1b “1”) for WL_b is set ON. After Forming, WRITE “0” or “1” can be executed depending of the data input fed to the write driver. For example, if the data input is “0”, the output signal is out “0”. Otherwise, if the data input is “1”, the output signal is out “1” as shown in Fig. 10. Note that WRITE operation is preceded by a Precharge as usual. During STORE operation, the peripheral circuits (precharge circuit, write driver, sense amplifier, and the row decoder) are disabled. Moreover, the column decoder is kept high (ENABLE2 “1”) and the second row decoder (WL_b) is enabled (ENABLE1b “1”) to allow an access to the OxRAM cell. The next stage is a Precharge followed by a READ. During OFF state, all the signals including V_{DD} are OFF.

After power-off, RESTORE operation is performed to re-establish the data on the nodes Q and Q_b of the NVSRAM cell. During this operation, the power supply V_{DD} is reactivated allowing the current to pass through PMOS M1p to the data nodes. This sequence restores the previous data already stored in the OxRAM cell. After RESTORE, a second Precharge and READ operations are executed to make sure that the data restored matches the initial data. Fig. 11 presents an example of the decoders control signals. In this case, all signals of the row decoder are set high, thus WL7 is selected. As for the column decoder, all signals are set high, thus col3 is selected.

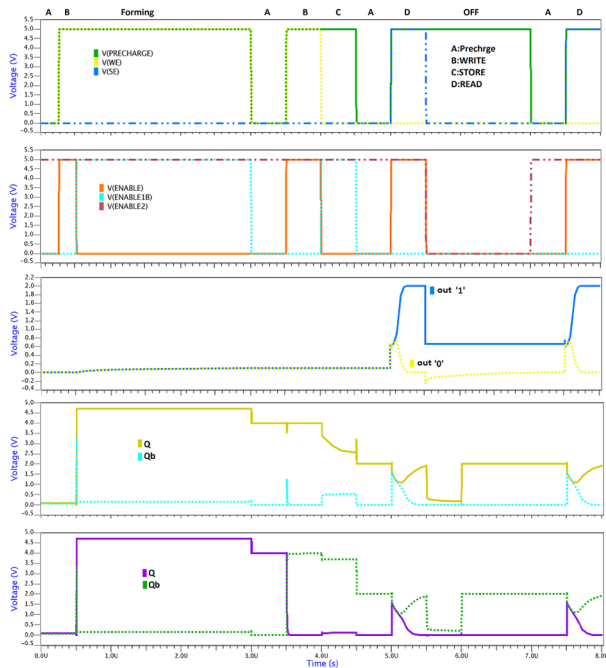


Fig. 10. NVSRAM array timing waveforms

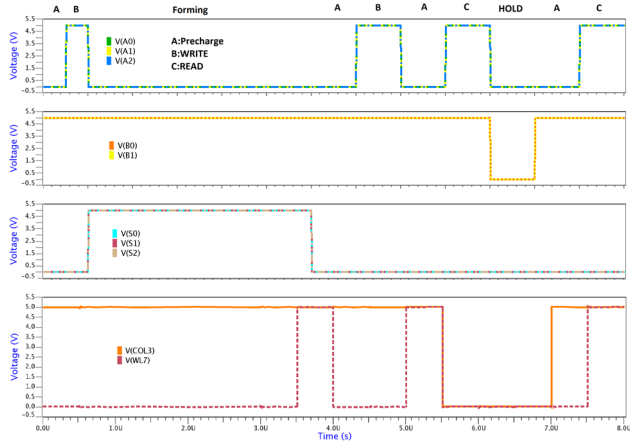


Fig. 11. Decoders Control Signals

C. Comparison

Table I shows a comparison between SRAM and NVSRAM arrays in term of energy consumption and area. The energy consumption of NVSRAM array is slightly higher than SRAM array in normal mode operations, indicating that both structures have similar consumption when used as classical SRAMs. Before power-OFF the data of the NVSRAM is stored in the OxRAM. This process requires specific programming operations (STORE and RESTORE) to be completed. In this special case, the energy consumption of the NVSRAM cell is 61 nJ. Note that the classical SRAM cell is volatile, preventing the data to be retained when powered down. During SRAM HOLD state, V_{DD} is kept high to ensure the data is retained. The energy consumption of the SRAM array in this state is 38.34 pJ. Same result for NVSRAM in HOLD state, since OxRAM device does not have any contribution in the normal mode.

TABLE I: COMPARISON BETWEEN SRAM AND NVSRAM ARRAYS

	SRAM	NVSRAM
Energy Consumption (normal operations)	13.64nJ	14nJ
Energy Consumption (non-volatile operations)	-	22.1nJ
Energy Consumption (hold state)	38.34pJ	38.34pJ
Area	16717 μm^2	20646 μm^2
Complexity (design)	Low	Medium

The area of the SRAM and NVSRAM arrays is 16717 μm^2 and 20646 μm^2 respectively. Since the SRAM array has lower number of transistors and does not embed resistive memory elements, its area is much smaller than the one of the NVSRAM array. Therefore, the area of NVSRAM array is 23.5% larger than that of SRAM array. Fig. 12 presents the 4x8 bytes SRAM array layout with the peripheral circuits. Fig. 13 presents the 4x8 bytes NVSRAM array layout with the peripheral circuits. The layouts have similar structure, since both rely on the same design for the peripheral circuits.

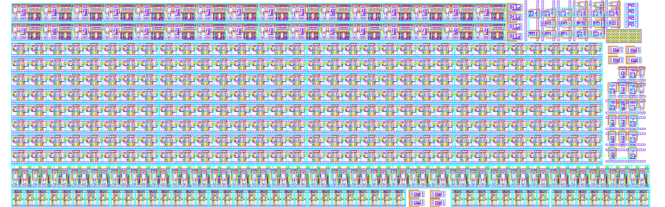


Fig. 12. Layout of 4x8 bytes SRAM array with peripheral circuits

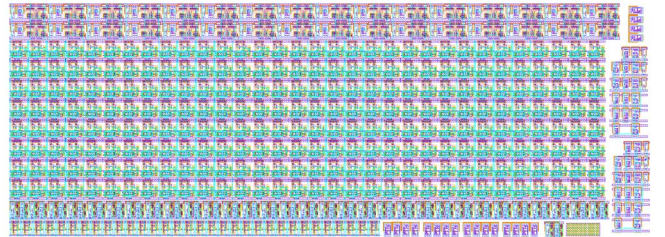


Fig. 13. Layout of 4x8 bytes NVSRAM array with peripheral circuits

V. CONCLUSION

This paper compares SRAM and NVSRAM performances at both cell and array levels. Both structures are implemented in 130-nm technology. The 8T1R NVSRAM cell can perform the normal programming operations (WRITE and READ) as SRAM. A traditional SRAM array and a novel NVSRAM array are presented, then compared in terms of area and power consumption. The NVSRAM array is non-volatile but at the expense of larger area, and higher power consumption. This array can be kept in sleep mode, which is useful for ultra-low power applications.

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