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RRAM-based Non-Volatile SRAM Cell Architectures for Ultra-Low-Power Applications

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Abstract— Static Random-Access Memories (SRAMs) have flourished in the memory market relying on their speed, power consumption and compatibility with standard CMOS process technology. Conventional SRAMs are characterized by volatility, limiting their role in applications where non-volatility is essential. Non-Volatile SRAMs (NVSRAMs) represent an appealing solution, where Resistive RAM (RRAM) can act as a non-volatile element for SRAM. RRAM relies on the basic physical phenomenon of operation called resistive switching. This paper presents different NVSRAM structures, while exploring their principle of operation. Also, a comparison in terms of area, speed, power consumption and design complexity is presented for three NVSRAM memory cells implemented in a 130-nm high voltage CMOS technology from STMicroelectronics.

Index Terms— Computing, Resistive Switching Memory (RRAM), Non-Volatile Static Random-Access Memory (NVSRAM), Area, Power Consumption, Switching Speed.

I. INTRODUCTION

In the recent years, several unconventional memory technologies have been explored [1]. This trend to investigate new technologies is driven by the growing demand for low power, high speed, and low-cost Non-Volatile Memory (NVM) technology suitable for today's market [2]. In this context, Resistive Random-Access Memory (RRAM) is a promising candidate among the next-generation NVM technologies [3]. This technology is characterized by its simple structure, fast switching speed, high scalability, and the capability to be integrated at the Back-End-Of-Line (BEOL) of a conventional CMOS process [4].

Nowadays, memory subsystem directly affects the performance of computing system. The hierarchy of the memory subsystem can be classified under numerous categories: Static Random-Access Memory (SRAM), Dynamic Random-Access Memory (DRAM), and flash memories. All these memories are charge-based. In SRAM, the data is stored as charges at the nodes of the cross-coupled inverters [5-9].

In general, charge-based memories suffer from performance degradation with the down scaling reaching deep nanoscale (10-nm node and beyond). This problem affects the reliability, endurance, and the noise margin of SRAM memory. In this context, emerging memory technologies and specifically RRAM, have been under

extensive research and development for charge-based memory replacement [10].

In the current mobile market, large number of electronic systems and applications depend on semiconductor solid state memories. The performance needed by new electronic devices pushes towards ultra-low power storage media. To fulfill this demand and answer tomorrow's challenges, RRAM emerging devices are considered to be part of these appraised memory technologies [11].

SRAM can benefit from this development, as it can be combined with RRAM technology to create a new hybrid structure called Non-Volatile SRAM (NVSRAM) [12]. NVSRAM array is designed to be electrically stable at the low supply voltages. Moreover, in order to achieve small chip size, the memory cell size must be as small as possible [13].

In this paper, 3 NVSRAM memory cells (6T2R, 10T1R and 8T1R) are presented and compared. These structures are implemented in a 130-nm high voltage CMOS technology from STMicroelectronics [14]. In section II, the oxide-based RRAM technology is presented. In section III, the traditional 6T SRAM is presented and proposed NVSRAM memory cell architectures are detailed. In Section IV, NVSRAM cell simulation results are presented. Also, the layout of all NVSRAM structures is provided along with benchmarking results. In section V, projections are provided to estimate the chip area of each NVSRAM cell at a memory array level. Section VI presents concluding remarks.

II. OXIDE-BASED RRAM TECHNOLOGY

Oxide-based RRAM technology (OxRAM) is based on a Metal-Insulator-Metal (MIM) structure, where the metal electrodes sandwich the insulator layer made of an oxide material as shown in Fig. 1. RRAM devices switching mechanism rely on the formation/dissolution of a conductive filamentary in the insulator layer. This filamentary is based on oxygen vacancies migration between the metal electrodes [15]. Filamentary switching based on Transition Metal Oxides (TMOs) has attracted a lot of attention [16]. In the pristine state, OxRAM device is initially in a very high resistive state and require an electrical soft-breakdown (Forming) equivalent to the injection of oxygen vacancies in the insulating layer. Forming is executed once in the life of an OxRAM cell, where a high voltage is applied across the cell to switch from High-Resistance State (HRS) to a Low-Resistance State (LRS) [17].

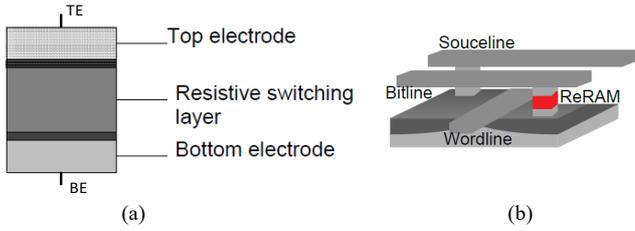


Fig. 1. Basic RRAM structure.

RRAM devices demonstrate reliable resistive switching between HRS and a LRS. The switching from HRS to LRS is termed “SET,” and the switching from LRS to HRS is termed “RESET.” An electrical stimulus (i.e. voltage pulse) applied across the OxRAM device terminals is needed to trigger the switching mechanism. Note that the considered OxRAM technology is compatible with the conventional CMOS fabrication environment and process temperatures [18].

From a circuit simulation point of view, in this work, the Stanford model [19] is used to model the OxRAM element. Stanford model is a physics-based compact model, taking into consideration the temperature effect, the timing effect and variability. These effects are observed in many actual OxRAM cells [20]. Temperature dependency is an important feature of the Stanford model. Indeed, the conductive filament rupture, or dissolution occurs under the effect of a significant change in temperature based on the fundamental concept of Joule heating [21]. During the RESET process and by increasing the applied voltage, the temperature steadily rises until a value called the critical temperature. Above this critical temperature, the conductive filament dissolution/rupture takes place at a fast rate inducing a High Resistance State (HRS) of the device. During the SET process, the temperature rises due to the increase in the CF radius. In the Stanford model [19], the applied voltage, as shown in Fig. 2, directly affects the temperature change in the CF radius. A temperature peak is observed at each SET and RESET sequence.

The correspondence between the experimental data and the simulation data proves that the model captures very well the randomness of the resistance levels during the SET and RESET processes of different RRAM cells. Fig. 3 depicts the simulated I-V curves of Stanford model for 10 SET cycles compared to the experimental data. The variation is mainly due to the random generation of oxygen vacancy.

The hysteresis loop of an OxRAM represented by its current-voltage (I-V) characteristic is shown in Fig. 4. The I-V characteristic shows a sharp SET/RESET transition. OxRAM device usually comes with a select transistor establishing the 1T1R structure. The current limitation is imposed by the select transistor during SET operation in order to limit the current flowing through the device. The current limit is called the “compliance current”. Based on the linear curve presented in Fig. 2, the V_{SET} value needed to switch from HRS to LRS state is equal to 1.6 V, while the V_{RESET} value required to switch back to HRS state is equal to -1 V.

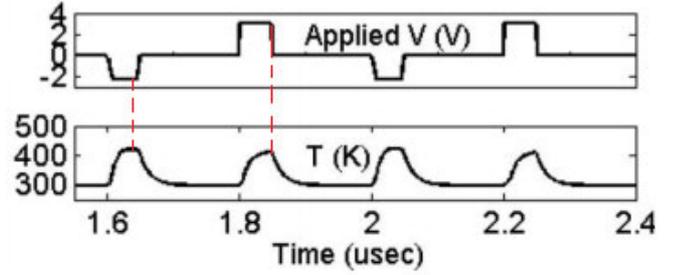


Fig. 2. Stanford model simulated temperature evolution as a function of the applied voltage [22]

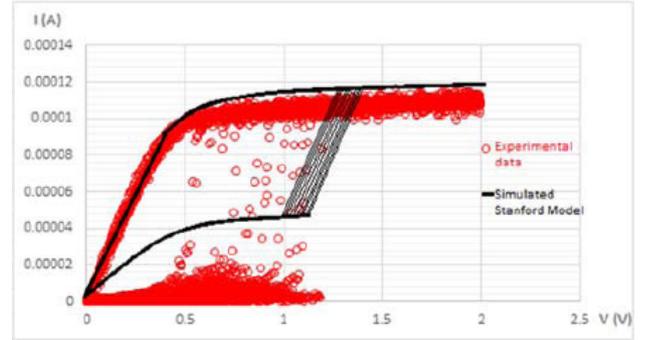


Fig. 3: Single-cell Stanford model variability for 10 SET cycles [21]

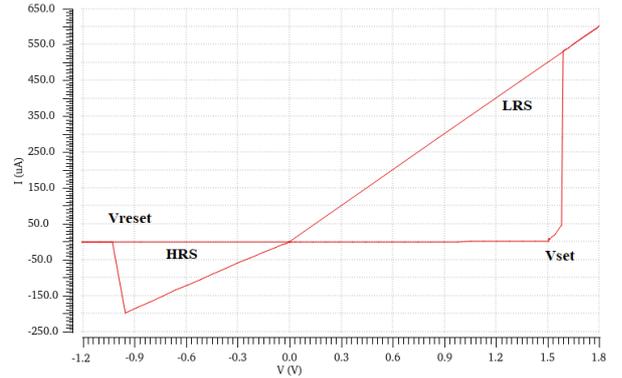


Fig. 4. OxRAM I-V characteristic

III. NVSRAM STRUCTURES

In RRAM-based NVSRAMs, the SRAM cell is combined with a RRAM device. Data nodes of the SRAM cell are connected to the resistive elements allowing data backup operations while the SRAM normal mode operation is preserved (i.e. HOLD, WRITE and READ operations). A STORE operation allows to save the SRAM data in the RRAM device and a RESTORE operation updates SRAM data. STORE and RESTORE operations are performed before power off and after power on respectively [14]. STORE/RESTORE operations in NVSRAMs are the counterparts of WRITE/READ operations in SRAMs.

A. Conventional 6T SRAM memory cell

The conventional SRAM structure follows the cross-coupled inverters structure presented in Fig.5. The 3 main operations in a SRAM are HOLD, READ and WRITE. In an

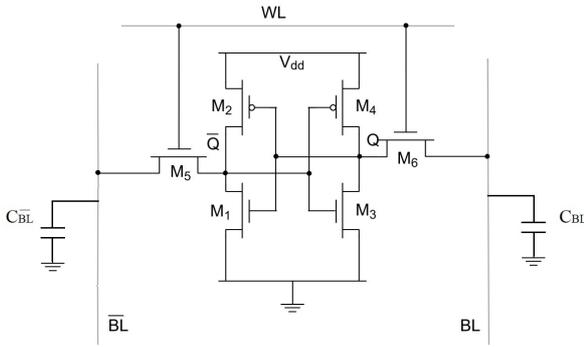


Fig. 5. 6T SRAM cell

array of SRAM memory cells, rows are called Word Lines (WLs) and columns are called Bit Lines (BLs). WLs are connected to the gates of the SRAM select transistors (M5 and M4). WRITE and READ operations in the memory cells are accomplished through the bit lines [23]. During a HOLD operation, the WL is deactivated to disconnect BL and BL/ from the SRAM cell. As a result, data is held in the latch structure on nodes Q and Q/. When WL is activated, READ and WRITE operations can be executed.

Three NVSRAM cells are presented in the next sections. These NVSRAM cells consist of 6 transistors and 2 RRAM devices (6T2R), 10 transistors and 1 RRAM device (10T1R), and 8 transistors and 1 RRAM device (8T1R).

B. 6T2R memory cell

For optimal performances, the addition of RRAM devices should be well located to avoid any malfunction in the storing and restoring operations [24]. To this end, RRAM devices take PMOS transistor locations in the 6T2R memory cell as presented in Fig. 6. This solution reduces the number of transistors of the memory cell compared to other NVSRAM cells with Transmission Gates (TGs). PMOS transistors are added on each side of the SRAM cell to form TGs. The main benefit of this topology is related to the use of TGs. A transmission gate is mainly used to enhance the switching speed, especially in storing “1” as the single NMOS in the traditional 6T SRAM is not able to pass strong “1”. The (W/L) ratio of NMOS and PMOS is kept as the standard minimum with $W = 150$ nm and $L = 130$ nm to limit the current during RRAM programming cycles [25].

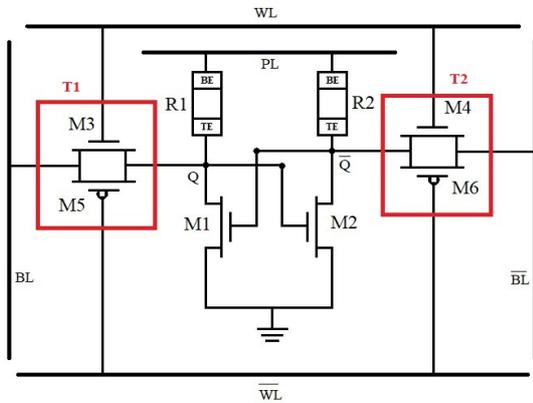


Fig. 6. 6T2R NVSRAM Cell

In the HOLD state, no write or read operation is permitted as the WL is grounded. During a STORE operation, TGs T1 and T2 are ON, connecting the bit lines to the RRAM top electrodes (TE). In the process of storing “1” on R1, BL is set to V_{DD} and BL/ and PL are grounded. In this configuration, M1 transistor is OFF and a current flows through T1 to R1. The voltage applied on TE decreases the resistance of R1, thus writing a logical “1” (R1 is SET). Note that when storing “1” in R1 on the first cycle, “0” is stored in R2 in a second cycle. In the process of storing “0” on R1, the BL is set to “0” and BL/ and PL are set to V_{DD} . In this configuration, M1 transistor is ON and a current flows through R1 to T1. The voltage applied on BE increases R1 resistance, thus writing “0” on R1 (R1 is RESET). Note that due to the design topology used, STORE and WRITE operations are exhibited simultaneously.

During a RESTORE operation, WL is set to 0 V. PL line is set to V_{DD} , inducing a current through the RRAM devices. Data stored in RRAM devices are restored (i.e. nodes Q and Q/ are updated). If R1 is in LRS state and R2 in HRS state, the storage node Q remains at “1” and node Q/ is discharged through M2. If R1 is in HRS state and R2 in LRS state, Q discharges back to “0” and Q/ is charged to “1”.

C. 10T1R memory cell

The 10T1R structure presented in Fig. 7 follows the basic SRAM cross-coupled structure and only one RRAM device is used. T1 and T2 are used as access gates similar to the 6T2R. RRAM top electrode is connected to the output of the control transmission gate T3. As usual, STORE is executed before powering down the cell. NMOS and PMOS transmission gates sizing follows the standard minimal design rule with $W = 150$ nm and $L = 130$ nm [26-27].

HOLD operation is similar to the 6T2R cell where TGs T1, T2, and T3 are OFF. During the WRITE operation, T1 and T2 are ON and T3 is OFF to complete the programming of the nodes (Q and Q/). During STORE, R1 is accessed by turning ON T3 allowing Q voltage to reach TE. For instance, in the process of storing “1”, PL and WL are grounded. As a result, R1 cell is SET since the node Q was already programmed to “1”.

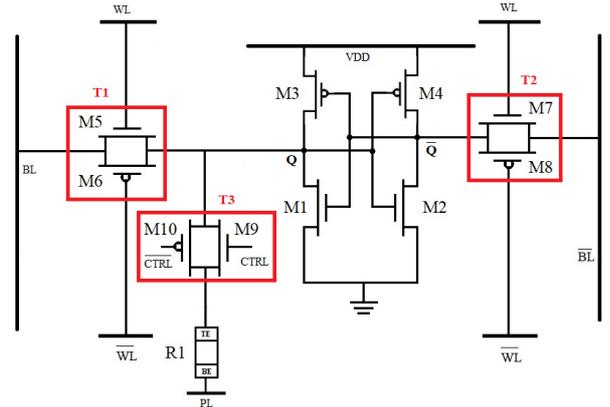


Fig. 7. 10T1R NVSRAM Cell

During a RESTORE operation, the reading circuitry is connected to the bit lines. PL is set to $V_{DD}/2$ and TG T3 is ON. The bit stored in R1 is restored, and nodes (Q and Q/) are updated. RESTORE state in this design rely on one RRAM device. In this structure, only one SET/RESET operation is needed, since there is one RRAM device, where in the previous structure 2 operations were needed.

D. Novel 8T1R NVSRAM cell

The proposed 8T1R structure presented in Fig. 8 is characterized by a minimal number of control signals (i.e. BL and WL). M3 and M4 represent the traditional SRAM access transistors. STORE/RESTORE operation is executed through two additional transistors M5 and M6. The OxRAM device is connected to M5 transistor (TE) and to the node Q/ (BE).

During Forming, BL and WL/ are set high, WL and BL/ are set low. In this stage, the OxRAM can be formed in one step (M6 is ON: direct connection between BL and the OxRAM). STORE operation is preceded by a WRITE operation. During WRITE “0” operation, BL and WL/ are set low, WL and BL/ are set high. RESET is the next stage after WRITE “0”, where WL and BL are set low. In the Pre-charge stage (normal operation), BL and BL/ are set to $V_{DD}/2$ (0.9V). Regarding the READ operation, it is executed through WL which is set high.

After STORE (SET/RESET) and READ operations, all the signals are turned OFF including V_{DD} . STORE operation is required to retain the data after the power is down.

IV. SIMULATION RESULTS

6T2R, 10T1R and 8T1R NVSRAM simulation results are proposed in this section, followed by comparison of the different NVSRAM architectures. Voltage pulses (WL, BL and PL) are set to 1.8 V which is compatible with the available voltage supply V_{DD} for the considered technology.

A. 6T2R NVSRAM

Fig. 9 presents the 6T2R NVSRAM cell operation waveforms. Timings are voluntarily relaxed for memory cell operation understanding. First, the OxRAM cell R2 is RESET and R1 cell is SET.

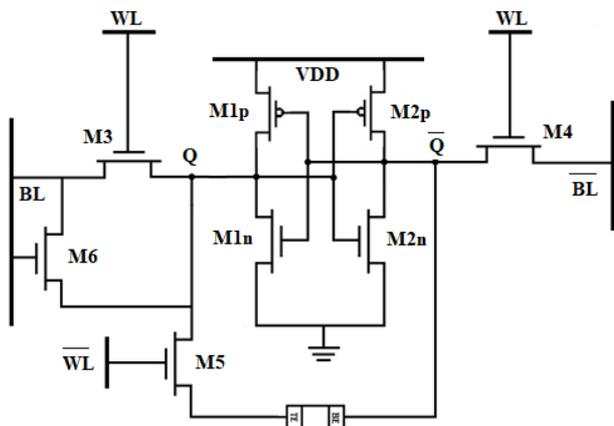


Fig. 8. 8T1R NVSRAM Cell

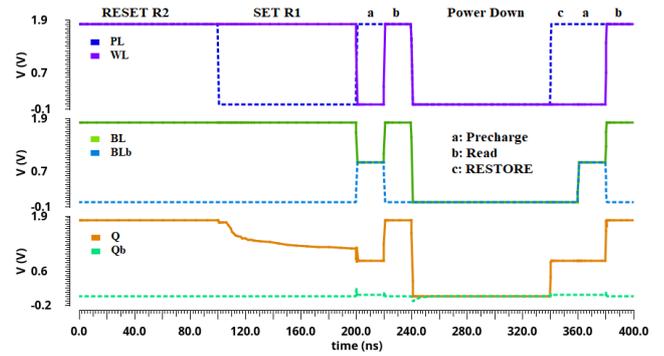


Fig. 9. 6T2R NVSRAM timing waveforms.

During OxRAM programming operations, WL is set High and PL is kept at V_{DD} during RESET and connected to ground during SET. During SET, Q voltage decreases to ~ 0.9 V, while Q/ stays at 0 V. After SET and RESET, a pre-charge and a read operation are executed. During the pre-charge stage, BL and BL/ are set to $V_{DD}/2$ and the WL is grounded. Result of the read operation is seen through the charge/discharge of BL capacitances. Q and Q/ kept their previous values equal to 1.8 and 0 V respectively.

At 240 ns the memory cell is powered down (i.e. all voltages are set to 0 V). RESTORE operation starts at 340 ns ($PL=V_{DD}$ and $WL=0$) to recover Q and Q/ values from the OxRAM devices. Following the RESTORE operation, a pre-charge and READ are performed from 360 ns to check Q and Q/ values. Q and Q/ values equal 1.8 and 0 V respectively confirming the proper operation of the RESTORE cycle. Fig. 10 shows the 6T2R cell layout with an area occupancy equals to $32.6 \mu m^2$. Static noise margin of the SRAM cell depends on the Cell Ratio (CR), supply voltage and also pull up ratio. Cell ratio is the ratio between sizes of the driver transistor to the load transistor during the read operation. Pull up ratio is also nothing but a ratio between sizes of the load transistor to the access transistor during write operation. Driver transistor is responsible for 70 % value of the SNM. SNM, which affects both read margin and write margin, is related to the threshold voltages of the NMOS and PMOS devices (i.e. in SRAM cells [28]).

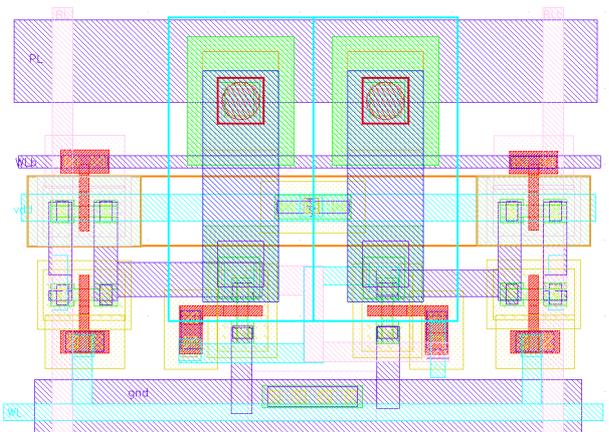


Fig. 10. 6T2R NVSRAM layout

Fig. 11 presents the Static Noise Margin (SNM) of the 6T2R cell for different SET/RESET duration (in the range [50ns-1 μ s]). The SNM is obtained using the butterfly method where Q voltage is measured against Q/ voltage and vice versa [29]. The SNM increases with the increase of the STORE Pulse (SP) to reach 365 mV. Table I shows the impact of SP parameter on the 6T2R parameters (SET current, R_{ON} , SET energy, switching speed and SNM). The energy consumed to store "1" as this value increases from 1.97 to 77.11 pJ.

B. 10T1R NVSRAM

Fig. 12 presents the timing waveform of the 10T1R NVSRAM cell. The 10T1R timing waveform starts with a WRITE operation then a STORE is performed before power down, which is mandatory to RESTORE data. RESTORE, pre-charge and read timing are kept to 20 ns. Fig. 12 shows that Q and Q/ values are equal to 1.8 and 0 V respectively indicating that RESTORE is working properly. Fig. 13 shows the 10T1R cell layout, where the area occupied is 40 μ m².

C. 8T1R NVSRAM

Fig. 14 presents the 8T1R NVSRAM cell operation waveforms. During Forming, BL, WL/ and V_{DD} are set high to form the OxRAM device, where the voltage applied to BL is 5 V. BL is first pre-charged to V_{DD} while BL/ is grounded and the access transistors (M5) is activated by applying a pulse on WL/. In a second step, power signal is reconnected (with a value of $V_{DD}/2$) and WL/ signal is disabled. During the pre-charge (after RESTORE), BL and BL/ are set to $V_{DD}/2$ (0.9V). READ after RESTORE follows the conventional signal sequence, where WL is set high and WL/ is set low.

The sequence of operation coming after power OFF consists in pre-charging the storage node Q according to the state of the OxRAM device, with BL set to 0.5 V. For instance, if the OxRAM device is in HRS, the voltage at the node Q is lower than the V_{th} of M_{1n}/M_{2n} .

Accordingly, when the power signal is reactivated to $V_{DD}/2$, the current coming from the supply, through the PMOS (M_{2p}) device of the inverter, charges the node Q/ to $V_{DD}/2$. Conversely, if the OxRAM device is in LRS, the voltage of the node Q is higher than the V_{th} of M_{1n} and the current coming from the power signal ($V_{DD}/2$) charges the node Q to a higher voltage than the V_{th} of M_{1n} . Fig. 15 shows the 8T1R cell layout, where the area occupied is 45 μ m². As already mentioned, the main advantage of this structure is the use of a minimal number of signals (BL, WL and V_{DD}). Also, this NVSRAM cell offers low power consumption, low chip area, and the Forming operation is executed in one step.

However, the drawback of this structure is related to the RESTORE operation complexity, which is executed in two steps. During the first step, V_{DD} is adjusted to $V_{DD}/2$ to RESTORE the right values at the nodes Q and Q/, thus BL and BL/ cannot interfere with nodes Q and Q/. WL and WL/ are both grounded in the second step of the RESTORE operation. BL and BL/ are adjusted to 0.5 V (below V_{th} of the

NMOS). When the power signal is reactivated ($V_{DD}/2$), the current coming from the supply through the PMOS device M_{1p} of the inverter tries to charge the node Q to $V_{DD}/2$. Yet, since the M_{1n} is ON, the charges previously built up on the node Q by PMOS M_{1p} discharge to ground.

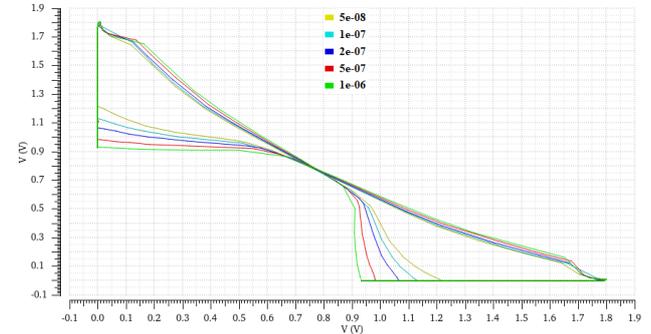


Fig. 11. 6T2R SNM for different STORE Pulses varying in the range [50ns-1 μ s].

TABLE I: IMPACT OF the STORE Pulse ON THE 6T2R CELL PARAMETERS

SP (ns)	SET current (μ A)	R_{ON} (K Ω)	off/on Ratio	SET energy (Store "1", pJ)	SNM (mV)
50	30.525	59	6.36	1.97	226
100	33.3	54	6.95	4.85	262
200	36.396	49.4	7.59	11.79	293
500	41.63	43.2	8.68	33.72	336
1000	47.678	37.7	9.95	77.11	365

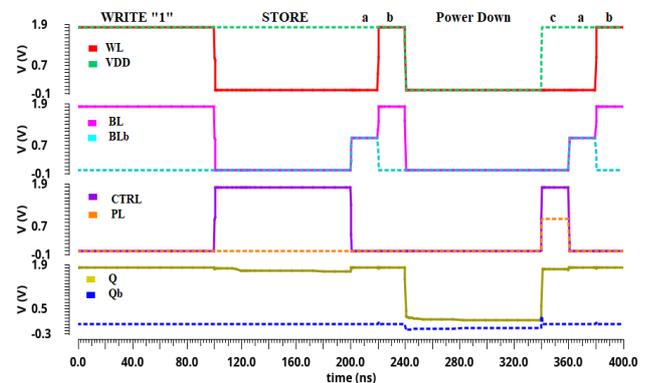


Fig. 12. 10T1R NVSRAM timing waveforms

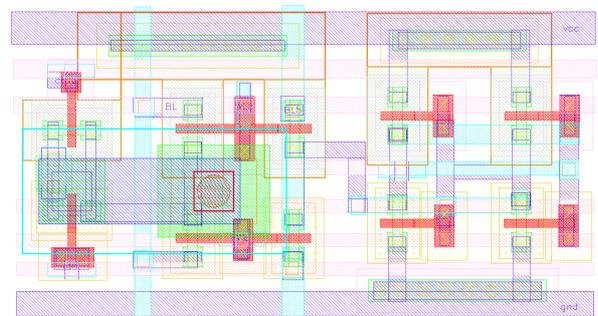


Fig. 13. 10T1R NVSRAM layout

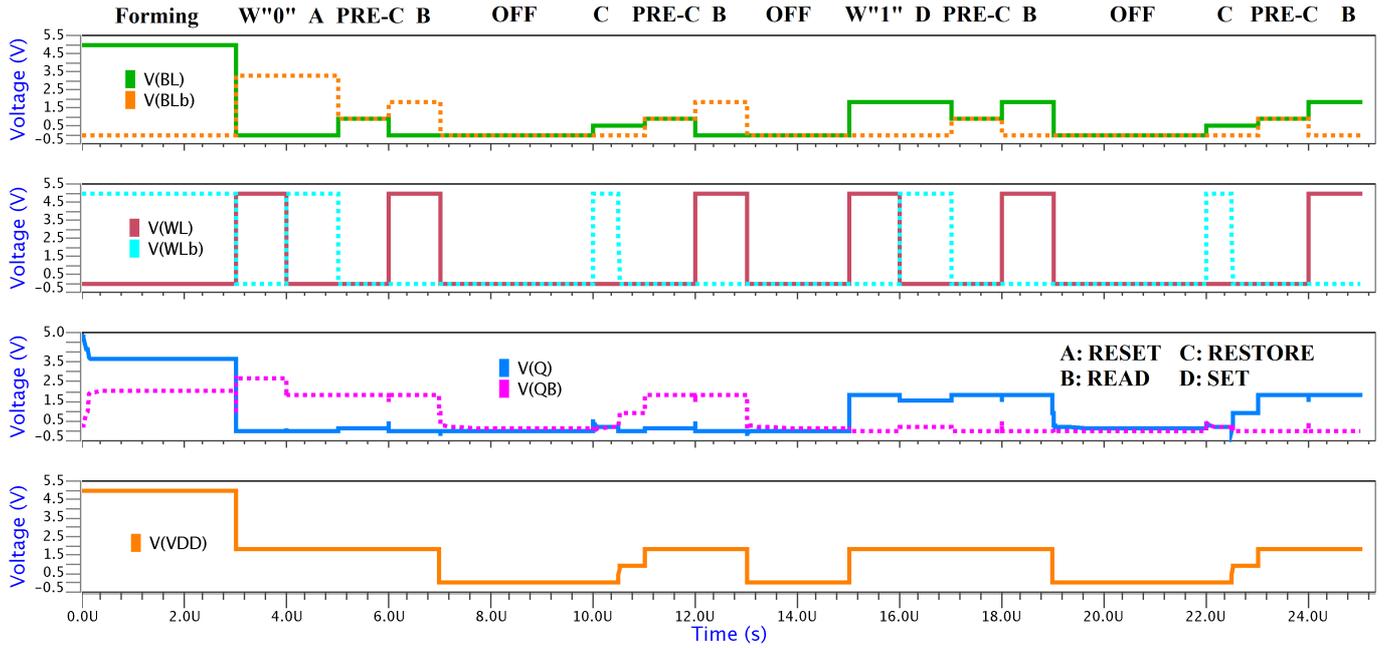


Fig. 14. 8T1R NVSRAM Timing Waveforms

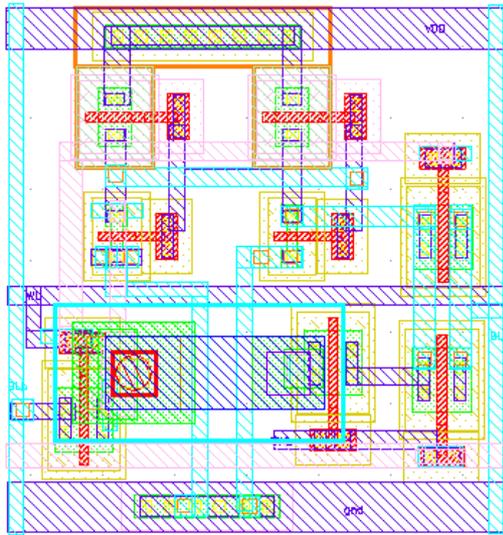


Fig. 15. 8T1R NVSRAM layout

D. NVSRAMs Comparison

A comparison between the 6T2R, 10T1R and 8T1R cells is essential to assess the performance of the different topologies. Table II shows a comparison between the three NVSRAM structures. The comparison is based on four essential parameters including the LRS resistance (R_{ON}), the SNM, the SET energy and the area. The 10T1R cell has higher LRS than the 6T2R and 8T1R. The SET energy of the 6T2R and 10T1R is very close, but the 10T1R STORE operation is executed just before shutdown. Same as the 8T1R, SET energy is significantly higher, since the final reached LRS is low. The area occupied by the 10T1R is larger (+22.7%) since there is a higher number of transistors. 8T1R

area is 38% larger than 6T2R, since transistors used have higher W/L ratio. These results indicate that the 6T2R cell has an advantage in terms of area, but the 10T1R and 8T1R cells avoid additional power consumption because WRITE and STORE operations are separated.

V. NVSRAM CELL ARRAY

In a memory array configuration, NVSRAM cells are arranged to share connections in horizontal rows and vertical columns. The horizontal lines are the Word Lines (WLs), while the vertical lines along which data flow into and out of cells are called Bit Lines (BLs). A cell is accessed for reading or writing by selecting its row and column [30]. Each NVSRAM cell has the capability of storing “0” or “1”.

An NVSRAM array is similar to a SRAM array. It consists of multiple cells, where each cell is designed following a specified structure as shown in Fig. 16. When a NVSRAM array is powered-up, initially each individual memory cell acquires either a logic “0” or logic “1” value according to data stored in the RRAM cells. Also, maximizing the noise margin of NVSRAM cells is a critical factor as it is directly related to the symmetry of the memory cell [31].

TABLE II: COMPARISON BETWEEN NVSRAM CELLS

Structure	R_{ON} (K Ω)	SET energy (pJ)	SNM (mV)	Area (μm^2)	Restore method	Non-volatility
6T2R [25]	54	4.85	365	32.6	Differential	Real-time
10T1R [26]	65	4.14	400	40	Single-ended	Before shutdown
8T1R	5.15	52.6	420	45	Single-ended	Before shutdown

The three NVSRAM cell architectures are used to build a 4x4 (16-bit) elementary SRAM array presented in Fig. 14. First, the functionality of each memory array is validated. Then, the area of the memory arrays is evaluated. Table III shows a comparison between the three different NVSRAM arrays. The area of the 6T2R, 10T1R and 8T1R NVSRAM arrays is approximately $572 \mu\text{m}^2$, $720 \mu\text{m}^2$ and $806 \mu\text{m}^2$ respectively. 6T2R array has better density ($35.75 \mu\text{m}^2/\text{bit}$) than the 10T1R array ($45 \mu\text{m}^2/\text{bit}$) and the 8T1R array ($50.375 \mu\text{m}^2/\text{bit}$) [32]. To be fully functional, the memory array has to be associated with the surrounding circuitry.

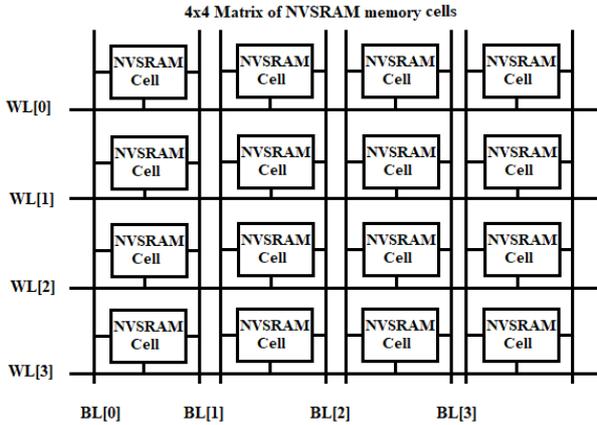


Fig. 16. NVSRAM cell array

TABLE III: COMPARISON BETWEEN NVSRAM ARRAYS

Arrays (16-bit)	Width (μm)	Height (μm)	Area (μm^2)	Bit Density ($\mu\text{m}^2/\text{bit}$)
6T2R	26.8	21.2	568	35.5
10T1R	34.8	18.8	655	41
8T1R	27.4	29.3	803	50.18

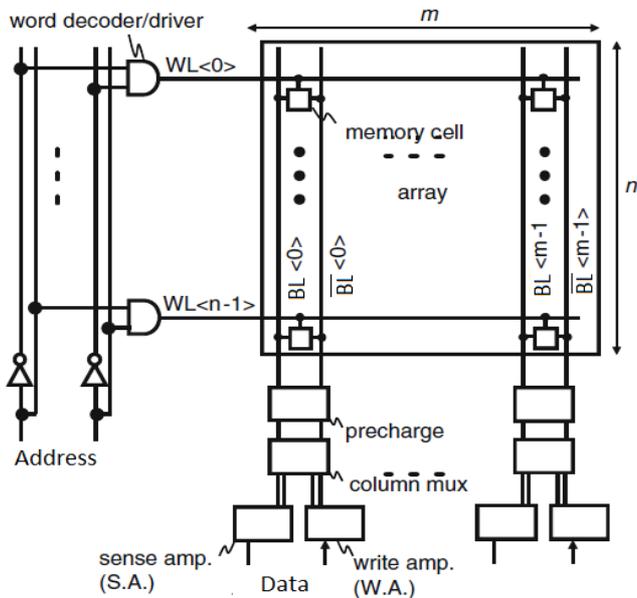


Fig. 17. Basic full NVSRAM cell array structure [28]

Fig. 17 shows a basic full NVSRAM cell array structure including n rows and m columns. A word decoder selects one WL based on addresses configuration. Column decoder control circuits consist in numerous peripheral circuits including pre-charge circuits, column multiplexers, sense amplifiers, write amplifiers, etc. READ operation is initiated by selecting the word line. Before this step, the pre-charge circuit increases the bit-line voltage to V_{DD} or $V_{DD}/2$. Circuits delivering the logic levels are located at the edge of the bit lines (write amplifiers). After transferring WRITE data to the bit lines, WRITE operation is finalized by turning off the word line [33-34].

VI. CONCLUSION

This paper compares three NVSRAM cells, including 6T2R, 10T1R and 8T1R cells. All structures are based on the traditional 6T SRAM and implemented in 130-nm technology. TGs are added to 6T2R and 10T1R structures to enhance the overall performance. 6T2R structure achieves low area compared to 10T1R and 8T1R cells. STORE and WRITE operations can be executed separately in 10T1R and 8T1R cells. 8T1R cell introduces a novel structure with a minimal number of control signals. Three NVSRAM array based on the proposed NVSRAM cells are presented with area estimation projections.

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