

A Novel Trench-Based Triple Gate Transistor With Enhanced Driving Capability

R. Gay, V. Della Marca, H. Aziza, M. Mantelli, F. Trenteseaux, F. La Rosa, A. Regnier, S. Niel and A. Marzaki

Abstract—This paper addresses the design, implementation, and characterization of a novel high-density Triple Gate Transistor in a 40 nm embedded Non-Volatile Memory technology. Deep trenches are used to integrate two vertical transistors connected in parallel with the main planar transistor. Thanks to the built-in trenches, the proposed manufacturing process increases the transistor width without impacting its footprint. The voltage/current characteristics of a planar MOS structure are compared with the features of the new Triple Gate Transistor. The new architecture provides an improved driving capability, with an on-state drain current twice as high as its equivalent standard MOS, combined with a lower threshold voltage, suitable for low-voltage applications. Finally, the gate oxide and junction reliability are validated over the operating voltage range.

Index Terms—Multigate transistor, MOS devices, Trench transistor, Driving capability, Flash memory.

I. INTRODUCTION

THE continuous development of consumer electronics underlines the high demand for low-cost and reliable microelectronic devices [1], [2]. The need for more integration has accelerated the current design trend for more scalability in almost every device parameter, such as channel length, gate dielectric thickness, supply voltage, and device leakage [3]. As most of these parameters are now reaching fundamental limits, new alternatives to the existing devices have to be identified in order to meet higher performance levels using new innovative architectures. In recent years, several devices, using multi-gate or gate-all-around transistors as an alternative to classical MOS, have emerged enabling enhancements in circuit performance [4]-[6]. Alternatively, and mostly for integrated passive devices, deep trenches are used in various ways, including as insulators, inductors, or DRAM capacitors to increase integration density [7].

The aim of this work is to build an area-efficient transistor with a high driving capability. Starting from a classical MOS transistor denoted Standard Gate Transistor (SGT), two lateral conduction channels controlled by vertical trenches enhance the

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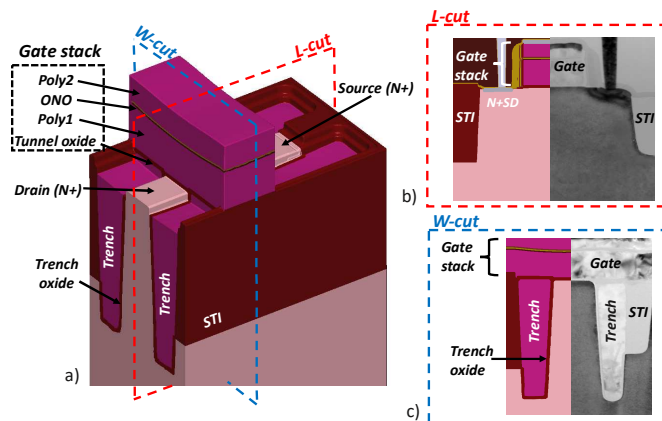


Fig. 1. (a) Triple Gate Transistor 3D view and TEM/schematic cross-sections (b) in length (L) direction, (c) in width (W) direction

driving capability. This combination results in the proposed Triple Gate Transistor (TGT) [8]. Note that vertical deep trenches are currently used in embedded NOR Flash fabrication processes [9].

The next paragraph presents the TGT device. In Section III, experimental results are presented to demonstrate the functioning of the device. Finally, Section IV concludes this paper.

II. DEVICE DESCRIPTION AND MANUFACTURING

The TGT is integrated in a Non-Volatile Memory (NVM) environment and designed following the process flow of an embedded NOR Flash technology. No additional steps or masks are required to build the device. Fig. 1 shows (a) a 3D schematic model of the TGT and (b) (c) TEM versus schematic cross-detailed views. The TGT is created as follows: active definition and NVM implantations are first performed. Deep trenches are then etched and an oxide is grown along sidewalls of the trenches. The latter are filled with an in-situ doped polycrystalline silicon to create two vertical gates. Finally, the planar gate patterning is processed. It includes two polysilicon layers (poly1 and poly2), an oxide/nitride/oxide (ONO) interpoly dielectric and a tunnel oxide. The planar gate contact is realized on poly1 through the poly2/ONO stack while two vertical trenches contacts are shifted with respect to the gate stack and connected to trenches polycrystalline silicon. Source and drain contacts are formed with n+ implantation.

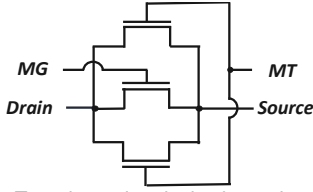


Fig. 2. Triple Gate Transistor electrical schematic

Fig. 2 maps the electrical schematic model of the TGT. The TGT is modeled by three MOS transistors connected in parallel, and therefore has three conduction channels. The first channel, which is located between the Drain and the Source, is controlled by the stacked gate (Poly1+tunnel oxide) and belongs to the device denoted by MOS Gate (MG) transistor. The second and third channels, which are also located between the Drain and the Source, are controlled by the trenches (shorted) and belong to the devices denoted by MOS Trenches (MT) transistors.

III. EXPERIMENTAL RESULTS

Fig. 3 shows I-V characteristics in linear mode with drain voltage $V_D = 0.1$ V and in saturated mode with $V_D = 2$ V for: (a) MG and SGT, (b) MT and (c) TGT. The TGT characteristics include the contribution of three transistors: the MG and two trench transistors. A summary of the most relevant parameters in saturated mode is shown in Table I of Fig. 3 (d). The driving current parameter (I_{on}) is extracted for gate voltage $V_G = 4$ V and the threshold voltage (V_t) is extracted for the drain current $I_D = 0.1$ μ A. Moreover, we highlight the I_{on}/V_t ratio that can be used as a design parameter figure of merit. In Fig. 3 (a) the standard SGT MOS is compared with the MG transistor of the triple-gate device. The conduction currents are equivalent, while the MG threshold voltage slightly decreases due to the presence of vertical transistors. The latter impact the oxide thickness at the edges of the active substrate. Based on Fig. 3 (a)-(c), we observe that the TGT provides an I_{on} driving current (463 μ A for $V_D = 2$ V) three times higher than the SGT (143 μ A for $V_D = 2$ V), because the TGT benefits from a triple conduction (i.e., trenches conduction in addition to the classical MOS channel conduction). Regarding the leakage current (I_{off}) extracted at $V_G = 0$ V, the TGT and SGT values are comparable

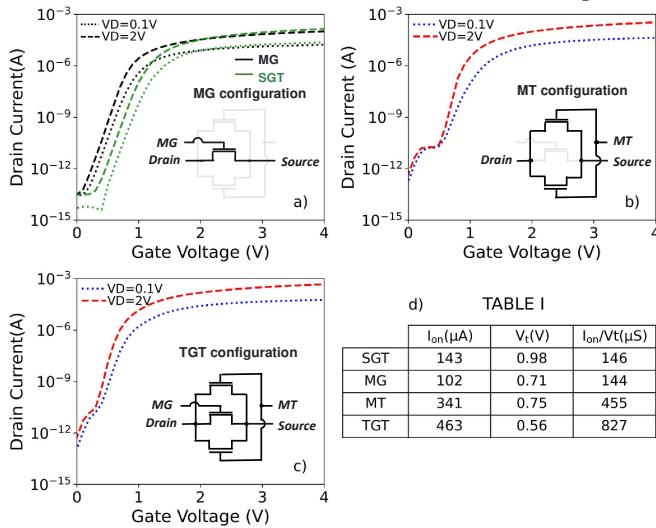


Fig. 3. I-V characteristics in linear and saturated conduction modes for: (a) MOS Gate and SGT, (b) MOS Trenches and (c) Triple Gate Transistor. (d) Comparison metrics in saturated mode.

(less than 1 pA). Quantitative results are provided in Fig. 3 (d) MOS Gate I_{on} (102 μ A) represents around 25% of the TGT I_{on} current and MOS Trenches I_{on} (341 μ A) represents 75% of the TGT I_{on} current. Moreover, we can see a higher threshold voltage for the SGT ($V_t = 0.98$ V) compared to the TGT ($V_t = 0.56$ V). This difference is explained by a thinner trench oxide thickness and by the MT geometry. In Fig. 3 (b) we can note at the beginning of I-V characteristics (around $I_D = 10E^{-11}$ A and $V_G = 0.2$ V) a hump effect due to the parasitic transistors formed by the active rounding [10], [11]. This effect is reflected in the TGT characteristics (Fig. 3 (b)) even though its impact is negligible.

In Fig. 4 (a), the test results of gate voltage stress are provided for the TGT and the SGT. We note that the tunnel-oxide breakdown is reached at 15 V for both devices. However, the MG gate current start increasing before the gate current of the SGT does. This early leakage current is caused by an oxide weakness at trench-gate corners induced by the manufacturing process (as already mentioned before during V_t extraction). Regarding the MT transistor, it starts to leak at 3 V with a breakdown voltage of 10 V. This lower value is explained by the irregular thickness of the trench oxide caused by a non-uniform oxide growth along sidewalls. In Fig. 4 (b) are featured the test results of Drain/Bulk junction voltage stress for the TGT and the SGT in off-state ($V_G = 0$ V). Comparable Drain/Bulk junction breakdown characteristics are reported for TGT and SGT. These last stress tests demonstrate the robustness of the TGT: indeed, the maximum gate and drain voltages reported for the addressed technology are respectively $V_G = 4$ V and $V_D = 3$ V, far from the breakdown threshold (around 7.7 V).

Fig. 5 reports the evolution of the driving current (I_{on}) versus different device footprints with constant L. The blue linear curve which is related to the SGT is compared with the characteristics of the proposed TGT. For equivalent I_{on} current, the trench transistors integration allows to divide the device

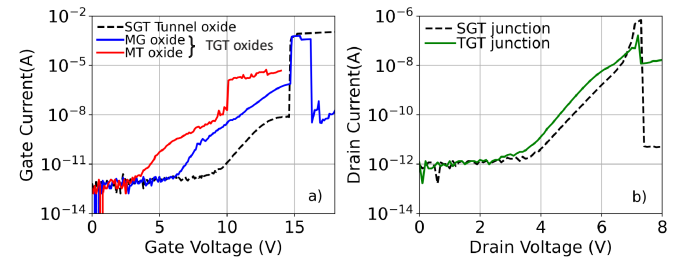
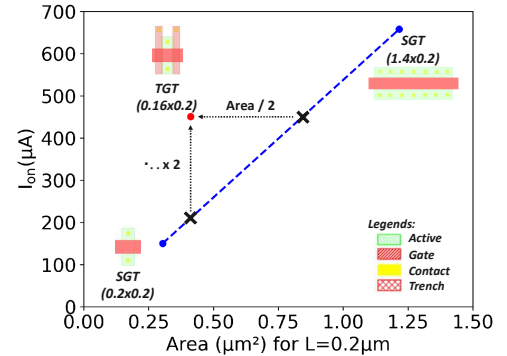


Fig. 4. (a) Gate voltage stress I-V characteristics. (b) Drain/Bulk junction voltage stress I-V characteristics (average over three measurements).

Fig. 5. I_{on} versus Area for the same L ($0.2\mu m$)

area by a factor two. Therefore, for an equivalent area, I_{on} current is doubled if the TGT architecture is considered.

IV. CONCLUSION

In this paper we propose a new transistor architecture denoted by Triple Gate Transistor that uses deep polysilicon trenches to build side transistor. The TGT manufacturing process and its different conduction modes are first introduced. The experimental results demonstrate the functionality and reliability of the TGT based on I-V characteristics and stress tests results. The driving capability of the TGT device is two times higher than its equivalent standard MOS counterpart. The I_{off} current is maintained constant and a V_t decrease is reported. The new proposed architecture can provide significant chip-level area savings as only half the silicon area is needed to reach an equivalent driving capability. For future work, we plan to use the TGT device with decorrelated gates (i.e., two different control signals for the trench transistors) to explore new opportunities for low-voltage and analog applications.

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