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# Performances and Stability Analysis of a novel 8T1R Non-volatile SRAM (NVSRAM) versus Variability

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**Abstract**— Static Random-Access Memories (SRAMs) are an integral part of the chip industry, occupying a noticeable share of the memory market due to their high performance and compatibility with CMOS technology. Traditional SRAMs do not have the capacity to retain data after power-off, preventing their use in non-volatile applications. This paper presents a novel Non-Volatile SRAM (NVSRAM) device based on Resistive RAM (RRAM) technology. A comparison between SRAM and the proposed NVSRAM performances is proposed at both cell and memory array level. The comparison covers several metrics such as energy consumption, area and static noise margin (SNM). Moreover, this work proposes a deep analysis of the impact of RRAM variability as well as the CMOS subsystem variability on the NVSRAM performances. The proposed structure demonstrates robust NVSRAM performances in terms of stability and reliability despite RRAM variability.

**Index Terms**— Static Random-Access Memories (SRAMs), Non-Volatile SRAM (NVSRAM), Resistive RAM (RRAM), energy, area, variability, switching time, Static Noise Margin (SNM).

## I. INTRODUCTION

For modern high-performance technologies, the memory subsystem directly affects the performance of computing systems [1]. The memory subsystem includes Static Random-Access Memory (SRAM), Dynamic Random-Access Memory (DRAM), and Flash memories. All these memories are charge-based. In SRAM, the data are stored as charges at the nodes of the cross-coupled inverters [2, 3]. SRAM has been widely used in the memory market. This rapid growth is backed by SRAM appealing characteristics, including fast operations and low power consumption in standby mode [4]. Moreover, SRAM cell uses the same fabrication process as logic, thus no extra cost is needed. These properties are unique for SRAM when compared to other memories such as DRAM or Flash memories. However, as the technology scales down, SRAM standby leakage power is becoming one of the most critical concerns for low power applications [5], particularly when battery-powered applications are targeted [6]. Therefore, there is a need for energy efficient non-volatile SRAM cell architectures able to retain data after power-off: data are moved to the non-volatile memory elements to retain the system state after power interruption and restored after power-ON.

Today's dominant Non Volatile Memory technology is Flash. But its endurance is limited (approximately  $10^6$  cycles), and its operation access frequency is very slow, with program/erase time in the order of microseconds to milliseconds [7]. Moreover, Flash devices need high voltages for storage operations which is hardly compatible with ultra-low power applications. The quest for low power NVM solutions is the main driving force behind the rapid growth of emerging memories, such as Ferroelectric RAM (FeRAM) [8], Spin Torque Transfer RAM (STT-RAM) [9], Phase-change RAM (PCRAM) [10] and Resistive RAM (RRAM) which encompass Conductive Bridge RAM (CBRAM) and Oxide based-RAM Memories (OxRAMs) [11,12]. RRAM is considered as a promising solution that can elevate SRAM to the next level in the memory technology hierarchy [13]. SRAM can be combined with Resistive RAM (RRAM) technology to create a new hybrid structure referred to as Non-Volatile SRAM (NVSRAM) [14]. Indeed, due to its relatively small write and read latency and high density [15], RRAM is considered as a promising candidate for designing NVSRAMs memory circuits. The latter is expected to replace traditional SRAM in SoC applications [16]. However, from a reliability point of view, RRAM is affected by variability. Indeed, the variance from cycle to cycle (C2C) and from device to device (D2D) can be very large, impacting directly the memory cell performances and particularly the resistance ON/OFF ratio. Although several NVSRAM architectures have appeared in the literature [17-25], none of the related work has validated the stability and performances of the proposed NVSRAM memory cells versus RRAM variability as well as CMOS variability. An attempt to address this issue was proposed in [26], but the FORMING operation of the RRAM memory cell is missing as well as the use of a RRAM model calibrated on actual RRAM devices for simulations. Moreover, the impact of the RRAM variability on Static Noise Margins (SNMs) is not analysed and the variability of the CMOS subsystem is not accounted. Also, projections at the circuit level are missing.

In this paper, we address these issues by leveraging on an OxRAM model calibrated on silicon [27] and featuring a FORMING operation as well as a variability dependency in agreement with experimental measurements [28]. This work is motivated by the strong variability inherent to actual RRAM technologies and more particularly to the OxRAM

technology addressed in this study. The variability analysis also targets the CMOS subsystem (including transistor mismatch [29, 30]) and especially the memory cell access transistor as its impact on the memory cell electrical characteristics is dominant [31, 32]. This type of analysis combining OxRAM and CMOS variability is completely missing in the current state-of-the art. In this context, the contributions of this paper are as follows:

- 1) A novel NVSRAM memory cell architecture implemented in a 130-nm high voltage CMOS technology from STMicroelectronics [33] is introduced.
- 2) A deep analysis regarding the effect of variability (including OxRAM and CMOS variability) is conducted based on an OxRAM model calibrated on silicon.
- 3) A detailed comparison between traditional SRAMs and the proposed NVSRAM is conducted at the cell level as well as the circuit level.
- 4) Factor of merits including energy consumption, switching times during FORMING, RESET and SET operations, SNMs and area are extracted and analysed.

In section II, OxRAM technology is introduced and OxRAM variability is investigated. In section III, the design of the proposed NVSRAM is presented and compared with a traditional SRAM cell at the cell level. In section IV, projections at the memory array level are provided. In Section V, SRAM and NVSRAM performances are compared based on electrical simulations. In section VI, the impact of variability is investigated based on Monte Carlo (MC) simulations. Section VII presents some concluding remarks.

## II. OXRAM TECHNOLOGY

### A. Background

An OxRAM device consists of three layers including two metal electrodes and an insulator layer [34], structure known as Metal–Insulator–Metal (MIM) shown in Fig. 1(a). This device can be integrated in the Back End Of Line (BEOL) of CMOS technology as depicted in Fig. 1(b), presenting important benefits in term of area and data transfer latency.

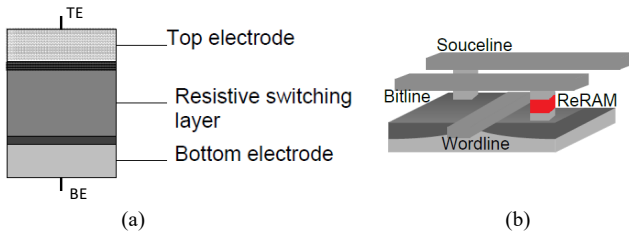


Fig. 1. (a) Basic RRAM structure and (b) its integration in the BEOL

Fig. 2 (a) and (b) show OxRAM I-V characteristic in linear and logarithmic scale respectively, extracted from actual OxRAM devices [27]. The first step in the OxRAM programming operation is FORMING where a high voltage is applied across the memory cell to switch the cell from HRS (high resistive state) to LRS (low resistive state). FORMING operation is performed once in the OxRAM device life. After FORMING, SET and RESET operations are executed by applying specific voltages on the electrodes of OxRAM cell

(i.e.  $V_{SET}$  and  $V_{RESET}$ ) [35]. Based on the linear curve presented in Fig. 2 (a), the  $V_{SET}$  value needed to switch to LRS state is equal to 0.57 V, while the  $V_{RESET}$  value required to switch back to HRS state is equal to -0.7 V [36, 37]. Note that log curve (Fig. 2 (b)) is the classical representation of the OxRAM I-V hysteresis as it amplifies low current values.

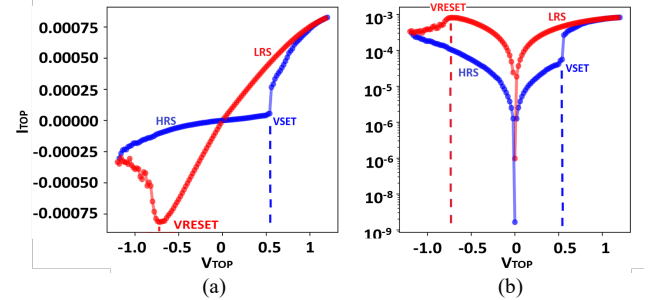


Fig. 2. I-V characteristic of an OxRAM cell in (a) linear and (b) log scale

### B. OxRAM Model

The OxRAM model approach used in this work (IM2NP model [27]) is based on the formation and destruction of oxygen vacancies by the induced electric field inside the insulator layer. The model is calibrated on silicon (130 nm technology from STMicroelectronics) with no convergence issues when used in combination with CMOS technology. Also, it is considered as one of the few models considering the FORMING operation, which is a crucial factor when targeting the fabrication of the devices. Moreover, the 130 nm technology provides High Voltage (HV) transistors needed for the FORMING operation.

As the OxRAM cells are integrated in the BEOL (on top of CMOS transistors), the performances of the proposed NVSRAM cell rely on the CMOS subsystem. If the performance in terms of speed and energy consumption is improved for advanced CMOS technology nodes (which is usually the case), it would be reflected in the NVSRAM performance. Regarding the area, it should be drastically reduced as the footprint of the transistors is reduced.

Fig. 3 depicts I-V characteristics for (a) SET, RESET and (b) FORMING operations measured on a large number of memory elements coming from [38-39]. A standard deviation of about  $\pm 5\%$  on selected parameters ( $\alpha$ : composition and  $L_x$ : local variations of thickness) enables satisfactorily accounting for the variability [27]. A modulation of  $\alpha$  impacts the creation/destruction kinetics of the conductive filaments (CFs) which introduces a variability in the programming voltage ( $V_{SET}$  &  $V_{RESET}$ ) and in the CF width. On the other hand,  $L_x$  variation impacts the current through the virgin oxide (i.e., post-FORMING current). The simulation data closely matches the measurement data as shown in Fig. 3, certifying the reliability of the model.

### C. OxRAM Variability

OxRAM devices suffer from a significant variability that can be divided into two categories, D2D and C2C variabilities [40]. The variability is demonstrated experimentally based on an elementary memory array. Fig. 4

(a) presents a classical 1T1R array which is used for experimental measurements. Memory cells are grouped to form eight 8-bit memory words. Word Lines ( $WL_X$ ) are used to select the active row, Bit Lines ( $BL_X$ ) are used to select active columns during a SET operation and Source Lines ( $SL_X$ ) are used to RESET a whole memory word or an addressed cell. Fig. 4 (b) presents the layout view of the memory array. Due to the limited pin out of the probe card used in the experimental phase, only a 7x7 memory array is available for our experiments (subset of the 8x8 array). Based on this elementary memory array, OxRAM variability is examined.

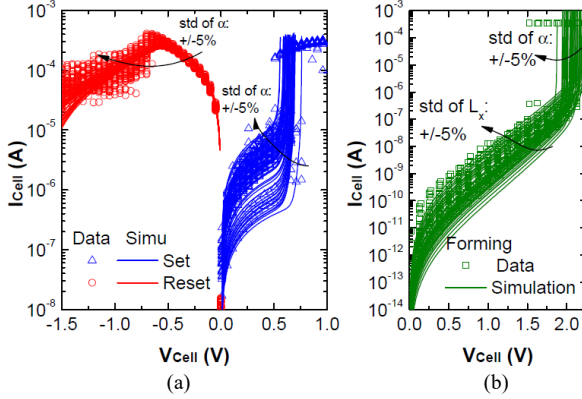


Fig. 3. Measured and corresponding simulated I-V characteristic showing LHS and HRS variations and switching parameters variation after (a) SET, RESET and (b) FORMING operations [28]

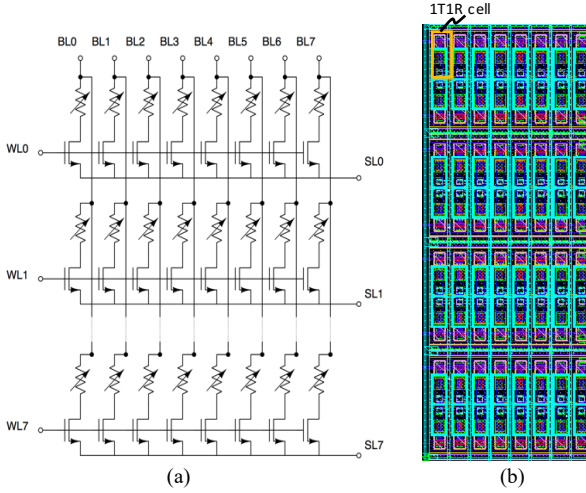


Fig. 4. (a) 8x8 OxRAM memory array and (b) corresponding layout view

Fig. 5 shows  $R_{ON}$  and  $R_{OFF}$  distributions combining C2C and D2D variabilities. Distributions are the result of 1000 consecutive RESET/SET operations applied to the whole memory array (1000x49 cells). HRS and LRS variability is clearly demonstrated and HRS distribution spread is more pronounced compared to the LRS spread, which is a common feature of the considered OxRAM technology. Hence, this drawback of the technology needs to be considered when designing OxRAM-based NVSRAMs. Indeed, in a NVSRAM context, variability can lead to a weak SET or RESET of the OXRAM when data is moved to the non-

volatile memory element. Moreover, the main problem that can occur is to RESTORE a false data after an extreme weak RESET operation (HRS post-RESET state located in the distribution tail). Table I presents the different voltage levels applied to the OxRAM cell during FORMING, RESET and SET operations. The whole experimental setup is based on a Keysight B1500 semiconductor parameter analyzer [41].

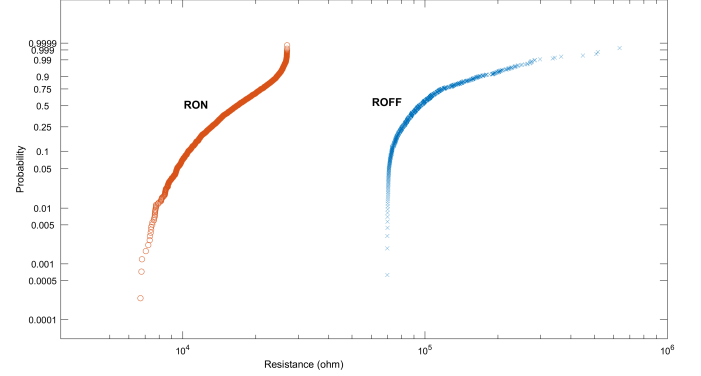


Fig. 5.  $R_{ON}$  and  $R_{OFF}$  distribution

TABLE I. STANDARD OPERATING VOLTAGES (CELL LEVEL)

	FORMING	RESET	SET	READ
WL	2V	4.5V	2V	4V
BL	2V	0V	1.2V	0.2V
SL	0V	1.8V	0V	0V

### III. CELL LEVEL : SRAM & NVSRAM

A NVSRAM cell is formed by the combination of a SRAM cell and an OxRAM memory device where some SRAM nodes are connected to the OxRAM cells. This structure allows backing up data from the SRAM to the OxRAM in the standby mode while the SRAM classical operations (i.e. HOLD, WRITE and READ operations) are maintained in the normal operating mode.

#### A. 6T SRAM memory cell

The 6T SRAM memory cell is the classical SRAM structure based on the cross coupled inverters presented in Fig. 6. HOLD, READ and WRITE are the main operations in an SRAM [42]. These operations are performed through Word Lines (WLs) and Bit Lines (BLs). WLs are connected to the gates of the select transistors (M3 and M4), and BLs are connected to the select transistor sources/drains. During the HOLD stage, BLs are disconnected from the SRAM core by deactivating the WLs. Data nodes Q and  $Q_b$  retain the data. READ and WRITE operations are completed by activating WL to sense or update the stored data respectively. Fig. 7 shows the 6T SRAM cell layout implemented in a 130 nm technology, with an area occupancy equals to  $34 \mu m^2$ .

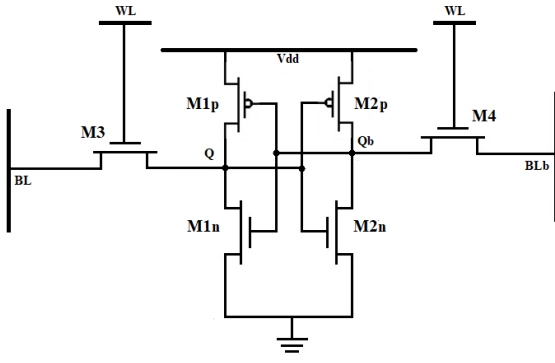


Fig. 6. 6T SRAM cell

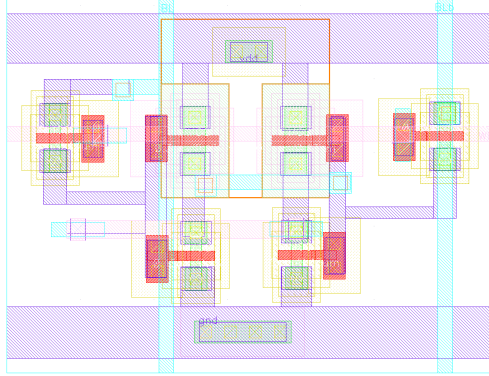


Fig. 7. 6T SRAM Cell layout

#### B. 8T1R NVSRAM memory cell

The proposed 8T1R structure is depicted in Fig. 8. The sizing of the transistors is as follow: M1n and M2n ( $w=150$  nm), M1p and M2p ( $w=450$  nm). M3, M4, M5 and M6 (900 nm). Note that the length of all transistors is fixed (130 nm). The top electrode (TE) of the OxRAM device is connected to transistor M5 and the bottom electrode (BE) to the node Qb. In this structure, transistors (M3 and M4) represent the access transistors and transistors (M5 and M6) are used for the non-volatile storage operations referred to as STORE and RESTORE. STORE consists of two operations: OxRAM SET (stores “1”) and OxRAM RESET (stores “0”).

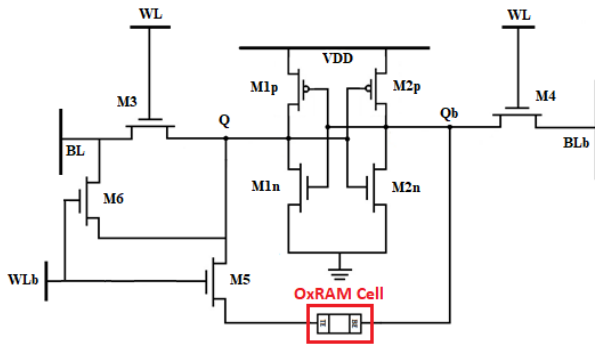


Fig. 8. 8T1R NVSRAM Cell

Before any STORE/RESTORE operation, the OxRAM cell needs to be formed. Forming is achieved in one step where WL and BL<sub>b</sub> are set low and BL and WL<sub>b</sub> are set high, allowing a direct connection between BL and the OxRAM though transistors M5 and M6. BL is set to 5 V while BL<sub>b</sub> is grounded and the OxRAM access transistors (M5 and M6) are controlled by applying a pulse to WL<sub>b</sub>. After Forming, the STORE operation has to be preceded by a WRITE operation. In this regard, WRITE “0” comes before STORE “0” (RESET) and WRITE “1” comes before STORE “1” (SET). During WRITE “0” operation, WL and BL<sub>b</sub> are set high, BL and WL<sub>b</sub> are set low. On the other hand, BL is set high and BL<sub>b</sub> is set low during WRITE “1” operation. During STORE, WL<sub>b</sub> is set high and WL is set low to access the OxRAM cell for programming: BL is set low and BL<sub>b</sub> is set high during STORE “0” (RESET), besides BL is set high and BL<sub>b</sub> is set low during STORE “1” (SET). Note that STORE and WRITE operations are independent as WRITE operations (normal operation) are executed separately from the STORE operations (RRAM programming).

Before a READ operation, a Precharge of the BLs is needed where BL and BL<sub>b</sub> are set to V<sub>DD</sub> (1.8V). Then, WL is set high to READ the cell. After STORE (OxRAM SET or RESET), V<sub>DD</sub> is turned OFF. During RESTORE, V<sub>DD</sub> is activated and WL<sub>b</sub> is set high (all the other signals are kept low) to recover the stored data. Fig. 9 shows the 8T1R NVSRAM cell layout with an area equals to 53  $\mu\text{m}^2$ . This novel memory cell is characterized by its low number of control signals compared to NVSRAMs proposed in [43-45, 20].

Table II illustrates the advantages and drawbacks of different NVSRAMs proposed in the literature in terms of STORE/RESTORE time, RESTORE method, non-volatility, STORE/RESTORE energy, and silicon verification. There are 2 types of RESTORE methods: single-ended and differential (diff.). In the single-ended topology, one OxRAM cell is used, where in the differential topology, two OxRAM cells are used. Another factor is the type of NVSRAM non-volatility.

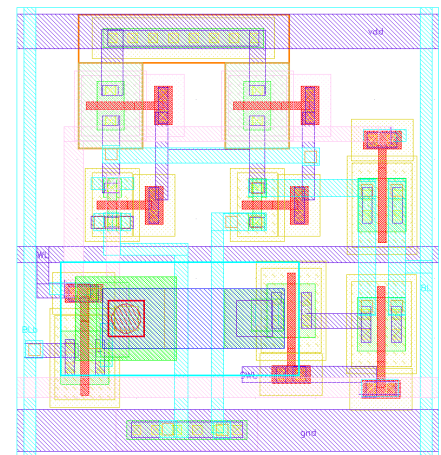


Fig. 9. 8T1R NVSRAM Cell layout

TABLE II. COMPARISON AGAINST DIFFERENT NVSRAM DESIGNS

	4T2R [19]	7T1R [20]	8T2R [43]	7T2R [44]	8T2R [45]	8T1R
<b>STORE Time</b>	1.45 ns	3 ns	3 ns	12.6 ns	10 ns	6.8 ns
<b>RESTORE Time</b>	20 ps	0.22 ns	0.22 ns	0.37 ns	0.36 ns	0.45 ns
<b>RESTORE Method</b>	Diff.	Single-ended	Diff.	Diff.	Diff.	Single-ended
<b>Non-Volatility</b>	Real-time	Last-bit	Last-bit	Last-bit	Last-bit	Last-bit
<b>STORE Energy</b>	594 pJ	36 pJ	121 pJ	218 pJ	194 pJ	176 pJ
<b>RESTORE Energy</b>	30 fJ	50 fJ	80 fJ	0.25 fJ	0.52 fJ	81 fJ
<b>FORMING Energy</b>	1.7 nJ	0.35 nJ	0.77 nJ	1 nJ	6.345 nJ	2.5 nJ
<b>Silicon Verified</b>	No	No	No	Yes	Yes	No

For example, some NVSRAM cells offer real-time non-volatility where the data is stored after every WRITE operation but at the expense of higher power consumption (Real-time). On the contrary, other NVSRAM cells follow the last-bit non-volatility where the data is stored just before shutdown (Last-bit).

STORE energy (hundreds of pJ for most of the NVSRAM cells) is the result of a programming operation. Whereas, the RESTORE operation is a sensing operation requiring less energy (order of tens pJ) and shorter READ pulses. Minimal STORE times are in the range of 1-10 ns (6.8 ns for the proposed 8T1R cell) and minimal reported RESTORE times are less than 1 ns (0.45 ns for the proposed 8T1R cell). Timing and energy requirements are dictated by the targeted application. When dealing with ultra-low power applications, timing is not an issue (i.e., can be relaxed) but STORE/RESTORE energies need to be lowered. Moreover, the number of STORE/RESTORE operations following power interruptions is application dependent. If power interruptions are frequent, a good balance between timing and energy can be required. Alternatively, parameters such as area and NVSRAM cell complexity (number of control signals and RESTORE method) play an important role when low-cost applications are targeted.

#### IV. MEMORY ARRAY LEVEL

In this section, a conventional SRAM memory array is designed and compared with our proposed NVSRAM array. Both arrays follow the same architecture. However, the NVSRAM array requires some additional blocks to complete the non-volatile operations.

##### A. SRAM Array Design

In a SRAM array, SRAM cells are arranged to share connections in horizontal rows and vertical columns. In this work, an elementary 4x8 bytes memory array presented in Fig. 10 is proposed with a total size of 256 cells. The horizontal lines are the WLs, while the vertical lines along which data flow into and out of cells are the BLs. To access a cell for READ and WRITE operations, a specific row and

column are selected [46]. The memory array is associated with peripheral circuits as illustrated in Fig. 10. Word decoder and column decoder select WL and BL consecutively, based on the provided address. Note that the column decoder controls numerous peripheral circuits including precharge circuits, column multiplexers, sense amplifiers and write drivers. Write drivers deliver the logic states to an addressed memory word. The BLs are connected to the precharge circuits. Also, BLs are connected to the write drivers and to the sense amplifiers to complete WRITE and READ operations, respectively.

During WRITE operation, data inputs are fed directly to the write drivers. The row decoder controls the selection of WLs, thus addressing the targeted row. The column decoder is used to select a group of columns, where the programming operations are executed. The column multiplexer role is to connect the sense amplifier to the BLs and disconnect the precharge circuit and write driver circuit to ensure that READ operation is completed properly. Before READ, the precharge circuit increases BL voltage to  $V_{DD}$  or  $V_{DD}/2$ . READ operation is initiated by enabling SE signal [47]. Fig. 11 presents the 4x8 bytes SRAM array layout.

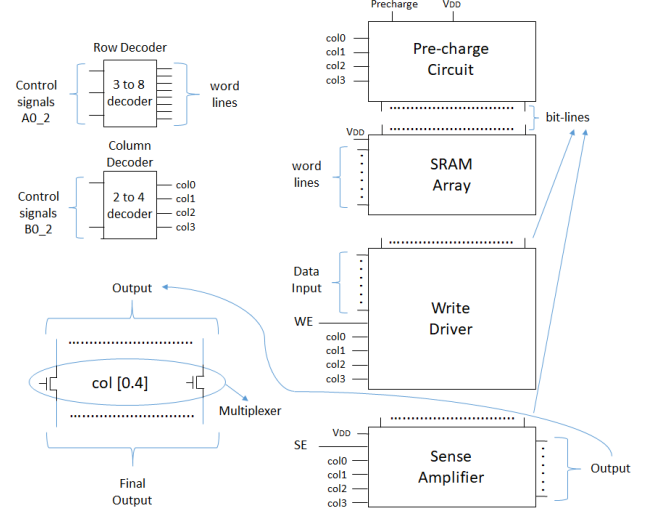


Fig. 10. SRAM Array Design

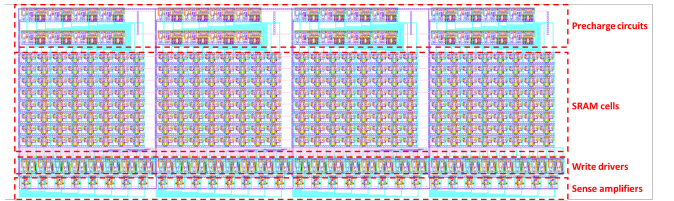


Fig. 11. Layout of 4x8 bytes SRAM array

Fig. 12 represents SRAM Finite State Machine (FSM) diagram. In this diagram, there are four different states (IDLE, Precharge, READ and WRITE), and two control signals (reset and RW). When the state is "IDLE" and "reset = 1", the FSM maintains its current state. "IDLE" state moves to "Precharge" state when "reset = 0" and moves back to "IDLE" when "reset = 1". The next state after "Precharge" is

“READ” or “WRITE”, if “RW = 0” and “RW = 1” respectively. “WRITE” and “READ” states move to “IDLE” state, when “reset = 1”. Note that if no control signal is activated, “WRITE” and “READ” states go back to “Precharge”. The complete SRAM array structure including the FSM block is shown in Fig. 13 (a). The structure inputs are the clock, the address bus, the data bus, and control signals. Fig. 13 (b) shows SRAM memory map with the address bus LSB and MSB bits.

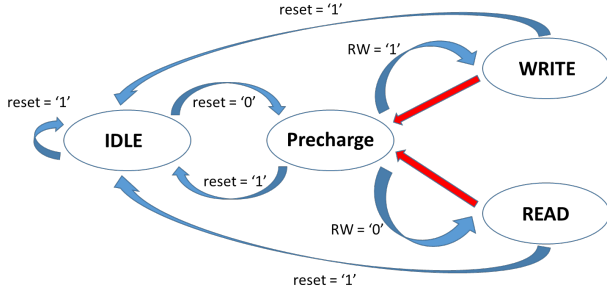


Fig. 12. SRAM Finite State Machine Diagram

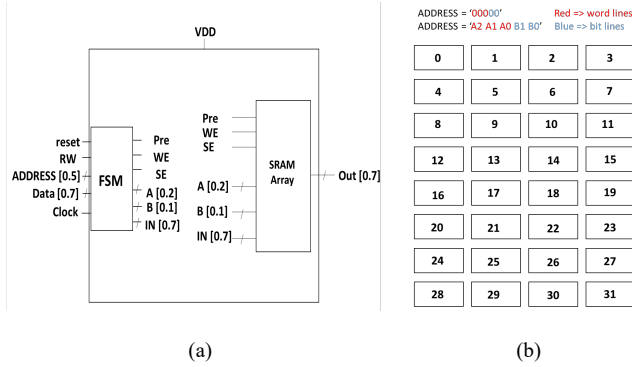


Fig. 13. (a) Complete SRAM array structure with FSM circuitry (b) SRAM address distribution

### B. NVSRAM Array Design

The proposed NVSRAM array structure is adjusted to the 8T1R cell presented in Fig. 8 which is the core cell of the memory array. The design includes all the peripheral circuits associated with a classical memory array with some marginal modifications as illustrated in Fig. 14. Additional logic circuits are added to handle the STORE (SET & RESET) and RESTORE operations. Note that,  $WL_b$  has its own decoder to have a direct control over the STORE operations. Fig. 15 presents the 4x8 bytes NVSRAM array layout.

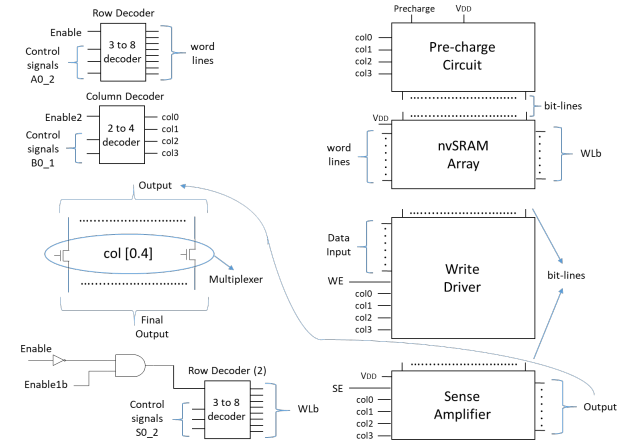


Fig. 14. NVSRAM Array Design

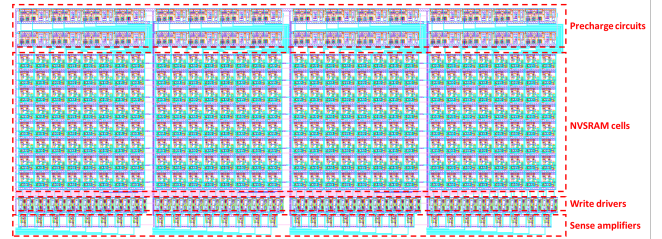


Fig. 15. Layout of 4x8 bytes NVSRAM array

Fig. 16 represents NVSRAM FSM diagram. In this diagram, three additional states (FORMING, STORE and RESTORE), and two additional control signals (FORMING control (Fc) and STORE control (Sc)) are available compared to the FSM associated with a classical SRAM array. In all, seven states and four internal signals are needed. When the state is “IDLE” and “reset = 1”, the FSM maintains its current state. “IDLE” state moves to “Precharge” state when “reset = 0 & Sc = 1”, and to “RESTORE” state when “reset = 0 & Sc = 0”. Proceeding to “READ” and “WRITE” states, “Fc = 0 & RW = 0” and “Fc = 0 & RW = 1”, respectively. To end up in “FORMING” state, “Fc = 1. After “WRITE”, the FSM can move to the “STORE” state where “reset = 0 & Sc = 1”. All states move to “IDLE”, when “reset = 1”. The complete NVSRAM array structure with the added FSM block is shown in Fig. 17 (a). The NVSRAM circuit inputs signals are the clock, the address bus, the data bus, and the FSM control signals. Fig. 17 (b) shows the NVSRAM memory map with the address bus LSB and MSB bits.

## V. SIMULATION RESULTS AND COMPARISON

SRAM and NVSRAM simulations results are proposed in this section at the memory array level. Voltage pulses levels for programming operations are set to be compliant with the available voltage supplies (1.8 V, 3.3 V and 5 V).

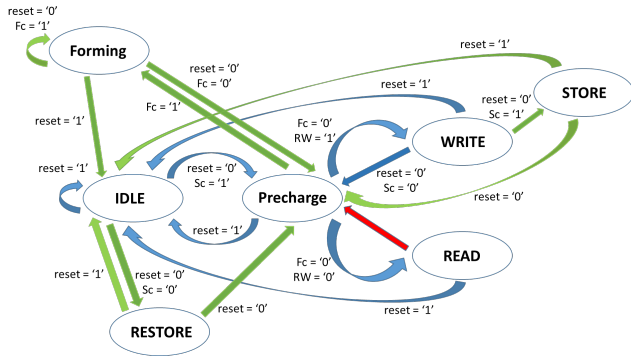


Fig. 16. NVSRAM Finite State Machine Diagram

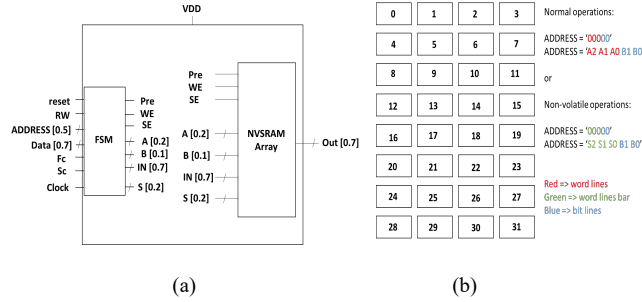


Fig. 17. (a) Complete NVSRAM array structure with FSM circuitry (b) NVSRAM address distribution

#### A. SRAM array simulation results

Based on the simulation of the circuit presented in Fig. 13 (a), the internal signals (FSM outputs) Pre, WE, SE, A, B, and IN have been extracted. These signals are presented in Fig. 18 and Fig. 19. Fig. 18 presents the row and column decoder inputs and outputs during the following set of operations: Precharge – WRITE – HOLD – Precharge – READ. When A0 and A1 signals of the row decoder are set high, WL3 is selected. For the column decoder, when B0 is high and B1 is low, col1 is selected.

The SRAM array timing waveforms are presented in Fig. 19. The precharge circuit is first activated (Precharge signal is set to “0”). Write drivers and sense amplifiers controlled respectively by WE and SE signals are deactivated. In this stage, the row decoder is OFF, as the memory cells are not selected, and the column decoder is turned ON to select the BLs to be precharged. During WRITE, the precharge circuit is disabled (Precharge is set to “1”), and the sense amplifier circuit is OFF (SE = “0”). Write driver is turned ON (WE = “1”), and the row decoder is enabled to access the addressed cells. During HOLD state, all the signals are turned OFF (except V<sub>DD</sub>) to maintain the data in the cross coupled inverters. HOLD operation is followed by Precharge to initiate a READ operation. During READ, precharge and write driver circuits are turned OFF. The column decoder connects the BLs to the selected sense amplifiers. The output (out = “0”) and (out = “1”) are the result of WRITE “0” and WRITE “1” operations, respectively.

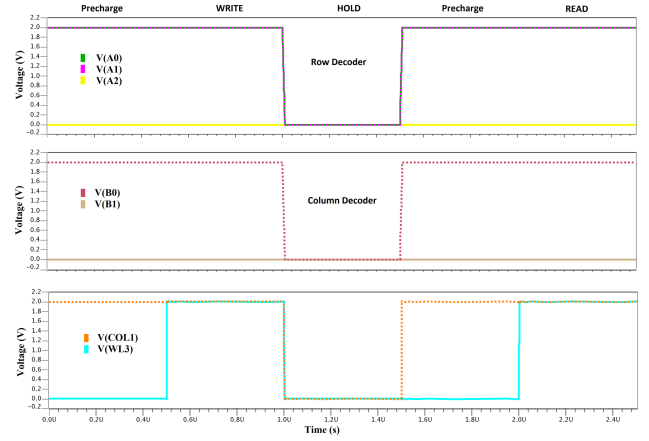


Fig. 18. Decoder Control Signals

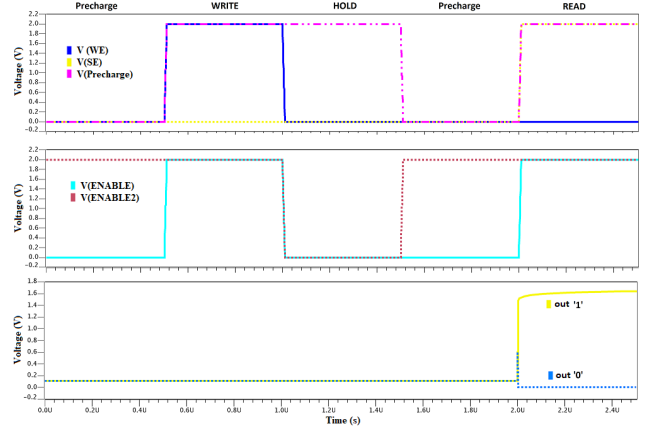


Fig. 19. SRAM array timing waveforms

#### B. 8T1R memory array simulation results

Based on the simulation of the circuit presented in Fig. 17 (a), Pre, WE, SE, A, B, IN and S have been extracted. These signals are presented in Fig. 20 and Fig. 21. The decoders control signals are presented in Fig. 20. All signals of the row decoder are set high to select WL7 row. For the column decoder, all signals are set high to select col3 column.

The timing waveforms of the NVSRAM array simulation are presented in Fig. 21. Precharge and WRITE “1” operations precede the FORMING stage. During WRITE “1”, the precharge circuit and the sense amplifier are OFF (Precharge = “1” & SE = “0”). The write driver is enabled (WE = “1”) and the data bus is set to “0xAA”. Also, the second row decoder that control WL<sub>b</sub> is set ON (ENABLE1b = “1”, see Fig. 14). After FORMING, a WRITE operation is executed after Precharge. During STORE operation, most of the peripheral circuits (precharge circuit, write driver, sense amplifier, and row decoder) are disabled. Moreover, the column decoder is kept high (ENABLE2 = “1”) and the second row decoder (WL<sub>b</sub>) is enabled (ENABLE1b = “1”) to access the OxRAM cell. The next stage is a Precharge followed by a READ operation where the output signal (out) is sensed according to the data bus values (“0” or “1”). During the “OFF” state V<sub>DD</sub> is set to 0. After power ON, the

RESTORE operation is performed to recover the data on nodes Q and Q<sub>b</sub> of the NVSRAM cell. During this operation, the power supply V<sub>DD</sub> is enabled allowing the current to pass through the OxRAM cell to the data nodes. After RESTORE, a second Precharge and READ operations are executed to check that the data restored matches the initial data. Regarding the recovery time (time needed to obtain a stable logical value after power-on), according to Fig. 21, its nominal value can be evaluated to 500 ns.

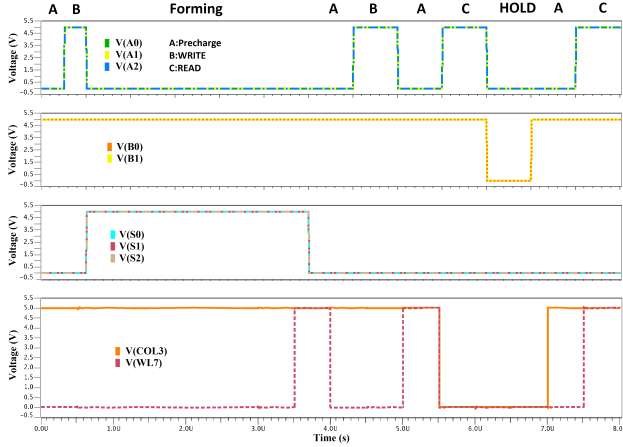


Fig. 20. Decoders Control Signals

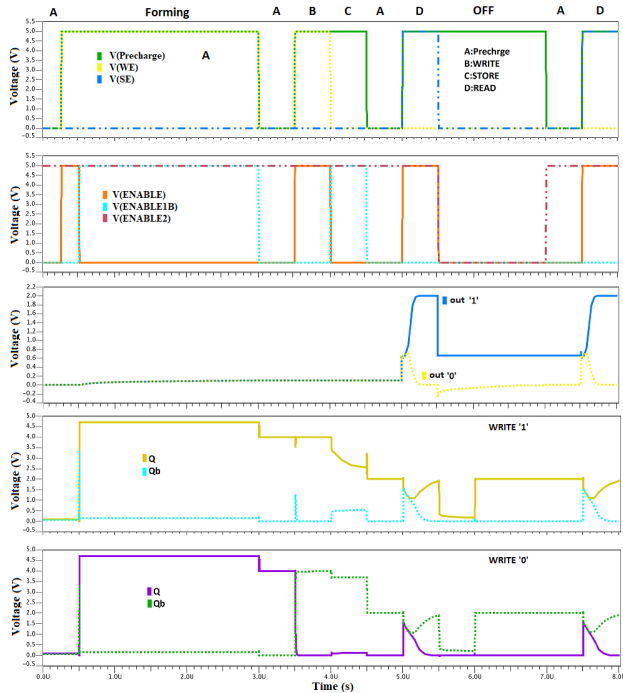


Fig. 21. NVSRAM array timing waveforms

### C. Comparison

Table III shows a comparison between SRAM and NVSRAM circuits in term of energy consumption, area, switching time, and SNM. The NVSRAM array has a slightly higher energy consumption (2.6%) when used in normal operations. The data of the NVSRAM cells is stored in the

OxRAM devices before the “OFF” state. This sequence requires specific programming operations to be completed (STORE before and RESTORE after power down). During HOLD state, V<sub>DD</sub> is kept high to ensure the data is retained. The energy consumption of both arrays in this state is around 38 pJ, since the OxRAM device does not interfere in the normal operations (SRAM mode).

The area of the SRAM and NVSRAM arrays is 18979  $\mu\text{m}^2$  and 25775  $\mu\text{m}^2$ , respectively. Hence, the area of NVSRAM array is 34.9% larger compared to the SRAM array. The layouts of SRAM and NVSRAM have similar structure since both rely on the same design for the peripheral circuits. However, since the SRAM array has lower number of transistors and does not embed resistive memory elements, its area is much smaller than the one of the NVSRAM array.

SRAM stability is conventionally defined by the SNM [45] which is the maximum value of the DC noise voltage that can be tolerated by the SRAM cell without altering/flipping the stored bit. Stability is the most important criterion in the design of an SRAM as it guarantees that the SRAM cell can hold its data under READ and HOLD conditions. In practice, the smallest square between the voltage transfer characteristics (VTCs) of the two inverters is used to graphically determine the SNM [48]. The nominal SNMs of the considered SRAM cell is 704 mV, 180 mV and 864 mV during HOLD, READ and WRITE states, respectively. Similarly, the nominal SNMs of the NVSRAM is 605mV, 150 mV and 795 mV during HOLD, READ and WRITE states, respectively. The smaller READ SNM of the NVSRAM cell (16.67% lower compared to the SRAM) shows that the cell is more vulnerable to data corruption during a READ operation. Write Margin (WM) is defined as the BL<sub>b</sub> value when nodes Q and Q<sub>b</sub> flip. The lower that value is, the harder it is to write the cell, implying a smaller write margin. The WM nominal value is 670 mV for the SRAM and 605 mV for the NVSRAM.

To gain non-volatility, the area is compromised (+34.9%) as well as some performance parameters such as SNMs and WM (8 to 17% loss). As already mentioned, the choice of moving from a classical SRAM to a NVSRAM is application dependent. For low-cost applications, a 35 % increase in the area can be problematic. However, for ultra-low power applications, the area overhead can be justified.

TABLE III. COMPARISON BETWEEN SRAM AND NVSRAM ARRAYS

	SRAM	NVSRAM	Difference (%)
Energy Consumption (Normal operations)	13.64 nJ	14 nJ	+2.6%
Energy Consumption (HOLD)	38.34 pJ	38.34 pJ	-
Area (4x8 bytes)	18765 $\mu\text{m}^2$	25312 $\mu\text{m}^2$	+34.9%
Nominal SNM (HOLD state)	704 mV	605 mV	-14%
Nominal SNM (READ state)	180 mV	150 mV	-16.67%
Nominal SNM (WRITE state)	864 mV	795 mV	-8%
Write Margin (WM)	670 mV	605 mV	-10.7%

Table IV shows NVSRAM specific operation results at the array level. The nominal energy consumption of the NVSRAM is 2.5 nJ, 280 pJ and 72 pJ during FORMING, RESET and SET operations, respectively. Moreover, The nominal switching time is 5.6 ns, 8 ns and 500 ns for RESET, SET and FORMING, respectively.

TABLE IV. NVSRAM SPECIFIC OPERATIONS

Nominal FORMING Energy	2.5 nJ
Nominal SET Energy (STORE “1”)	72 pJ
Nominal RESET Energy (STORE “0”)	172 pJ
Nominal FORMING Switching Time	500 ns
Nominal SET Switching Time	8 ns
Nominal RESET Switching Time	5.6 ns

## VI. IMPACT OF VARIABILITY ON NVSRAM METRICS

In this section, MC simulations are performed to evaluate the impact of OxRAM combined with CMOS variability on the NVSRAM performances. For the OxRAM, only actual variation are reported as the OxRAM model is calibrated on silicon. For the CMOS subsystem, on each simulation run, the MC analysis calculates every parameter randomly according to statistical distribution models. These statistical models are provided for active devices (MOSFETs) as well as for passive devices and cover corner cases. Fig. 22 shows the energy distributions resulting from 1000 MC simulation runs after FORMING, RESET and SET operations. As expected, the energy consumption during FORMING is considerably high compared to SET and RESET operations. If we consider the distribution medians, the average energy consumptions are 2.5 nJ, 280 pJ and 72 pJ after FORMING, RESET and SET operations, respectively. High voltage programming pulses are required during FORMING and RESET, which leads to higher power consumption in both operations compared to SET. Note that a large energy is required during FORMING due to the large initial resistance of OxRAM cell which is in the pristine state. The voltage pulse level applied during FORMING is 5 V compared to 3.3V and 1.8V for RESET and SET operations, respectively. Hence, FORMING energy consumption is 8.9x and 34.7x higher than RESET and SET operations, respectively. Also, the energy consumption during RESET operation is 3.8x higher than that recorded during the SET operation.

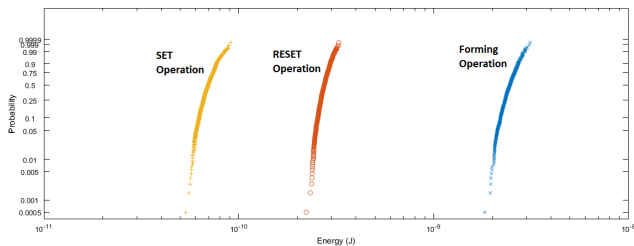


Fig. 22. MC simulations results for energy consumption during FORMING, SET and RESET operations

Fig. 23 shows the switching time distributions from 1000 MC simulations runs after FORMING, RESET and SET operations. The switching time needed for the FORMING operation is significantly high compared to SET and RESET operations.

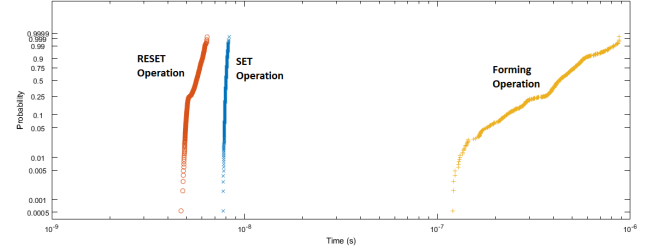


Fig. 23. MC simulations results for switching time during FORMING, SET and RESET operations

If we consider the distribution medians, the switching time average is 5.6 ns, 8 ns and 500 ns for RESET, SET and FORMING, respectively. Compared to SET (0.6 ns) and RESET (1.7 ns) switching time dispersion, larger programming pulses are required for FORMING operation in order to cover its large switching time dispersion (770 ns). It is worth noting that the magnitude of the voltage pulse directly affect the switching time of the NVSRAM STORE operation (SET and RESET). The higher the programming pulse, the shorter the switching time.

SNM stability criteria is also evaluated after 1000 MC runs to assess the cell stability of the NVSRAM. Fig. 24 (a), (b), and (c) show simulated results of the 8T1R NVSRAM cell. HOLD, READ, and WRITE SNM (denoted by HSNM, RSNM, and WSNM, respectively) are considered. These plots present the best and worst SNM cases (highlighted in black) based on the 1000 MC runs (gray lines). During the HOLD operation, HSNM varies between 560 mv and 650 mv. During the READ operation, RSNM varies between 120 mv and 180 mv. Based on the butterfly curves of Fig. 24(c), it is observed that the process variations have negligible effect on the WSNM. In this regard, WSNM is equal to 790 mv in the worst case and 800 mv in the best case. Table V summarizes SNM best and worst cases for HOLD, READ, and WRITE. Additionally, the success rate of data recovery is 100% as after the 1000 MC runs, the proposed NVSRAM was able to restore the saved data.

As the main driving force when moving from SRAMs to NVSRAMs is the targeted application, the best and worst case SNM values are valuable information if the reliability criteria is considered. For instance, worst case SNMs can prevent the use of NVSRAMs in spatial or smartcard applications.

TABLE V. SNM BEST AND WORST CASES

	Best Case	Worst Case
SNM (HOLD)	650 mV	560 mV
SNM (READ)	180 mV	120 mV
SNM (WRITE)	800 mV	790 mV

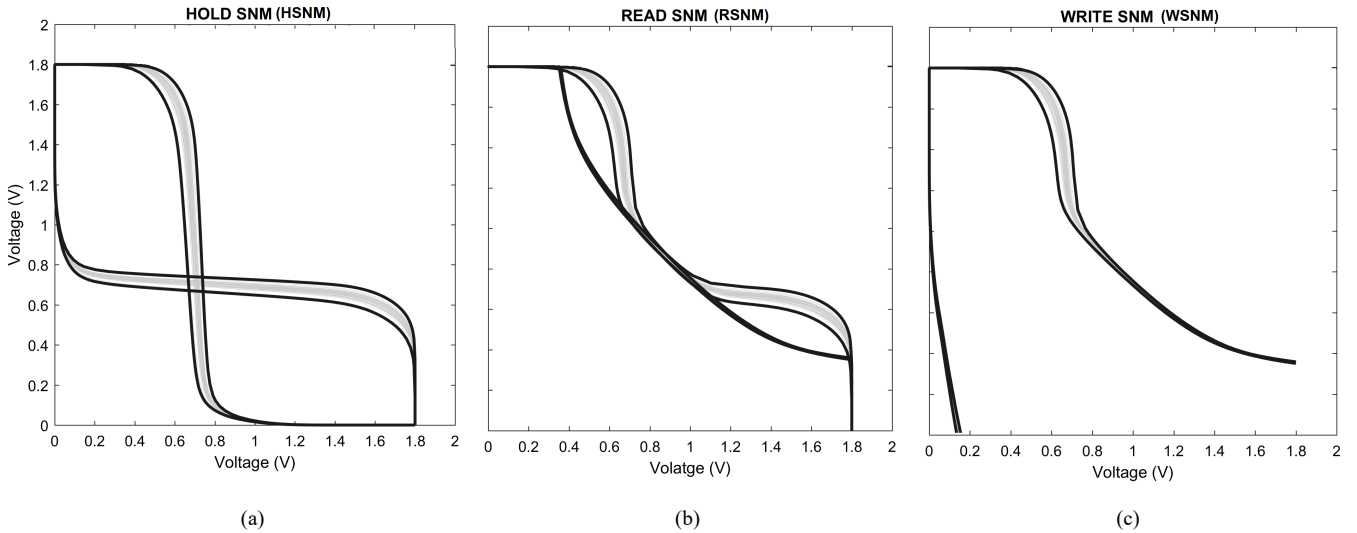


Fig. 24. (a) HOLD SNM (HSNM), (b) READ SNM (RSNM), and (c) WRITE SNM (WSNM)

## VII. CONCLUSION

This paper advances the state-of-the-art of NVSRAM stability analysis by investigating the impact of OxRAM and CMOS variability on a novel 8T1R NVSRAM cell. The proposed 8T1R NVSRAM cell can be used in SRAM mode with classical HOLD, WRITE and READ operations. Also, this structure exhibits additional operations in non-volatile mode such as STORE and RESTORE. A comparison with a classical 6T SRAM is provided considering metrics such as area, energy consumption and SNMs. We demonstrated that a NVSRAM array is non-volatile but at the cost of larger area (34.9%), and higher power consumption (2.6%). This array can be kept in power OFF mode, which is useful for ultra-low power applications.

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## DATA AVAILABILITY STATEMENT

Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

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