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Hot-carrier evaluation of a zero-cost transistor developed via process optimization in an embedded non-volatile memory CMOS technology

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Abstract

A new transistor architecture is developed by reusing already existing fabrication process bricks in an embedded non-volatile memory (eNVM) sub-40 nm CMOS technology, resulting in a middle-voltage zero-cost transistor, ideal for low-cost products. TCAD simulations are undertaken to confirm the feasibility of the process optimization and predict the transistor performance and reliability. The new transistor is fabricated then electrically characterized. The new device shows good analogue performances for no cost added. A hot-carrier injection (HCI) degradation evaluation is performed and confirms the reliability of the device.

Keywords

Transistor, MOSFET, CMOS, zero-cost, analogue, middle-voltage, hot-carrier, HCI, reliability

1. Introduction

In low-cost and high-volume products, such as smartcards and Internet of Things (IoT) devices, low-cost transistor architectures are highly desirable [1]. An ideal CMOS technology contains a multitude of transistor architectures, each one addressing different voltage ranges, with adjusted implants, oxide thicknesses, and spacers (Fig. 1a). A small transistor is used for digital areas, a larger one for input/output (IO) functions. With embedded Non-Volatile Memory (eNVM), it is even more complex, as specific transistors are needed to handle memory-related High-Voltage (HV) operations [2]. This leads to a high number of photomasks, and dedicated process steps for each device, increasing the cost of the technology.

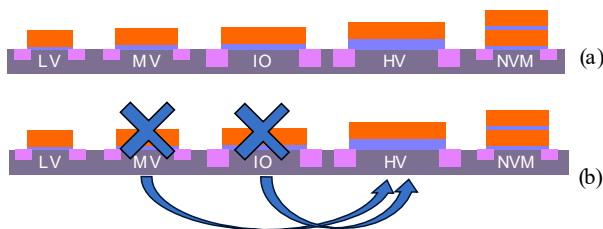


Fig. 1 – (a) Device architectures used in a standard eNVM technology. (b) Reduction of the number of Device architectures in a low-cost eNVM technology.

To minimize the cost of a technology, the number of process steps and photomasks must be reduced. Consequently, only a small subset of the different transistor architectures presented in Fig. 1a are used. In the targeted sub-40 nm eNVM low-cost technology, a single HV transistor architecture is used as an alternative to the IO and Middle-Voltage (MV) transistors for all circuit designs that need to withstand a voltage higher than the one supported by the Low-Voltage (LV) digital transistor, as shown in Fig. 1b. This approach is not optimized, as HV transistors are designed firstly to withstand high-voltages, and not necessarily to have good analogue performances, or to provide the smallest silicon footprint. Thus, there is a need for a “zero-cost” device to address the MV range (between 3 and 5 V), which is often neglected in favour of LV or HV transistors in low-cost technology.

In this work, we investigate the possibility of reusing already existing process bricks (oxide, implants, spacers), to build a new zero-cost transistor for the MV range that have better analogue performances compared to the HV transistor. In section 2 the proposed zero-cost process optimization is presented. TCAD simulation of the new transistor is undertaken, including transistor performance and reliability prediction. The results are presented in section 3. In section 4 the newly fabricated MV transistor is electrically characterised and compared to the existing HV transistor. Finally, hot-carrier injection (HCI) stress tests of the transistors are performed and presented in section 5.

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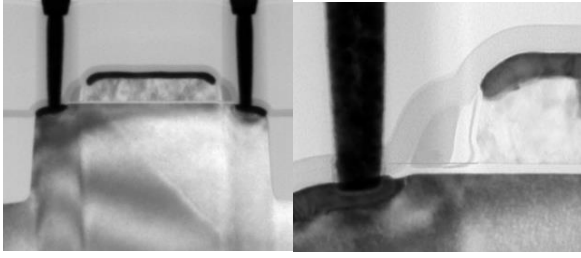


Fig. 2 – Transmission Electron Microscopy (TEM) images of the new MV device

2. Presentation of the new transistor architecture

The new MV transistor reuses most of the process steps of the available HV device, which is engineered to withstand voltages up to 10 V on its source, drain and gate. For that, a thick gate oxide, large spacers, anti-punch-through well implants and large lightly-doped-drain (LDD) implants are used. These process features are relevant when dealing with high-voltage, but not necessarily optimized for low or middle-voltage. Compared to the classical HV transistor, our new MV device uses a thinner oxide, that already serves as a tunnel oxide in the eNVM available in the technology. Fig. 2 shows the Transmission Electron Microscopy (TEM) images of our new MV device.

The gate oxide thickness is reduced by 40 %, which has the immediate effect of increasing the gate capacitance C_{OX} , thus lowering the threshold voltage V_T , and increasing the saturated drive current I_{ON} . Those effects are highly desirable for analogue applications. On the other hand, the gate oxide thickness reduction is usually accompanied by a higher OFF-state leakage current I_{OFF} . An enhancement of the transistor matching parameter A_{VT} is also predicted, since it is known to be proportional to the gate oxide thickness [3, 4].

3. TCAD simulation

Technology Computer Aided Design (TCAD) simulations are performed to verify the feasibility of the fabrication process, to predict the electrical characteristics of the new transistor, and the expected performance gains compared to the HV transistor. Two-dimensional static simulations are made using the Synopsys Sentaurus TCAD suite [5, 6]. During electrical behaviour simulation, the electrostatic potential is modelled using the Fermi-Dirac statistic. The drift-diffusion model is used to model the carrier transport. Mobility is modelled using the Philips unified mobility model (PhuMob) [7]. Shockley-Read-Hall (SRH) recombination is taken into account, including doping and electric field correction. Finally, avalanche generation (impact ionisation) is modelled using the new University of Bologna impact ionization model (UniBo2) [8].

3.1. Device performance metrics

Important device parameters are the linear and saturated threshold voltages V_{T-LIN} and V_{T-SAT} , measured at a fixed constant drain current I_D equal to 100 nA multiplied by the polysilicon gate width/length ratio W/L , and with a drain-source voltage V_{DS} equal to 0.1 V and 3.3 V, respectively. We are particularly interested in the variations of these parameters with the gate length L of the device, as it can highlight Short Channel Effects (SCE) [9]. We will also study the ON-state saturated drain current I_{ON} at a V_{DS} and gate-source voltage V_{GS} both of 3.3 V, and the OFF-state leakage current I_{OFF} at a V_{DS} of 3.3 V. Finally, we will examine the drain-source breakdown voltage $B_{V_{DS}}$, defined as the V_{DS} value for which I_D is equal to 1 nA, with the source, gate and bulk grounded.

3.2. Fabrication process TCAD simulation

The first stage of the TCAD simulation is the fabrication process simulation. The fabrication steps such as photolithography, etching, deposition, implantation, oxidation are simulated using physical equations modelling these phenomena, along with the layout sketch of the device's structure. The device is discretized (meshed) into a finite element structure. Fig. 3a shows TCAD simulation results for the new MV transistor, with a gradient colourmap of the doping concentration. The comparison of the TCAD snapshots with the TEM pictures of Fig. 2 confirms the good agreement between the TCAD simulation and the actual fabrication process.

3.3. Electrical behaviour simulation

The second stage of TCAD simulations is the electrical behaviour simulation of the transistor. This operation takes as input the meshed device generated by the fabrication process simulation. The simulator solves at each mesh point the fundamental physical equations describing the device operation, such as the electrical transport equations. By applying the same voltages used during electrical device characterisation and presented in section 3.1, TCAD simulation can predict the performance of our new MV transistor compared to the HV device.

The threshold voltages V_{T-LIN} and V_{T-SAT} of the HV and the new MV device have been simulated for different gate lengths (L) ranging from 0.5 to 10 μm , with a width (W) of 10 μm . The results for NMOS are shown in Fig. 3b. These results confirm the expected V_T drop associated with thinner gate oxide, close to a rigid curve shift. The V_T curve of our new MV device is in an interesting range above 200 mV. This value is low (good for analogue applications) but high enough to account for the decrease in V_T with temperature, as the transistor should still have a positive V_T at 125 °C. For V_{T-SAT} (dark blue in Fig. 3b, TCAD and measurements are

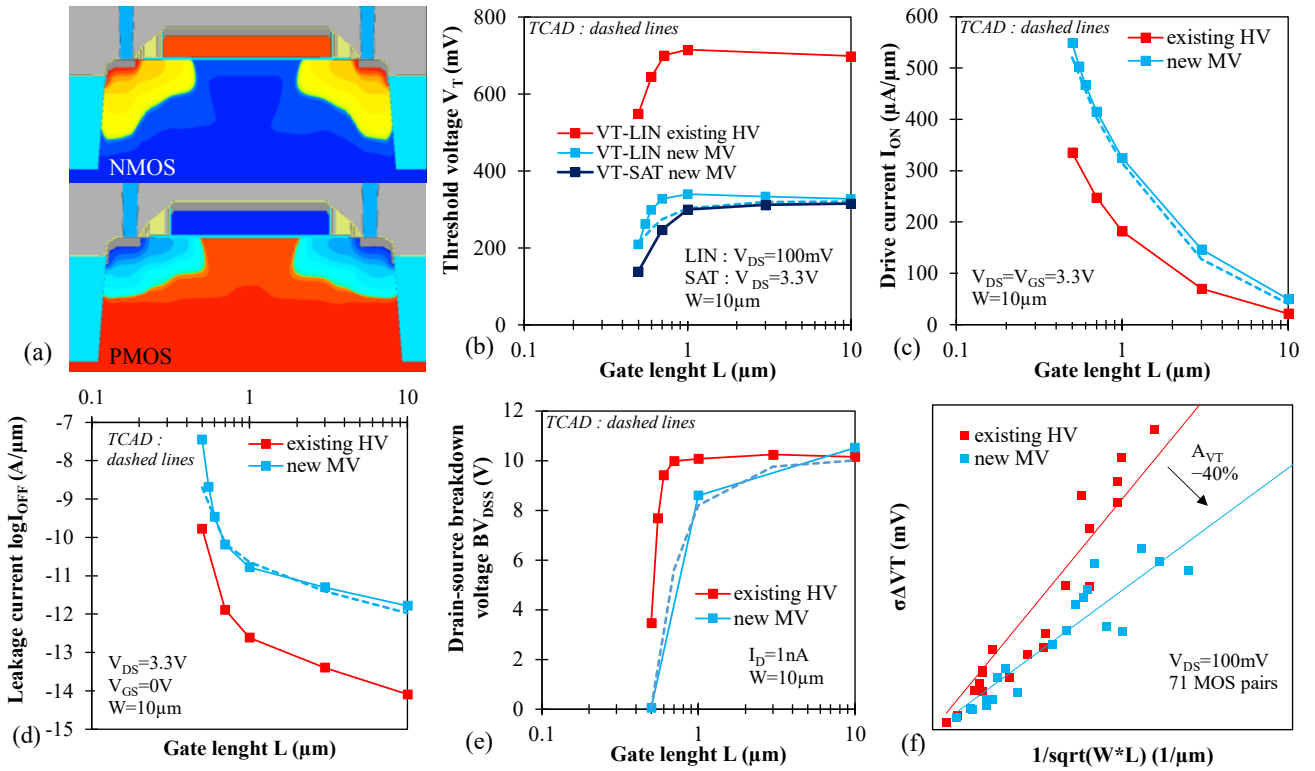


Fig. 3 – TCAD and silicon results. From top to bottom and left to right: (a) TCAD snapshots with doping gradient colourmap (NMOS on the top and PMOS on the bottom), (b) V_T vs L (dashed lines are from TCAD simulations, solid lines are silicon measurements), (c) I_{ON} vs L , (d) I_{OFF} vs L , (e) BV_{DSS} vs L , and (f) Pelgrom plot (transistor matching),

superimposed), the new MV transistor undergo Drain-Induced Barrier Lowering (DIBL) [10], which reduces the V_T when the drain voltage is high. DIBL and SCE limit the minimal gate length L_{min} to around $0.7 \mu m$.

The saturated ON-state drive current I_{ON} has been simulated with the same TCAD setup. NMOS results are shown in Fig. 3c. The expected gain in the drive current associated with thinner gate oxide is confirmed. For the same polarization, a device with a lower V_T has a higher drain current. This is a second advantage of the proposed device.

The OFF-state leakage current I_{OFF} has been simulated (Fig. 3d), and as expected, it is higher because of the thinner gate oxide and lower V_T . This parameter also limits the L_{min} to around $0.7 \mu m$ to stay below our maximum acceptable leakage current value of $100 pA/\mu m$.

The drain-source breakdown voltage BV_{DSS} has been simulated (Fig. 3e). BV_{DSS} has several contributors including drain-bulk reverse diode leakage current and OFF-state channel leakage current [11]. For large L , the main contributor is the drain-bulk junction leakage current, so a thinner gate oxide has minor impact on BV_{DSS} . When reducing L , the OFF-state channel leakage current increases, lowering the value of the extracted BV_{DSS} . This is also a consequence of SCE.

TCAD simulation results confirms the functionality of our new MV transistor. This motivates its

development as it can be obtained for free in terms of process steps and photomasks. It provides a lower V_T (an improvement for analogue design), a higher I_{ON} compared to the HV transistor, and it can withstand high drain voltages. The main drawback is that SCE and DIBL limits the L reduction to no lower than $0.7 \mu m$ due to V_T roll-off (which can lead to a negative V_T at high temperature or high drain voltage) and increased leakage current I_{OFF} .

3.4. Device reliability prediction

To predict the hot-carrier injection (HCI) reliability of our new MV transistor compared to the existing HV, several TCAD simulation output data can be used, without the need of a full degradation model calibration. These output data includes the avalanche generation rate (impact ionization), which is dependent of the electric field and the possibility of acceleration, in other words, a sufficiently large space charge region compared to the mean free path of the charge carrier.

Fig 4a shows the electric field intensity (top) and impact ionization (bottom) colourmaps to illustrate in which regions these phenomena are the most intense. The black isolines represent the doping, showing the source and drain junction position. Fig. 4b shows the lateral electric field along the channel when the transistor is biased in the saturation region with $V_{GS} = V_{DS} = 3.3 V$.

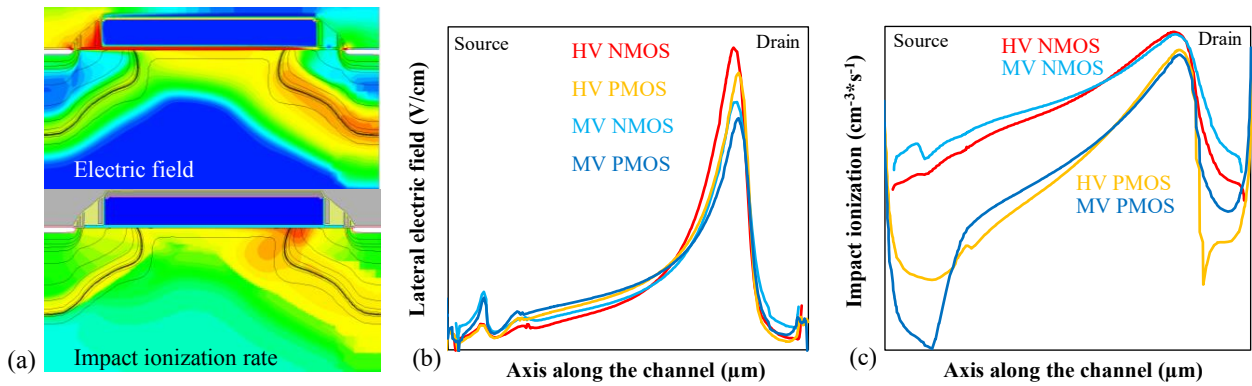


Fig. 4 – TCAD data for hot-carrier degradation prediction. (a) TCAD colourmap of electric field (top) and impact ionization rate (bottom). Black isolines are doping concentration to highlight the drain (right side) and source (left side) junction positions. (b) Lateral electric field in the channel. (c) Impact ionization rate in the channel.

The maximum lateral electric is located near the drain region (right side in Fig. 4), and at that maximum, the lateral electric field in the channel of MV transistors is lower than the one in HV transistors (comparing NMOS transistors together and PMOS together). Although the difference is small, if the injection and degradation mechanisms were the same, we could expect a slight increase in the device lifetime for the new MV NMOS transistor. Fig. 4c shows the impact ionisation rate along the channel with the same voltage biasing. Note that this biasing condition may not be the worst case condition for HCI degradation, but it allows us to locate the region where carrier injection would most likely take place. TCAD simulation of Fig. 4c shows a very small difference of electron pair generation between MV and HV transistors for the considered bias conditions. In this graph, the difference between the NMOS and PMOS in terms of impact ionisation rate can be observed, this is due to the shorter mean free path and higher oxide barrier for holes in PMOS transistors [12].

4. Experimental results for device parameters

After promising TCAD results, the new MV device has been fabricated on sub-40 nm eNVM technology engineering wafers. Experimental results will be presented in this section.

Experimental results show an overall good agreement with the TCAD simulation results. Fig. 3 presents a comparison between the TCAD and experimental results for the NMOS version of our new MV transistor. PMOS results are not shown here for conciseness but the conclusions are similar.

As predicted by the TCAD simulation, the V_T of our new MV transistor is lower due to the thinner gate oxide, but compared to the results of the TCAD simulation, the transistor shows a small increase in V_T with decreasing L before the roll-off at small L . This phenomenon is known as reverse short channel effect (R-SCE) and can have multiple origins [13]. On the other hand, I_{ON} , I_{OFF} and B_{VDSS} of the fabricated transistor show very good agreement with the TCAD simulation.

Concerning the transistor matching, the threshold

voltage matching parameter A_{VT} has been calculated by firstly measuring the standard deviation of the difference of threshold voltages $\sigma_{\Delta V_T}$ of many pairs of identical adjacent transistors. The results are presented in the form of a Pelgrom Plot in Fig. 3f. The A_{VT} dependence with gate oxide thickness is observed, as our new MV device shows an improved A_{VT} compared to the HV device. A small A_{VT} is highly desirable for analogue designs, usually containing a lot of differential pairs and current mirrors, which are fundamental circuit blocks relying on the matching of transistor parameters for optimal performance.

The electrical results obtained using TCAD simulations are confirmed by silicon characterization. By reusing a thinner oxide already available in the technology, we have obtained a new transistor with enhanced performances that can be made for free. It has a lower V_T , a higher I_{ON} and a better A_{VT} compared to the HV transistor.

5. Hot-carrier injection (HCI) degradation

The degradation of the device parameters over time caused by hot-carrier injection (HCI) is important for assessing the reliability of the transistor. During HCI stress, carriers of high energy are generated near the drain where a high electric field exists, and they are injected in the gate oxide where they can be trapped or break Si-H bonds. This phenomenon shifts the transistor parameters such as V_T and I_{ON} by affecting the channel carrier mobility and the effective channel potential [14, 15, 16].

5.1. HCI degradation measurement setup

For the evaluation of HCI reliability of new devices, the worst-case bias conditions need to be evaluated during preliminary measurements. The V_{DS} at which the HCI stress is applied is usually either the maximum voltage at which the transistor will be used during normal usage plus a small margin to account for possible power supply overshoots, or the voltage at which the breakdown region starts. For a given V_{DS} , the

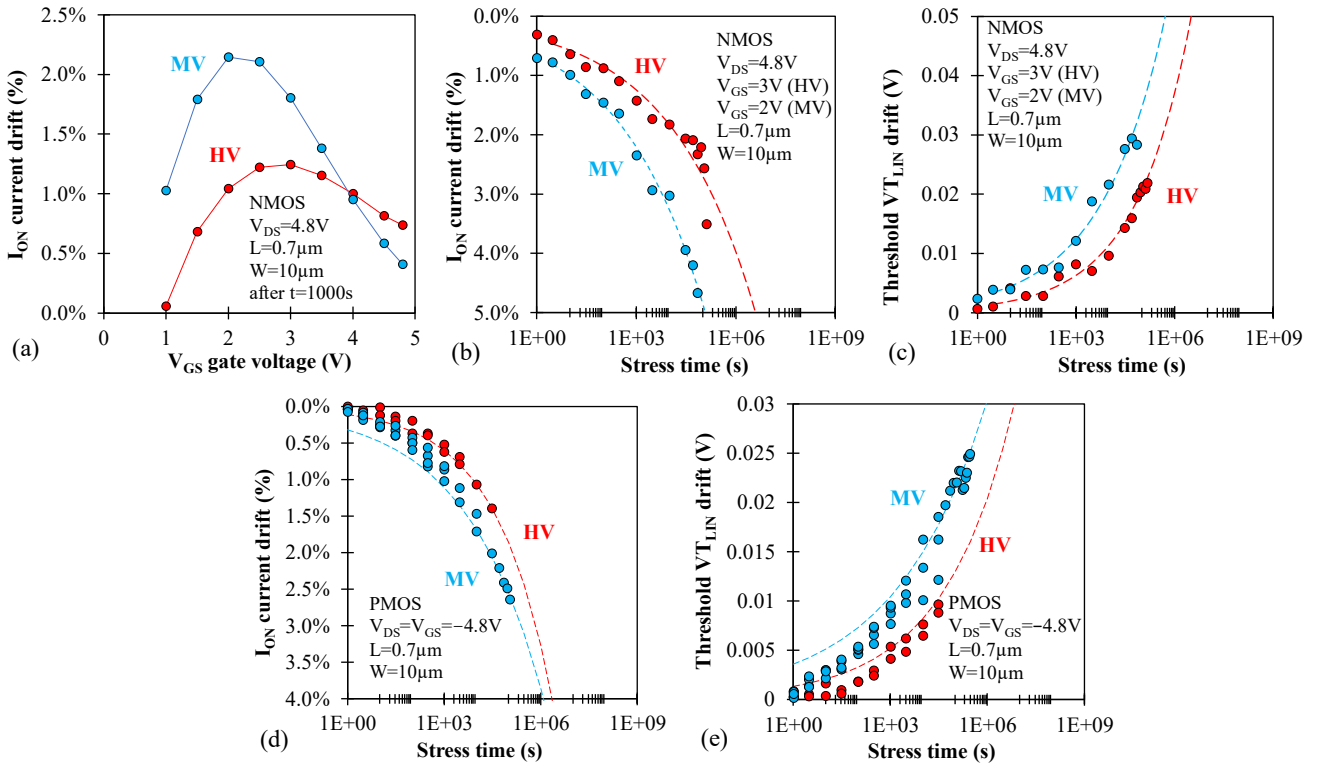


Fig. 5 – HCI experimental results. (a) I_{ON} degradation after 1000 s of preliminary HCI stress of the NMOS transistors to select the most stressing bias condition. (a) Absolute value of drive current drift over HCI stress time for MV and HV NMOS. (b) Threshold voltage shift over HCI stress time for NMOS. (c) Absolute value of drive current drift over HCI stress time for MV and HV PMOS (d) Absolute value of threshold voltage shift over HCI stress time for PMOS

corresponding V_{GS} is chosen to generate the maximum degradation. The worst-case HCI degradation can usually be observed for two different gate voltage conditions:

- maximum gate voltage V_{GS}
- maximum bulk current I_B

I_B being proportional to the number of electron-hole pairs produced by hot carrier [14]. In the first case (maximum V_{GS} , i.e. $V_{GS} = V_{DS}$), hot electrons are injected in the gate (for NMOS transistors, and hot holes for PMOS). This is usually the worst case for PMOS transistors. In the second case, both hot holes and hot electrons are believed to be injected in the gate [12]. This is generally the worst case for NMOS transistors.

HCI reliability strongly depends on the device architecture, especially on the effective gate length L_{eff} , the channel-drain junction, the spacer type, and the oxide thickness [16]. The proposed process optimisation reduces the gate oxide thickness, thus increases the gate oxide electric field transversal to the channel. This should be a disadvantage for our new MV transistor compared to the HV transistor, which is subjected to a more important electric field for the same polarisation.

HCI degradation evaluation has been performed on transistors having the minimal length L_{min} , in our case $0.7 \mu m$, with a W of $10 \mu m$. Initial characterizations of the transistors are made before any HCI stress, by extracting their initial V_T , and I_{ON} . The transistors are

then stressed based on a half-decade time step interval pattern, the degradation being known to follow a power-law with time. The cumulative stress times is 1, 3 10, 30 s, etc. and between each stress interval a characterization is made to track the devices parameters degradation over time [17]. Stress duration went up to 100 000 s.

For device qualification, the device lifetime is usually defined as the stress time necessary to cause a 10 % drift of the I_{ON} current or a 100 mV drift of the threshold voltage.

5.2. Experimental results

The new MV transistor will be subjected to an absolute maximum V_{DS} voltage of 4.8 V for the NMOS and -4.8 V for the PMOS. For this reason, we will perform the HCI stress at this V_{DS} voltage. Corresponding to this V_{DS} voltage, the V_{GS} voltage of worst degradation must be selected. Fig. 5a shows the I_{ON} current degradation after preliminary HCI stresses of 1000 s for different V_{GS} voltages for the MV and HV NMOS transistors. This measurement shows that the strongest degradation for $V_{DS} = 4.8$ V for both NMOS transistors occurs at $V_{GS} = 2$ V for the MV transistor and 3 V for the HV transistor. For the PMOS transistors, the HCI stress will be performed at maximum gate voltage, in our case $V_{GS} = V_{DS} = -4.8$ V, which has been verified

to inflict the maximum damage on PMOS transistors.

Fig. 5b,c,d,e shows the evolution of the device parameter (I_{ON} and V_T) versus the cumulative stress time. The evolution for PMOS transistors is shown in absolute value. A decrease of I_{ON} drive current over stress time is observed for all the transistors, and an increase of V_T during stress time is observed. Power-law fits are added to the HCI measurement data using the least-squares method (dashed lines on Fig. 5b,c,d,e). After 50 000 s of HCI stress, the V_T degradation is equal to 20 mV for the HV NMOS, 30 mV for the MV NMOS, 10 mV for the HV PMOS and 13 mV for the MV PMOS. The I_{ON} degradation after 50 000 s of HCI stress is equal to -2 % for the HV NMOS, -4.25 % for the MV NMOS, -1.5 % for the HV PMOS and -4 % for the MV PMOS. The oxide reduction associated with the new MV transistor has moderately decreased its lifetime.

The HCI reliability results of our new MV transistor are comparable with those of the HV transistor (with a slight advantage for the HV transistor), posing no reliability issues at the studied voltage and gate length.

Perspectives

Although the new MV transistor has very interesting performances at zero-cost, there are still some electrical parameters that can be improved upon regarding SCE. Firstly, because of SCE, the V_T undergoes a roll-off that limits the transistor length to a L_{min} value around 0.7 μm . This is accompanied by a leakage current increase that can cause problems in low-power applications. To try to solve these issues, TCAD and silicon investigations are ongoing to optimize the LDD regions of our new MV transistor, which are inherited from the HV transistor and not necessarily optimized for the MV range. Future work will consist in investigating several other LDD recipes from other devices from the technology that may be reused at zero-cost in our MV device, such as the LV transistors, the SRAM and flash memory devices. We will be particularly interested in the reliability of these optimisations.

Conclusion

A process optimisation is proposed to build a new "zero-cost" device able to address the MV range (3 - 5 V) in an eNVM technology for low-cost products. The proposed device is intended to replace a regular HV device that is currently used instead of a dedicated MV transistor to reduce cost by minimizing the number of photomasks and fabrication process steps. The process optimization resulting in this new MV transistor lowers the V_T and increases the I_{ON} at the cost of an increased I_{OFF} compared to the HV device. It also enhances the matching performances, which is highly desirable for analogue applications. Hot-carrier degradation evaluation shows a slightly shorter lifetime compared to the HV device, but no reliability issues.

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