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Gate stress reliability of a novel trench-based Triple Gate Transistor

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Abstract

This paper addresses the reliability on a novel trench-based Triple Gate Transistor (TGT) fabricated in a 40nm embedded Non-Volatile Memory (e-NVM) technology. In the studied device, two vertical transistors are integrated in deep trenches alongside the main planar transistor to build a TGT. The reliability of this device is investigated targeting the gate oxide degradation, that represents one of the major reliability issues in e-NVM environment. Gate stress tests are motivated by the possibility to use independently trench transistors and the main planar transistor. Thus, the reliability of each gate oxide needs to be studied separately to the others. Moreover, different DC and AC stress tests are performed and analysed to understand the degradation mechanisms effecting the TGT device.

1. Introduction

Today, the semiconductor industry is dominated by submicron devices and unconventional device architectures designed for high density and performance enhancement [1]. In this context, several devices using multi-gate or gate-all-around transistors as an alternative to classical MOSFET have emerged in the last few years [2]-[4]. The studied device follows this trend: two lateral conduction channels controlled by vertical trenches filled with polysilicon are added to the main planar transistor. This arrangement results in a novel Triple Gate Transistor (TGT) which proposes an improved driving capability combined with a minimal footprint compared to conventional MOS transistors [5].

However, the TGT fabrication process includes the etching of deep trenches and the growth of a thin oxide around the trenches profile. Thus, gate oxide stress reliability tests are carried out to assess the possibility of controlling individually trenches and planar transistors of the TGT through their respective gates.

Usually, the oxide degradation investigation is based on DC stress tests. These experiments represent the worst case of the normal operating conditions. Concerning the device life aging in the e-NVM environment, AC stress tests have to be performed. In this paper both DC and AC stress methods are applied

to the TGT for a deep comprehension. The first part of this work presents the TGT manufacturing process. Then, experimental DC and AC stress tests are presented and analysed.

2. Manufacturing and device description

The TGT is integrated in a Non-Volatile Memory environment and designed following the process flow of an embedded NOR Flash technology [6]. No additional steps or masks are required to fabricate the device. The TGT is manufactured as follows: active and oxide Shallow Trench Isolation (STI) regions are first performed (Fig. 1a). NVM implantation is then performed to realize the p-type well of the NMOS-based TGT. Then, the trench patterning presented in Fig. 1b is realized. An oxide is grown along sidewalls of the trenches which are filled with an in-situ doped polycrystalline silicon (Fig. 1c). To achieve the trench patterning, Chemical and Mechanical Polishing (CMP) is performed. As the TGT is realized in a NVM environment, its planar gate is processed based on the Flash floating gate stack (Fig. 1d). This latter includes two shorted polysilicon layers, an oxide/nitride/oxide inter-poly dielectric and a tunnel oxide. The planar gate contact is realized through the gate stack. Two vertical trenches contacts are shifted with respect to

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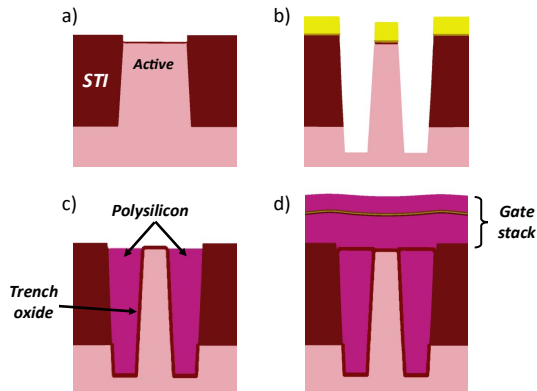


Fig. 1. TGT process flow. a) Active/SOI definition, b) trenches etching, c) oxide grown and polycrystalline silicon deposition, d) gate stack patterning.

the gate stack and connected to the poly-silicon gate trenches. Finally, source and drain contacts are formed with n+ implantations.

Fig. 2a shows the TGT top view. The first conduction channel located between the Drain and the Source is controlled by the planar stacked gate (MG). This transistor is represented with a solid line. The second and third channels, also located between the Drain and the Source, are controlled by the gate trenches (shorted). These devices denoted by MOS Trenches (MT) transistors are represented in dotted line. Finally, the TGT has three conduction channels and it can be represented by three MOS transistors connected in parallel.

Fig. 2b and Fig. 2c show TEM cross-section views of the TGT in width (W) and length (L) directions

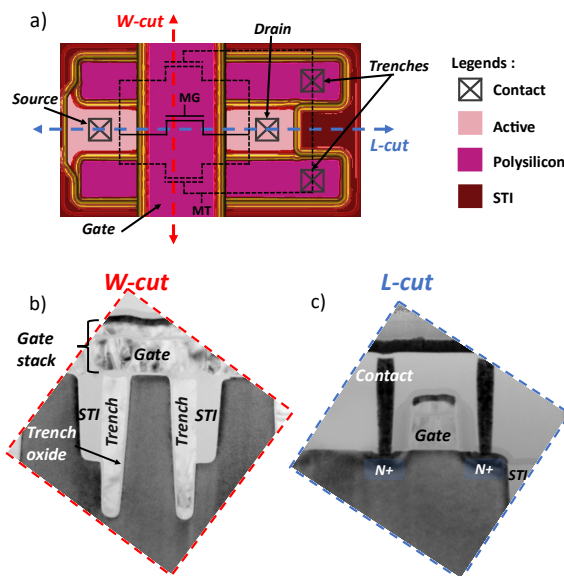


Fig. 2. a) TGT top view and b) W and c) L TEM cuts.

respectively. Based on these figures, we can see that the proposed 3D structure can be used to build an area-efficient transistor with a high driving capability compared to classical planar MOS transistor [5].

3. Experimental results

3.1. Experimental setup

The TGT is made of two different gates: MG controls the planar transistor and MT controls the vertical trenches. Thus, stress tests will address the reliability of both gate oxides. The tested samples, manufactured in a 40nm e-NVM technology, are integrated in a 300 mm wafer. The experimental setup includes an Agilent 4156C semiconductor parameter analyser for electrical characterizations coupled with a Keysight 33500B waveform generator using a Keithley 7174A switch matrix. All stress tests and measurements are performed at room temperature (25°C).

AC stress tests are defined with the following parameters: a rising/falling time (t_{rf}) of 100 ns, a period (cycle) of 200 μ s with a 50% duty cycle. DC and AC stress tests are performed under positive gate bias with drain, source and bulk nodes connected to ground. Tests are periodically interrupted and drain current versus gate voltage (I_d - V_g) characteristics are extracted for both MG and MT transistors to evaluate device performances. A gate voltage sweep ranging from 0 V to 3 V with a drain voltage (V_d) at 0.7 V is used. The threshold voltage (V_t) extraction is performed for a gate voltage associated to a drain current equal to 100 nA. The Subthreshold Slope (S_s) is defined as the required voltage to increase the current by one decade between 1 nA and 10 nA.

3.2. DC stresses

Preliminary measurements are carried out to evaluate the optimal gate bias stress for each transistor. Fig. 3. presents the gate current evolution after applying a Linear Ramp Voltage Stress (LRVS) to the MT and MG gates. We can see that the MG oxide breakdown is reached at 15 V and the MT one at 10 V. Note that MT gate current starts increasing before the MG one. This early leakage current is caused by an irregular thickness of the trench oxide which can be explained by the non-uniform oxide growth along the sidewall. This means that trenches and planar gate cannot support the same bias stress, resulting in different AC and DC test conditions: MG gate stress is performed at $V_G = 10$ V and the MT one at $V_G = 8$ V.

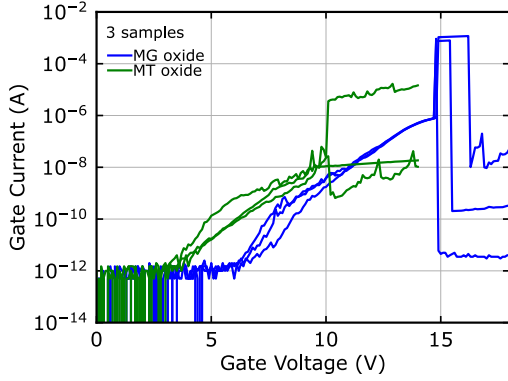


Fig. 3. I-V characteristic of LRVS applied to MG gate and MT gate (three samples).

Constant Voltage Stress (CVS) performed on MG (Fig. 4a) and MT (Fig. 4b) transistors are shown. Note that in Fig. 4a, during the V_{gMG} bias stress, $V_{gMT} = 0$ V and during the V_{gMT} bias stress, $V_{gMG} = 0$ V. For the MG gate stress, we can see a progressive positive shift of the V_t versus stress time and a degradation of the S_s . However, no significant variation is observed for the MT transistor up to 100s (Fig. 4b). At 300s, a flat I_d - V_{gMT} characteristic is measured showing that the transistor breakdown has been reached.

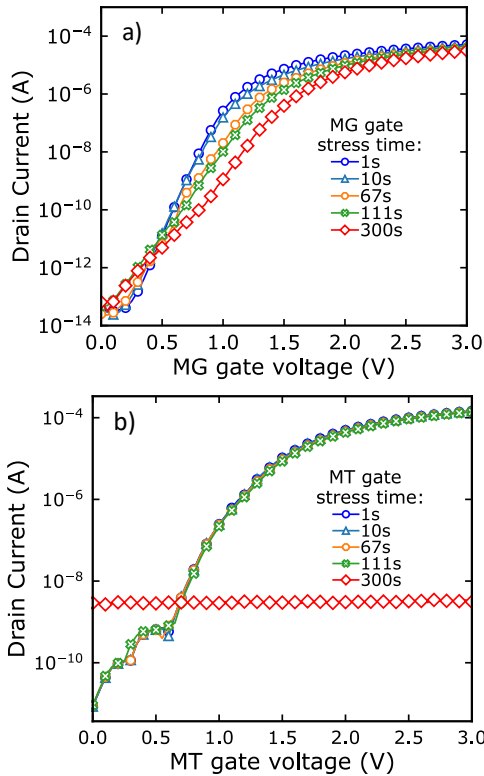


Fig. 4. DC gate bias stress applied on a) MG for $V_{gMG}=10$ V and b) on MT for $V_{gMT}=8$ V.

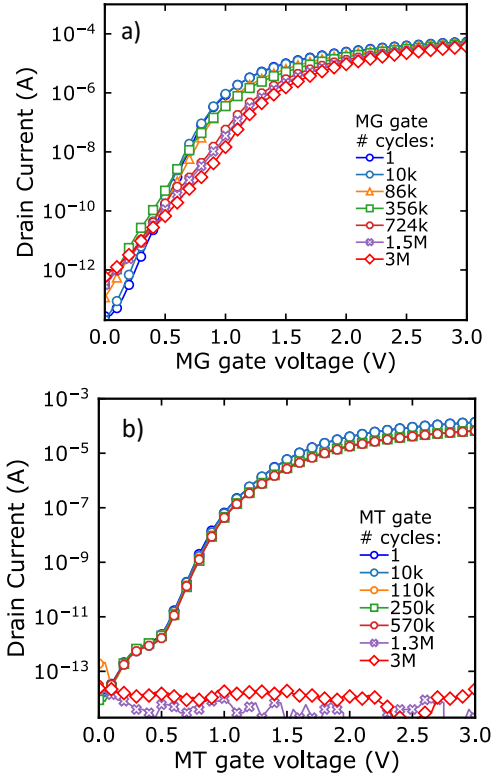


Fig. 5. I_d - V_g characteristics in AC stress mode a) MG stressed with $V_{gMG} = 10$ V, $V_{d,s,b} = 0$ V and (b) MT stressed with $V_{gMT} = 8$ V, $V_{d,s,b} = 0$ V.

3.3. AC stress

Fig. 5a shows the I_d - V_{gMG} characteristics during AC stress tests for $V_{gMG} = 10$ V. As the number of cycles increases up to $3 \cdot 10^6$, V_t and S_s degradation and the leakage current (I_{off}) extracted at $V_{gMG} = 0$ V increases. Fig. 5b presents I_d - V_{gMT} characteristics for $V_{gMT} = 8$ V AC stress. We can notice a slight decrease of driving current (I_{on}) extracted at 3V gate voltage up to 570k cycles. The MT results off after 1.3M cycles.

4. MG transistor versus MT transistor reliability

In some low voltage or analog applications, one can use the different transistors of the TGT separately. The objective here is to study the impact of the MT gate stress on the MG performances and conversely. During the transistor stress test, the other transistor is grounded. This reliability evaluation is conducted by extracting and analysing I-V characteristics as well as key performance parameters (I_{off} , I_{on} , S_s and V_t) after CVS and AC stress.

4.1. Impact of MG stress on MT performances

The V_t and S_s shifts (ΔV_t and ΔS_s) versus stress time are presented after CVS (Fig. 6a) and AC stress (Fig. 6b) applied to the MG gate. For a fair comparison between AC and CVS tests, the effective stress time is plotted (i.e., the relaxation time of AC stress is not accounted). The MG transistor ΔV_t (ΔV_t MG) increases with stress time from 10 s for both AC and CVS tests while the MT transistor ΔV_t (ΔV_t MT) remains constant. The variation of ΔV_t MG is explained by the electron trapping at the channel/oxide interface and in the oxide bulk [7]. The ΔS_s shows the same trend. It increases only for the MG transistor since 30 s stress which indicates interface states generation [8] more present in AC compared to CVS stress. The ΔV_t MT and ΔS_s MT remain constant during the stress time suggesting that the MT transistor is not impacted by charge trapping occurring during MG gate stress.

The I_{on} and I_{off} variations (ΔI_{on} and ΔI_{off}) after CVS (Fig. 7a) and AC (Fig. 7b) stress applied to the MG gate are reported. For both stresses, ΔI_{on} decreases during the time for the MG (ΔI_{on} MG) while it remains constant for the MT (ΔI_{on} MT). No significant ΔI_{off} is measured for both transistors and stress types. These variations can be explained by trapped charge or interface traps generation, localized at channel-oxide tunnel interface [8]. During the I-V reading state, interface traps become negatively charged and create an inversion region. This region leads to increases the drain resistance, resulting in a decreases of the driving current I_{on} and increases of the S_s parameter.

4.2. Impact of MT stress on MG performances

We report here the evolution of ΔV_t and ΔS_s after CVS (Fig. 8a) and AC (Fig. 8b) stress tests applied to the MT gate. In the case of the CVS, ΔV_t and ΔS_s of both transistors remain constant until 200 s. After 200 s, ΔV_t MT and ΔS_s MT significantly increase, which corresponds to the MT transistor breakdown. In contrast, ΔV_t MG and ΔS_s MG decrease, indicating that the MG transistor is damaged but still operating. However, for the AC stress presented in Fig. 8b, a different behaviour is observed. ΔV_t MT increases and ΔS_s MT decreases at 100 s while ΔV_t MG and ΔS_s MG are not affected. Therefore, the MG transistor is not damaged during MT transistor AC stress.

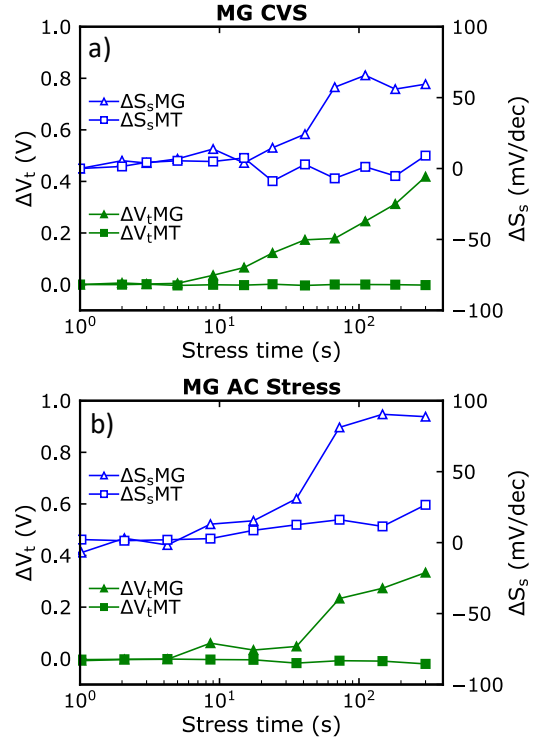


Fig. 6. V_t and S_s shifts as function of (a) CVS and (b) AC stress time applied to the MG gate (V_g MG = 10 V, $V_{d,s,b}$ = 0 V).

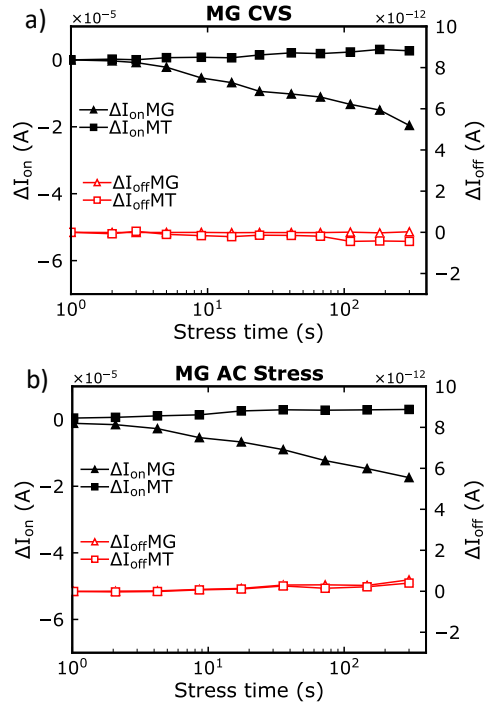


Fig. 7. I_{on} and I_{off} shifts as function of (a) CVS and (b) AC stress time applied to the MG gate (V_g MG = 10 V, $V_{d,s,b}$ = 0V)

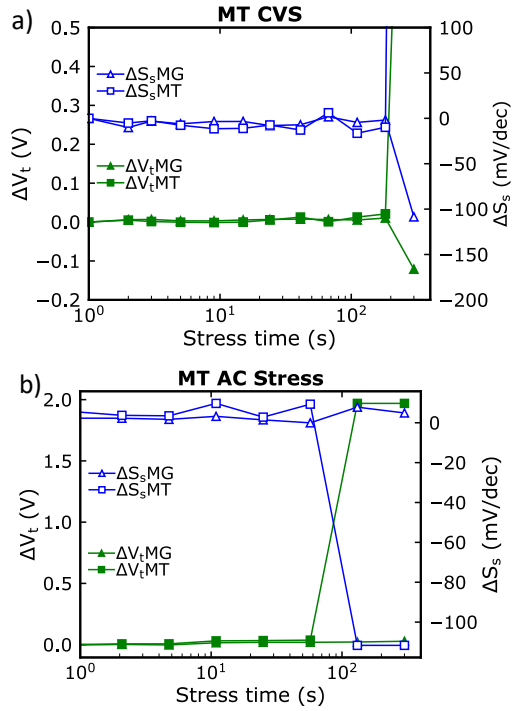


Fig. 8. a) CVS and b) AC stress dependence of V_t and S_s shift as function of stress time for MT gate stress with $V_{g,MT} = 8$ V, $V_{d,s,b} = 0$ V.

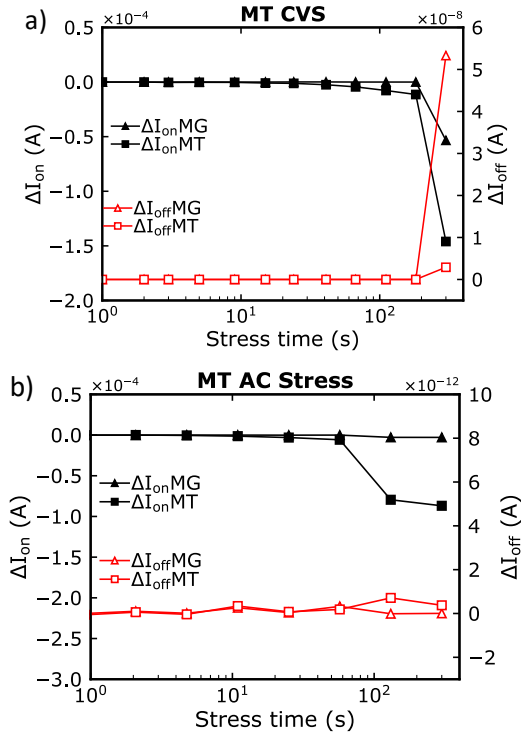


Fig. 9. a) CVS and b) AC stress dependence of I_{on} and I_{off} shift as function of stress time for MT gate stress with $V_{g,MT} = 8$ V, $V_{d,s,b} = 0$ V.

Fig. 9a presents ΔI_{on} and ΔI_{off} evolution versus stress time during the MT gate CVS and the Fig. 9b shows the variation for the AC stress. In the first case, $\Delta I_{off,MT}$ increases and $\Delta I_{on,MT}$ decreases since 200 s. The MG transistor is also impacted with a slight variation of its parameters ($\Delta I_{on,MG}$ and $\Delta I_{off,MG}$). In Fig. 9b the $\Delta I_{on,MT}$ starts decreasing just before 50 s while no shifts are observed for the MG transistor parameters. These results indicate that the MG transistor is not damaged during MT gate AC stress.

4.3. Summary results

Fig. 10a reports the MT transistors I_d - V_g characteristics after the MG gate stress for different stress methods. The I_d - V_g characteristics are similar before and after the different stress types. Thus, the MG degradation does not damage the MT transistor, whatever the stress is. Regarding the fact that for the LRVS stress, the MG transistor breakdown does not impact the MT transistor. It can be related to the MG oxide breakdown probability which depends on its area [9]. Indeed, the intersection between the MG oxide and the MT oxide located at the substrate-trench-gate intersection region is narrow, limiting the impact of the MG stress on the MT.

In Fig. 10b where different stress types are applied to the MT gate, the MG transistor is damaged. Specifically, after the LRVS test, the MG transistor is no operational (the drain current is constant at $10 \mu A$) suggesting that the MG transistor has been damaged by the MT breakdown. After the CVS test, the final characteristic shows a low I_{on} and a high I_{off} current compared to the fresh characteristic. Finally, the AC stress test has no impact compared to the fresh characteristic except a lower I_{on} current. The difference between the characteristics after AC stress and LRVS can be explained by the charge detrapping during the relaxation time [10] (i.e, stress interruption during the I_d - V_g MG extraction). However, after the AC stress the I-V characteristic is comparable to the fresh one as it includes periodically stress interruptions defined by the AC duty cycle.

The impact of the MT stress on the MG transistor degradation needs more investigation. What we can infer from Fig.10b is that the LRVS test of the MT transistor short-circuits the source and drain of the MG transistor, resulting in a high current ($10 \mu A$) when its gate voltage is equal to zero. Moreover, due to the manufacturing process, we have observed a tip effect located at the substrate/trench/gate intersection oxide region

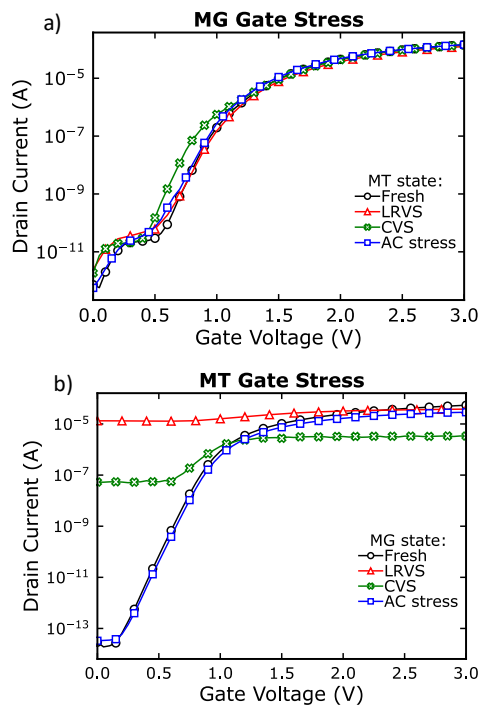


Fig. 10. a) I_d - V_g MT curves versus MG stress and b) I_d - V_g MG curves versus MT stress obtained after LRVS, CVS and AC stress.

which can lead to an enhanced electrostatic potential. Therefore, this effect can explain the non-reciprocal oxide breakdown between the MG and MT transistor.

5. Conclusion

In this paper we investigate the electrical reliability of a novel TGT transistor under positive gate DC and AC stresses. The TGT is made of distinct transistors (MG and MT) controlled by independent gates. The electrical parameters evolution as a function of stress time revealed that the MG gate degradation does not impact the MT transistor, whatever the stress type applied. On the contrary, the MT gate degradation leads to the MG transistor damage depending on the applied stress type. Indeed, DC stress applied to the MT gate strongly damage the MG, but AC stress has a minor impact as a slight decrease of the I_{on} parameter of the MG transistor is reported. Therefore, for decorrelated gate applications, it will be suitable to report the maximal stress on the MG transistor.

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