# Ultra Low-Power 2.5$\mu$W CMOS Implementation of a Mixed Analog-Digital Wake-Up System Based on Frequency Analysis

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# Ultra Low-Power 2.5$\mu$W CMOS Implementation of a Mixed Analog-Digital Wake-Up System Based on Frequency Analysis

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***Abstract*—An ultra low power acoustic wake-up detector based on high frequency signal analysis is presented in this paper. Focused on environmental or military Internet of Things (IoT) applications, it aims at detecting in real time the presence of specific animal species or drones for generating alerts and for triggering power consuming tasks such as high frequency signal recording only when needed.**
**This wake-up detector continuously monitors the presence of specific frequencies in an analog acoustic signal, with a good frequency selectivity and a high frequency range detection capability. It is based on an ultra-low power analog frequency to voltage converter using a current-mirror, analog timers and synchronous comparators.**
**Dedicated to long term stealth environmental or military surveys, a strong emphasis has been put on power consumption reduction in order to reduce batteries constraints. Its power consumption has been reduced to $2.5\mu W$, leading to an autonomy of more than $28$ years with a single coin cell CR2032 battery.**

## I. Introduction

Autonomous embedded intelligent monitoring systems having an ultra low power consumption (less than $100\mu W$) are an important field of the industrial Internet of Thing (IoT). They can be operated operated over a long period of time without changing batteries, making them useful for constrained applications such as industrial or military monitoring in harsh environments where it is difficult or dangerous to send a human, or for environmental surveys such as in strict nature reserves where it is not advisable to disturb fauna.

In most of these applications, interesting events are rarely present [1], [2]. Thus, it is not relevant to perform a very accurate detection all over the time (such as detecting a given specie) as it would lead to consume a lot of power. Instead of that, is it better to split the detection in two parts as described in Fig. 1 : first one is to detect when signal has a good probability of being a true positive using a simple ultra low-power always-on detector, and to confirm this detection in a second step using more accurate embedded classification techniques (such as neural networks) having a higher power-consumption.

This paper focuses on the always-on ultra-low power first step of this detection, focused on a specific type of pattern: the presence of a signal having it base frequency in a given frequency interval. This pattern is relevant for applications such as environmental study on animals emitting echolocation [3], [4], or military application such as drone detection [5].

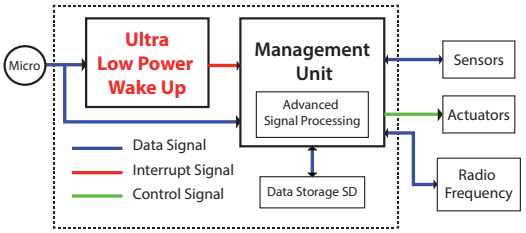


Fig. 1. General system presentation.

## II. Always on Ultra Low-Power Wake-Up Detector

In this paper, a silicon implementation of the always-on ultra-low power detector is proposed in $0.35\mu m$ Austria Micro System (AMS) technology. It aims at optimizing drastically power consumption of the wake-up detector while allowing input signals detection in a large frequency range (up to $200kHz$) in ultra low power, making it versatile for many applications. It makes the most of mix-analog and digital circuits in order to improve power budget. It has been inspired by several previous implementations. [6] is energy efficient ($1.8\mu W$), but its input signal frequency is limited (less than $1kHz$). [7], [8] are also really energy efficient, but focused on detection of specific ultra-sonic frequencies (41 kHz and 57 kHz respectively). [9], [10] have a wider input frequency range, but are based on digital or analog discrete circuits making their power consumption higher than previous implementations.

### A. Architecture description

Fig. 2 presents the wake-up system description. Input signal $U_S$ is pre-filtered by an hysteresis comparator for both removing noise and selecting signal having a minimal amplitude. Then, output signal $U_{InCp}$ of the comparator triggers a monostable generating a signal $U_M$ with a constant pulse time,

on each rising and falling edge of $U_{InCp}$. Thus, $U_M$ average value is directly proportional to the $U_S$ frequency.

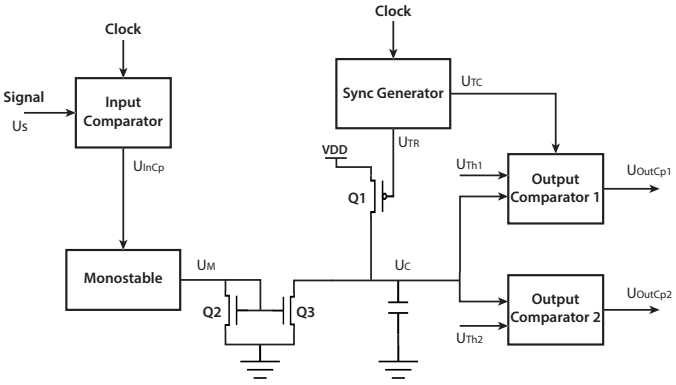


Fig. 2. General system schematic.

A frequency to voltage linear conversion is done by using a current mirror coupled to a capacitor $C_1$. The current mirror is used as a charge time measurement unit : $U_M$ pulses create a constant current in the left transistor of the current mirror. This current is mirrored into the right transistor, discharging $C_1$ by a constant current $I_{C1}$. Thus, $U_{C1}$ decreases linearly during monostable pulses.

Equation 1 describes $U_{C1}$ evolution, corresponding to waveforms shown in Fig. 3:

$$U_{C1} = V_{DD} - \int_0^t \frac{I_{C1}(t)}{C_1} dt \quad (1)$$

This leads a succession of linear discharges during monostable pulses, alternating with constant voltage phases as shown in Fig. 3. Considering that the number of small linear discharges between two successive resets is $N = \frac{F_S}{F_{TC}}$, where $F_S$ is the input signal frequency, $F_{TC}$ is the sampling frequency of the synchronization generator, and $T_{PW}$ is the pulse duration, leads to equations 2.

$$U_{C1} = V_{DD} - \frac{I_0}{C_1} * N * T_{PW} \quad (2)$$

Consequently, $U_{C_1}$ is linear with input signal frequency $F_S$ at the end of each signal's period. $U_{C_1}$ is reset to $V_{DD}$ by $U_{TR}$, the output of the synchronization generator, after being processed by output comparators. The role of this pair of comparators is to determine whether the input frequency is within a specified interval or not. This is done by adding a AND gate at their outputs $U_{OutCp1}$ and $U_{OutCp2}$. In order to save energy, dynamic comparators are used and triggered by $U_{TC}$, just before the reset of $U_C$ by $U_{TR}$. The input comparator is also dynamic for the same reason.

In order to ensure strict timing for signals $U_{TR}$ and $U_{TC}$, with a precise delay between them, the synchronization generator uses an external clock with frequency dividers.

### B. Harware Implementation

*1) Comparators:* Three comparators are used in this system: an input comparator and two output comparators. A basic

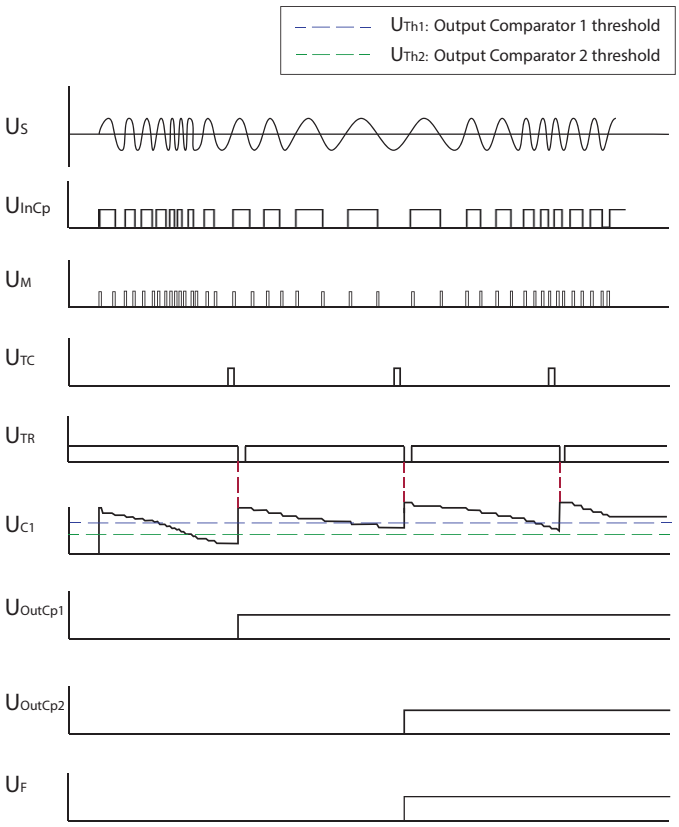


Fig. 3. wake-up system waveforms.

implementation would be to use analog comparators working continuously, but this would result in an excessive power consumption (around $4\mu W$ in the best case). Instead, we have chosen to use a customized latch dynamic comparator presented on Fig. 4. This standard dynamic comparator, triggered by an external clock, consumes approximately $2nW$ at the maximum required frequency ($200kHz$) for our applications.

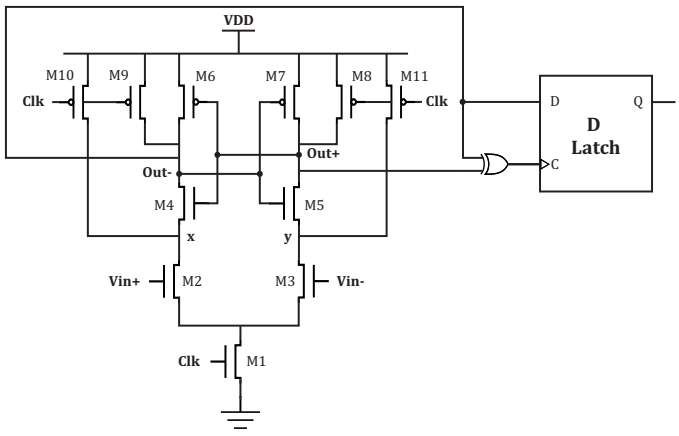


Fig. 4. Schematic diagram of latch dynamic comparator.

As we can see on the Fig.4, the comparator consists of a differential pair coupled with two inverters mounted head-to-tail. Comparator is reset by holding $Clk$ signal to $0V$, turning

on $M10$ and $M11$ PMOS transistors, setting $x$ and $y$ in Fig.4 to $V_{dd}$. In this case, $Out-$ and $Out+$ are also set to $V_{dd}$. When clock is set to $V_{dd}$, a comparator active phase begins as $x$ and $y$ are no longer tied to $V_{dd}$. An imbalance on $x$ and $y$ voltages is caused by the differential pair inputs, leading to discharge $M4$ and $M5$ capacitances at a different micro-current. This imbalance is amplified by the two head to tail inverters, leading to a fast and efficient convergence of outputs $Out+$ and $Out-$ to their final values. In order to maintain output $U_{InCp}$ state, we added to the basic structure of a dynamic comparator a D-latch. This one is triggered by a XOR gate generating a rising edge as soon as comparator outputs are stabilized. These comparators can be used in hysteresis mode, like a standard comparator, in order to avoid the system being disturbed by noise.

*2) Monostable:* The monostable signal is generated by a double inverter coupled with a $RC$ circuit, as we can see on the Fig. 5. Output of the second inverter is similar to the input of $UInCp$, with a fixed delay $\tau$ created by the first order low pass filter composed by $R_1$ and $C_2$. Each time input $U_{InCp}$ is changing (rising or falling edges), the output XOR gate generates a high state pulse having a length $\tau$.

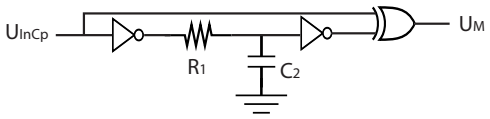


Fig. 5. Schematic diagram of the monostable implementation.

$U_M$ is shown on the Fig. 3. This monostable is very efficient, as its average power consumption is around $100pA$. Its pulse width can be adjusted very precisely by an external capacitor, allowing user to customize the behaviour of the chip for different input signal frequencies.

*3) Current Mirror:* Current mirror is one of the central elements of this system. It is replacing the CTMU used in [9]. The current mirror is used as a constant controlled current source driven by the monostable output $U_M$ to discharge the main capacitor $C_1$. When activated, current value in the mirror, $I_0$, is defined by the output voltage of the monostable. Monostable pulses voltage being positive, the current mirror has to be implemented using NMOS transistors. Consecutively, mirrored current will discharge $C_1$ capacitor as shown in Fig. 3.

*4) Capacitor and associated currents:* Being discharged linearly by successive phases, the $C_1$ capacitor is the heart of this wake-up detector. It is being discharged by the current mirror triggered by the monostable, and periodically reset to $V_{DD}$ by the $Q_1$ PMOS transistor driven by the synchronization generator. The values of $C_1$ and $I_0$ have to be chosen carefully, following this equation:

$$\frac{I_0}{C_1} = \frac{V_{DD}}{\frac{F_S}{F_{TR}} \times 2 \times T_{PW}} \tag{3}$$

where the input frequency to be detected is approximately $F_S = 100kHz$, periodical reset frequency is $F_{TR} = 1kHz$, duration of the pulse of the monostable is $T_{PW} = 14ns$, supply voltage $V_{DD} = 3V$ and $U_{C_1}$ minimal value is 0. Thus, having chosen to limit $I_0$ to $5\mu A$ for power saving reasons, $C_1$ capacitor value must be equal to $4pF$.

*5) Synchronization generator:* The reset trigger and the comparator trigger are generated by the synchronization generator. It is based on a succession of $JK$ flip-flops dividing the clock signal frequency by 2 at each step as we can see on Fig. 6. In order to make the flip-flop toggle on each clock signal, like a $T$ flip-flop, $JK$ flip-flops inputs are connected to $V_{DD}$. By adding both an AND gate and a NAND gate having as inputs the outputs or the complemented outputs of the flip-flops, we generate both the comparator trigger signal and the reset signal delayed by a fixed amount of time. The NAND gate is necessary for generating reset signal because it is driving a PMOS transistor. The NOT gate placed in output of one of the flip-flops induces a delay between $U_{TR}$ and $U_{TC}$ in order to ensure that output comparison is done before capacitor voltage is reset to $V_{DD}$. $U_{TC}$ and $U_{TR}$ pulses length can be adjusted by disconnecting the outputs of the first flip-flops as shown on Fig. 6. This does not affect $U_{TC}$ frequency which is equal to:

$$F_{U_{TC}} = \frac{F_{clock}}{2^n} \approx 2kHz \tag{4}$$

where $F_{clock} = 2MHz$ is the clock frequency and $n = 10$ is the number of flip-flops.

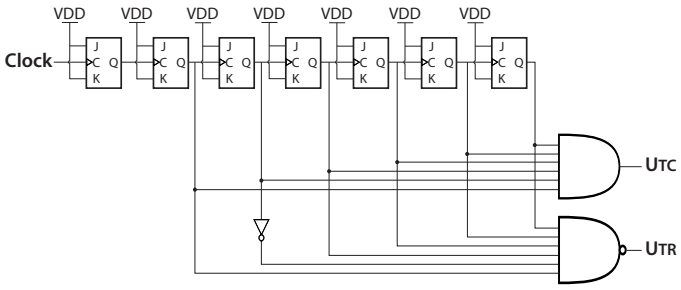


Fig. 6. Schematic diagram of the synchronization generator implementation.

An analog astable implementation for this module could have been chosen, but the digital one presents many advantages like a very low power consumption and timing precision. Moreover, a customization of the frequency divider can be integrated for changing the division factor using an external pin in order to change the reset frequency of capacitor $C_1$.

## III. Results

Fig.7 shows the Cadence simulation of the wake-up system previously presented in Fig.3. $U_C$ signal is decreasing gradually on each capacitor discharge, and periodically reset to $V_{DD}$.

Using this wake-up detector implementation for detecting a $100kHz$ signal (*i.e.* bat echolocation frequency), has an average power consumption of about $2.5\mu W$ with a power supply in $3V$, which is more than 12 times lower than

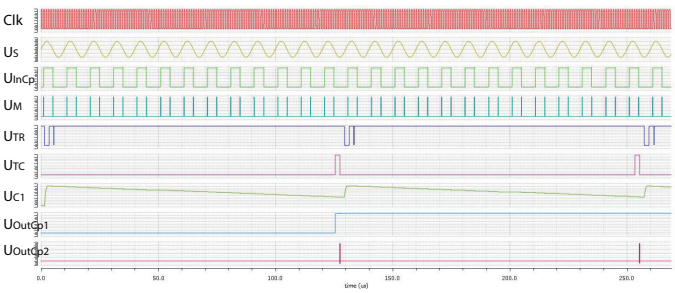


Fig. 7. Simulation results of the acoustic wake-up system.

the analog implementation proposed in [10]. Moreover, it power consumption is comparable to [6]–[8] but without the constraints of fixed frequencies or a limited frequency range, making it interesting for a more versatile use.
Power budget is split between very short power consuming phases and longer ones having a close to zero power consumption :

- $C_1$ reset phase : a current of $20\mu A$ is drawn during 2 clock pulses every $1024$ clock pulses. This leads to an average current equal to $I_{RC1} = 40nA$.
- Input comparator active phase : current is drawn in dynamic comparators mainly during initialization before each comparison phase. Simulations have shown that a current equal to $800\mu A$ is drawn during $2ns$. Thus, input comparator power consumption is proportional to its triggering frequency. Input signal frequency to be detected is equal to $100kHz$. A triggering frequency of $500kHz$ is necessary in order to avoid aliasing of signal in a range between $100kHz$ and $250kHz$. At this frequency, average current drawn is equal to $800nA$.
- $C_1$ discharge phases : a current of $5\mu A$ is drawn during each monostable pulse having a duration of $14ns$. In the worst case for power consumption, when input signal frequency is $100kHz$, interval between two discharge phases is $5\mu s$ (there are 2 pulses for each period). Thus, average power consumption of this phase is $I_{DC1} = 14nA$.
- $C_1$ constant phases : most of the time, $C_1$ has a constant voltage. During this phase, average current drawn is $I_{idle} = 0.6nA$.

Finally, overall average consumption of the proposed ultra low power wake-up system is equal to $2.5\mu W$ under $3V$.

Coupled with a single coin cell CR2032 $700mWh$ battery, detector can keep running for about 28 years, without taking into account battery self-discharge.

## IV. Conclusion and future works

Thus, the ultra low power wake-up detector presented in this paper consumes only $2.5\mu W$. More versatile or more energy aware than existing implementations, it can be used for applications in environmental or military surveys such as stealth intelligent recording of acoustic signals emitted by animals or drones, or alarm systems such as smart dust presented in [11]. Other applications using non-acoustic high frequency signal analysis and detection could also be developed using this wake-up detector, such as pulsed light wake-up systems operated from a long distance to trigger simultaneously a whole environmental wireless sensor networks [11].

An application of this system will help to protect a strict nature reserve island (Ilot Bagaud, part of the *Parc National de Port Cros* in France) from rats intrusions [12], and to record, analyze and transmit alerts in real time.

## Acknowledgment

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