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Design of Analog Nonlinear Transformations based on a Gilbert Multiplier for Energy Detection

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Abstract—This paper focuses on the design of two analog nonlinear transformations dedicated to analog signal processing such as energy detection: the square function and the Teager Energy Operator (TEO). Both requiring an analog multiplier, this paper firstly analyses the design equations of a MOS Gilbert cell in order to operate around the mid supply voltage. Considering this, an analog multiplier, having a differential input range of ± 400 mV, has been designed using an AMS 0.35 μm technology and a voltage supply (VDD) of 3.3 V. It has a core area of 620 μm^2 and offers power-gating capability, which enables a power consumption of 2.28 μW when a duty cycle of 0.25% is considered. Next, an analog square function and an analog TEO, have been implemented and manufactured using the designed Gilbert cell. The analog square function has a core area of 0.9 mm^2 and measurement results show that it is able to compute the square value of its differential input voltage with a mean precision of 2.92% in 5 μs assuming a differential input voltage of ± 400 mV with a common voltage of $VDD/2$. Moreover, it generates 700 mV spikes when 200 mV pulses are applied on its input. Finally, the designed analog TEO has been implemented using its discrete time equation instead of its continuous time equation since it does not require derivatives computing. It has a core area of 2.2 mm^2 , an active power consumption of 6.21 mW and a standby power consumption of 1.43 nW. Measurement results shows that it generates until 250 mV spikes when 200 mV pulses are applied on its input.

Keywords—analog multiplier, energy detection, Gilbert cell, power-gating, square function, Teager energy operator

I. INTRODUCTION

Among the different cardiovascular diseases which cause as many deaths as cancer in Europe, cardiac arrhythmia is one of the most common one. Fortunately, several types of cardiac arrhythmia can be detected using only heart rate variability [1]. To achieve it, the instantaneous heart rate can be estimated in real-time from pulsed physiological signals synchronized with heartbeats such as electrocardiogram [2], phonocardiogram [3], arterial pressure [4] or photoplethysmogram [5]. It is also necessary to be able to detect each pulse associated to a heartbeat in one of these signals, which has led to the development of lots of heartbeat detection methods [6].

Most of instantaneous heart rate detection methods are based on a digital signal processing [7][8][9] in addition to an analog conditioning chain for the pre-processing of the sensed signal. They also require at least an Analog-to-Digital Converter (ADC) and a computing unit such as a microcontroller, both having a certain cost in terms of power, size, and price. However, the time during which cardiac arrhythmia is detectable can be very brief. Its detection also requires a full-time monitoring which can be more comfortably achieved from the patient point of view with a compact battery-powered device.

Unfortunately, advanced digital processing and full-time monitoring can be done by compact battery-powered devices at the cost of regular battery recharges. To reduce power consumption, size, and cost, it has been proposed in [2] a processing based on an analog energy detector to detect heartbeat-synchronized pulses in electrocardiograms, which has been inspired by low-power and low-cost non-coherent receivers used in Ultra-WideBand Impulse Radio (IR-UWB) [10][11]. The main processing step of this non-coherent detection is the nonlinear transformation which computes the square value of the sensed signal. This can be done in the analog domain with an analog multiplier [12] which potentially has a smaller cost in terms of power consumption (especially when it can be periodically turned-off), size, and price compared to a digital processing.

Nevertheless, another approach is to replace the square function by another energy operator such as the Teager-Kaiser Energy Operator (TEO). The TEO has been initially developed by Herbert M. Teager and Shushan M. Teager [13] for “Vocal Tract” applications, and largely investigated by J. F. Kaiser [14][15][16]. It acts as a squarer and a high-pass filter at the same time [17]. The TEO has been used for energy detection in various applications [18][19][20][21] such as amplitude and frequency demodulation [16] or the detection of heartbeat-synchronized pulses in electrocardiograms [22]. Unfortunately, conversely to the square function, an implementation of the TEO based on its continuous time equation requires derivatives computing in addition to multipliers. For this reason, it is mainly computed in the digital domain with a microprocessor using its discrete time equation [20][21][22] even if some analog implementations using the continuous time equation can be founded for spike detection in neural recording systems [18][19]. However, the TEO discrete time equation requires only one subtractor, two multipliers and three sample & hold circuits which can be implemented easier than derivatives operators in the analog domain. For this reason, a new analog implementation of the TEO based on its discrete time equation is proposed here and this implementation also requires two multipliers.

However, whatever the used analog energy operator, it is important to underline that it must have a voltage response with a high magnitude to make easier spike detection when a comparison with a voltage threshold is used [10]. To increase the response magnitude of an analog energy operator based on multipliers such as an analog TEO implementation, multipliers with wide output dynamic range must be used. Moreover, in the context of biological signals such as electrocardiogram which can know high variations around its baseline (if the patient moves for example), it is necessary for multipliers to operate on a wide input voltage range too. For this reason, inputs and output must be biased to the mid-supply voltage which is $VDD/2$ when a single supply of VDD is used.

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Thus, the main design challenge for the analog energy operator is to work on the widest voltage range around $VDD/2$, which means it must be able to process large input signals.

Many analog multiplier architectures have been proposed in literature and especially the well-known Gilbert cell. However, they are usually able to work as a multiplier on a limited input voltage range. Indeed, a true multiplication can be obtained with bipolar Gilbert cells when input voltages are small in front of the twice of the thermal voltage, or with MOS Gilbert cells when one of the both input voltages is small and the other one is large. Although this is enough for mixing stage in wireless emitters and receivers, this becomes an issue when the square value of sensed physiological signals has to be computed since they can have a high dynamic range according to the measurement conditions.

For these reasons, the design of the MOS Gilbert cell is analyzed in section II in order to optimize the voltage input range, and the also the associated voltage output range, for which a true multiplication can be obtained. In section III, post-layout simulation results of the designed multiplier are provided and analyzed in terms of computing precision of the multiplication. Next, section IV deals with the implementation of an analog square function built around the designed multiplier and shows measurements results which are compared to an ideal squarer. In section V, the TEO is presented and especially the effect of the sampling frequency on its output magnitude. Finally, section VI proposes a new analog implementation of the TEO using its discrete time equation. Measurement results are provided and compared to the ones obtained with the analog square function.

II. DESIGN OF THE ANALOG MULTIPLIER

The designed analog multiplier is based on a Gilbert cell which has the advantages to use a limited number of transistors in addition to have high input impedances. Its transistor level schematic is shown on Fig. 1.a. This structure also consists of three differential pairs (M1-M2, M3-M4, and M5-M6), two active loads (MA and MB), and a current source M0 controlled here by a *PDB* signal, *PDB* being a logic signal which enables the multiplier to be switched-on or switched-off. Finally, for reasons of symmetry, it should be noted that the transistors M1 and M2 must have the same dimensions, as well as the transistors MA and MB and the transistors M3, M4, M5, and M6.

However, it should be noted that although *VD1* and *VD2* are differential inputs voltage, *VOP* is here a single output voltage thanks to the connection between the gate and the drain of the MA transistor. Thus, this analog multiplier and also, the processing chain where it could be used, does not require an additional differential to single voltage converter. Nevertheless, a differential output can be obtained by removing this connection but then requires an appropriate biasing of MA and MB gates.

In the following subsections, the designed analog multiplier is analyzed in order to demonstrate with the help of design equations that it can operate as a true multiplier over a large range of *VD1* and *VD2*.

A. Biasing and Kirchhoff's Laws

To allow a four-quadrant multiplication on the widest dynamic range, the circuit must be biased as follows:

$$VOP = \frac{VDD}{2} \text{ when } VIP = VIN = V2P = V2N = \frac{VDD}{2}. \quad (1)$$

Indeed, from an ideal point of view, the use of the mid supply voltage as input and output common mode voltages will potentially authorize the use of the overall voltage range delimited by the negative voltage supply (here GND) and the positive supply voltage (here VDD).

In this case, if capacitive effects are neglected, the output voltage *VOP* can be written for low working frequencies according to Fig. 1.a as follows:

$$VOP = \frac{VDD}{2} + R_{OUT} \cdot I_D \quad (2)$$

where R_{OUT} is the output resistance of the analog multiplier and I_D is the differential current in the active loads defined as follows:

$$I_D = I_A - I_B \quad (3)$$

with:

$$I_0 = I_A + I_B. \quad (4)$$

To demonstrate that the proposed circuit works as an analog multiplier, it is necessary to write I_D as a function of *VD1* and *VD2*. To do this, I_A and I_B can be written as follows:

$$I_A = I_3 + I_5 \quad (5)$$

$$I_B = I_4 + I_6, \quad (6)$$

which allows I_D to be computed as follows:

$$I_D = I_{D1} - I_{D2} \quad (7)$$

with:

$$I_{D1} = I_3 - I_4 \quad (8)$$

$$I_{D2} = I_6 - I_5 \quad (9)$$

where I_{D1} (resp. I_{D2}) is the differential current of the differential pair M3-M4 (resp. M5-M6), and I_X is the drain-source current of the MX transistor. Thus, it is now necessary to compute I_{D1} and I_{D2} using the well-known long channel MOS model introduced by Shockley [23] since every MOS length L has been set to $1\mu\text{m}$ according to Fig. 1.a.

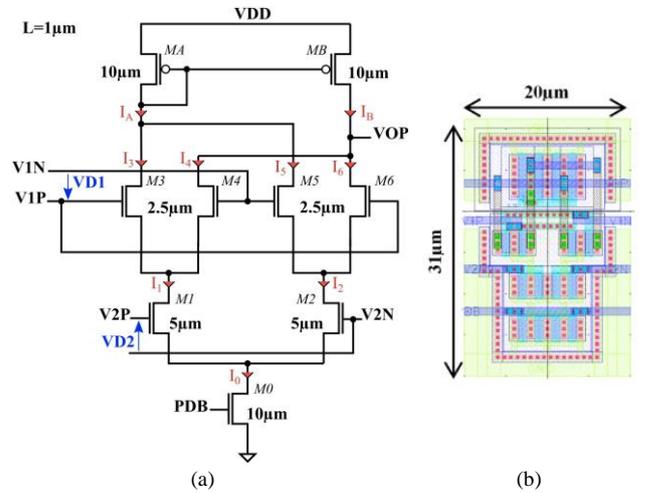


Fig. 1. Transistor level implementation (a) of the designed analog multiplier and its layout implementation (b).

B. Study of the Differential Pairs M3-M4 and M5-M6

In this subsection, the differential pair M3-M4 is firstly considered. Then, using the Kirchhoff's current law, I_1 can be written as follows:

$$I_1 = I_3 + I_4 \quad (10)$$

However, considering (1), M3 (resp. M4) must be in the saturation region of the Shockley's model since the drain-source voltage of M3 (resp. M4) is higher than its gate-source voltage minus the threshold voltage of NMOS transistors. This leads to:

$$I_3 = \frac{\beta_{3-6}}{2} (V_{GS3} - V_{THN})^2 \quad (11)$$

$$I_4 = \frac{\beta_{3-6}}{2} (V_{GS4} - V_{THN})^2 \quad (12)$$

with:

$$\beta_{3-6} = \alpha_{3-6} \frac{W_{3-6}}{L_{3-6}} \approx \alpha_N \frac{W_{3-6}}{L_{3-6}} \quad (13)$$

where W_{3-6} (resp. L_{3-6}) is the width (resp. the length) of transistors from M3 to M6, α_{3-6} and also α_N depends on the charge mobility and the oxide capacitance, V_{GSX} is the gate-source voltage of MX, and V_{TH} is the threshold voltage of NMOS transistors. For the considered 0.35 μm technology and for a MOS length of 1 μm , α_N (resp. α_P) is about 70 $\mu\text{A}/\text{V}^2$ (resp. 28 $\mu\text{A}/\text{V}^2$) and V_{THN} (resp. V_{THP}) is about 0.52 V (resp. 0.77 V) considering threshold voltage extraction methods proposed in [24].

By solving the equation system constituted by (8) and (10), it is possible to write with the help of (11) and (12):

$$I_1 + I_{D1} = \beta_{3-6} (V_{GS3} - V_{THN})^2 \quad (14)$$

$$I_1 - I_{D1} = \beta_{3-6} (V_{GS4} - V_{THN})^2 \quad (15)$$

which enables to write V_{GS3} and V_{GS4} as follows:

$$V_{GS3} = \sqrt{(I_1 + I_{D1}) / \beta_{3-6}} + V_{THN} \quad (16)$$

$$V_{GS4} = \sqrt{(I_1 - I_{D1}) / \beta_{3-6}} + V_{THN}. \quad (17)$$

However, since V_{IP} and V_{IN} can be expressed as follows:

$$V_{IP} = VDD/2 + VDI/2 = V_{GS3} + V_{DS1} + V_{DS0} \quad (18)$$

$$V_{IN} = VDD/2 - VDI/2 = V_{GS4} + V_{DS1} + V_{DS0} \quad (19)$$

with V_{DSX} is the drain-source voltage of MX transistor, the differential input voltage VDI can be written as follows:

$$VDI = V_{GS3} - V_{GS4} = \left(\sqrt{I_1 + I_{D1}} - \sqrt{I_1 - I_{D1}} \right) / \sqrt{\beta_{3-6}}. \quad (20)$$

By supposing:

$$|I_{D1}| \ll I_1 \quad (21)$$

which is true thanks to (18) and (19) while:

$$|VDI| \ll VDD - 2(V_{DS1} + V_{DS0} + V_{THN}) \quad (22)$$

since as detailed in the subsection A appendix, (21) leads to:

$$\begin{cases} 0 \ll 2(V_{GS4} - V_{THN})^2 & \text{if } V_{D1} > 0 \\ 0 \ll 2(V_{GS3} - V_{THN})^2 & \text{if } V_{D1} < 0 \end{cases} \quad (23)$$

and also to:

$$\begin{cases} V_{THN} \ll V_{GS4} & \text{if } V_{D1} > 0, \\ V_{THN} \ll V_{GS3} & \text{if } V_{D1} < 0 \end{cases} \quad (24)$$

(20) becomes:

$$VDI = I_{D1} / \sqrt{\beta_{3-6} I_1} \quad (25)$$

which allows the differential current I_{D1} of the differential pair M3-M4 to be written as follows:

$$I_{D1} = VDI \sqrt{\beta_{3-6} I_1}. \quad (26)$$

By following the same reasoning from (10) to (25) for the differential current I_{D2} of the differential pair M5-M6, I_{D2} can be written as follows:

$$I_{D2} = VDI \sqrt{\beta_{3-6} I_2} \quad (27)$$

which is true while:

$$|VDI| \ll VDD - 2(V_{DS2} + V_{DS0} + V_{THN}). \quad (28)$$

Thus, (7) becomes:

$$I_D = VDI \sqrt{\beta_{3-6}} \left(\sqrt{I_1} - \sqrt{I_2} \right) \quad (29)$$

while (22) and (28) are true and it is also necessary to study the differential pair M1-M2 to link I_D to $VD2$.

C. Study of the Differential Pair M1-M2

In literature, M1 and M2 transistors are usually considered in saturation region which leads to:

$$I_D = \sqrt{\frac{\beta_{3-6} \beta_{1-2}}{2}} \cdot VDI \cdot VD2 \quad (30)$$

since:

$$I_1 = \frac{\beta_{1-2}}{2} (V_{GS1} - V_{THN})^2 \quad (31)$$

$$I_2 = \frac{\beta_{1-2}}{2} (V_{GS2} - V_{THN})^2 \quad (32)$$

with:

$$\beta_{1-2} = \alpha_{1-2} \frac{W_{1-2}}{L_{1-2}} \approx \alpha_N \frac{W_{1-2}}{L_{1-2}} \quad (33)$$

where W_{1-2} (resp. L_{1-2}) is the width (resp. the length) of M1 and M2 transistors, and α_{1-2} depends on the charge mobility and the oxide capacitance.

However, in practical, it is not possible to bias M1 and M2 in saturation region due the stacking of 4 MOS lines between the ground and the voltage supply when the Gilbert multiplier is biased according to (1). Indeed, this biasing requires that:

$$V_{DSX} > V_{DSXsat} = V_{GSX} - V_{THN} \quad (34)$$

where X has to be replaced by 1 or 2 according to the considered transistor is M1 or M2. When applied to M1 and M2, (34) leads, as detailed in the subsection B of the appendix, to the following impossible conditions:

$$VD2 \ll -|VD1| \quad (35)$$

$$VD2 \gg |VD1|, \quad (36)$$

since (22) and (28) combined to (34) can be written as follows:

$$2V_{DS1sat} \ll VDD - |VD1| - 2(V_{DS0} + V_{THN}) \quad (37)$$

$$2V_{DS2sat} \ll VDD - |VD1| - 2(V_{DS0} + V_{THN}) \quad (38)$$

where V_{GSX} and also V_{DSXsat} can be computed with the help of:

$$V2P = VDD/2 + VD2/2 = V_{GS1} + V_{DS0} \quad (39)$$

$$V2N = VDD/2 - VD2/2 = V_{GS2} + V_{DS0}. \quad (40)$$

M1 and M2 can also never be in the saturation region in the same time.

For this reason, it is now considered in this paper that M1 and M2 operate in linear region which leads according to the Shockley model to:

$$I_1 = \beta_{1-2} (V_{GS1} - V_{THN} - V_{DS1}/2) V_{DS1} \quad (41)$$

$$I_2 = \beta_{1-2} (V_{GS2} - V_{THN} - V_{DS2}/2) V_{DS2}. \quad (42)$$

Thus, by supposing that:

$$V_{GS1} - V_{THN} \gg V_{DS1}/2 \quad (43)$$

$$V_{GS2} - V_{THN} \gg V_{DS2}/2 \quad (44)$$

(41) and (42) can be written as follows:

$$I_1 = \beta_{1-2} (V_{GS1} - V_{THN}) V_{DS1} \quad (45)$$

$$I_2 = \beta_{1-2} (V_{GS2} - V_{THN}) V_{DS2}. \quad (46)$$

According to the Fig. 1.a, I_1 and I_2 can be equally written as a function of the bias current I_0 and of the differential current I_{D0} of the differential pair M1-M2:

$$I_1 = (I_0 + I_{D0})/2 \quad (47)$$

$$I_2 = (I_0 - I_{D0})/2 \quad (48)$$

since:

$$I_0 = I_1 + I_2 \quad (49)$$

$$I_{D0} = I_1 - I_2, \quad (50)$$

which allows (29) to be rewritten as follows:

$$I_D = \sqrt{\beta_{3-6}/2} \cdot VD1 \cdot \left(\sqrt{I_0 + I_{D0}} - \sqrt{I_0 - I_{D0}} \right) \quad (51)$$

and simplified to:

$$I_D = \sqrt{\beta_{3-6}/(2I_0)} \cdot VD1 \cdot I_{D0} \quad (52)$$

when:

$$|I_{D0}| \ll I_0 \quad (53)$$

which is true by replacing I_1 , and I_2 in (49) and (50) with their expression given (45) and (46) when:

$$|VD2| \ll VDD - 2(V_{DS0} + V_{THN}) \quad (54)$$

as detailed in the subsection C of the appendix.

Considering the assumptions made on V_{DS1} and V_{DS2} indicated in (43) and (44), it is also possible to assume that V_{DS1} and V_{DS2} have small variations compared to their average values and therefore that:

$$V_{DS1} \approx V_{DS2} \approx (V_{DS1} + V_{DS2})/2 \quad (55)$$

By injecting now (45) and (46) in (50) taking into account (39) and (40), this gives:

$$I_{D0} = \beta_{1-2} \cdot VD2 \cdot (V_{DS1} + V_{DS2})/2 \quad (56)$$

since:

$$VD2 = V_{GS1} - V_{GS2}. \quad (57)$$

Using (52) and (56), the differential current I_D of the analog multiplier can also be written as follows:

$$I_D = \beta_{1-2} \cdot \sqrt{\frac{\beta_{3-6}}{2I_0}} \cdot \frac{V_{DS1} + V_{DS2}}{2} \cdot VD1 \cdot VD2 \quad (58)$$

which demonstrates that the proposed Gilbert cell works as a voltage multiplier while (28) and (54) are true when M3 to M6 operate in saturation region and M1 and M2 in linear region. It can be noted that the drain-source voltage of M0, M1, and M2 should be as low as possible to optimize the input voltage range of the multiplier.

Finally, it is possible to write (58) using only the technology parameters, the biasing current I_0 and V_{DS0} . For this, by now injecting (45) and (46) in (49) and taking into account (39), (40), and (55), I_0 can be written as follows:

$$I_0 = \beta_{1-2} \frac{V_{DS1} + V_{DS2}}{2} (VDD - 2 \cdot [V_{DS0} + V_{THN}]) \quad (59)$$

which leads using (58) and (59) to:

$$I_D = \sqrt{\frac{\beta_{3-6} I_0}{2}} \cdot \frac{1}{VDD - 2 \cdot [V_{DS0} + V_{THN}]} \cdot VD1 \cdot VD2 \quad (60)$$

Thus, the output voltage of the proposed analog multiplier can be written as follows:

$$VOP = VOP_{OFFSET} + K \cdot VD1 \cdot VD2 \quad (61)$$

where K is the gain of the analog multiplier which is equal to:

$$K = \sqrt{\frac{\beta_{3-6} I_0}{2}} \cdot \frac{R_{OUT}}{VDD - 2 \cdot [V_{DS0} + V_{THN}]} \quad (62)$$

and VOP_{OFFSET} is the output offset voltage which is equal to:

$$VOP_{OFFSET} = \frac{VDD}{2}. \quad (63)$$

III. POST-LAYOUT SIMULATIONS OF THE DESIGNED ANALOG MULTIPLIER

The proposed analog multiplier has been implemented using an AMS 0.35 μm CMOS technology with a supply voltage of 3.3 V. Its layout is shown in Fig. 1.b and has a core area of 620 μm^2 . The size and the post-layout simulated operating point of each MOS transistor, which have been initially chosen to obtain a multiplier with an output dynamic of $VDD/2$ (1.65 V) for the $VD1$ and $VD2$ range $[-400 \text{ mV}; +400 \text{ mV}]$ ($K=5.16$), are shown in Tab. I when V_{IP} , V_{IN} , $V2P$, and $V2N$ are set to $VDD/2$ and when PDB is equal to

VDD (3.3 V). These values lead to an output voltage VOP of 1.75 V instead of $VDD/2$ as initially desired in (1). However, this is not an issue since it is just an offset which can be taken into account by increasing the threshold used in the analog processing chain [10]. Finally, operating regions of each transistor are in accordance with the theoretical analysis. The equations and the procedure used to size the MOS transistors of the analog multiplier are respectively detailed in the subsections D and E of the appendix.

To analyze multiplier performances in terms of computing precision, the distribution of its gain K defined in (61) has been studied using post-layout simulations for given ranges of $VD1$ and $VD2$. Indeed, K being extracted as a gain relative to the true multiplication, the less the distribution of K over an input range is wide, the more the multiplier is accurate. Thus, the figure of merit used here is the relative standard deviation (also known as coefficient of variation) of K in percent noted c_{V-K} which is defined, with the help of the average value of K noted μ_K and the standard deviation of K noted σ_K , as follows:

$$c_{V-K} = \frac{\sigma_K}{\mu_K} \times 100. \quad (64)$$

TABLE I. SIZE AND BIASING OF MOS TRANSISTORS USED IN THE DESIGNED MULTIPLIER

MOS	W (μm)	L (μm)	$ I_{DS} $ (μA)	$ V_{GS} $ (V)	$ V_{DS} $ (V)	Region
M0	10	1	275	3.3	0.1	Linear
M1-M2	5	1	138	1.55	0.25	Linear
M3-M6	2.5	1	68.8	1.3	1.4	Saturation
MA-MB	10	1	138	1.55	1.55	Saturation

The output voltage VOP obtained for the range of $VD1$ and $VD2$ defined over the interval $[-400 \text{ mV}; 400 \text{ mV}]$ is shown in Fig. 2 when $VD1$ is independent of $VD2$. From this curves network, the distribution of K for different ranges of $VD1$ and $VD2$, which are $[-100 \text{ mV}; 100 \text{ mV}]$, $[-200 \text{ mV}; 200 \text{ mV}]$ and $[-400 \text{ mV}; 400 \text{ mV}]$, has been extracted and results are shown in Tab. II. It also appears that μ_K is relatively stable over the ranges since it is between 4.51 and 4.60. Moreover, σ_K and c_{V-K} , decreases as the ranges of $VD1$ and $VD2$ are reduced. This was expected since the more the ranges of $VD1$ and $VD2$ are small, the more the conditions seen during the theoretical study on $VD1$ and $VD2$ are true. Furthermore, for the range $[-400 \text{ mV}; 400 \text{ mV}]$ corresponding to the worst case, c_{V-K} which represents the mean computing precision of the multiplier is 5.72%. Finally, the theoretical conditions on the voltage ranges of $VD1$ and $VD2$ allowing multiplier operation of the proposed circuit are verified since $VD1$ (resp. $VD2$) is small in front 1.5V (resp. 2V) according to (28) (resp. (54)).

Since the proposed analog multiplier has to be used in an energy detector, the distribution of the gain K has been equally studied when it works as a squaring stage, or in other words, when $VD1$ is equal to $VD2$. The output voltage VOP obtained for the $VD1$ range (and also $VD2$ range) $[-500 \text{ mV}; 500 \text{ mV}]$ is shown in Fig. 3. To verify that the circuits operates as a true square function, the curve of an ideal squarer having a gain of 4.5 has been plotted on the same figure. It appears that the curves are very close to each other as confirmed by the analysis of the distribution of K indicated in Tab. III. Indeed, it appears that for the interval $[-400 \text{ mV}; 400 \text{ mV}]$, μ_K value is 4.50 and c_{V-K} (mean computing

precision of the squarer) is only 1.14% which is better than the 5.72% obtained in multiplier mode.

Finally, the multiplier output has a slew rate of $0.56 \text{ V}/\mu\text{s}$ on a capacitive load of 10 pF for a simultaneous step of $VD1$ and $VD2$ from 0 V to 0.4 V . According to Tab. I, the current consumed by the multiplier is $275 \mu\text{A}$ (i.e. a power consumption of 0.91 mW) when it is turned-on ($PDB = VDD$), but it is only 5 pA (i.e. a power consumption of 16.5 pW) when it is turned off ($PDB = 0 \text{ V}$). Thanks to its output slew rate and its very low power consumption when it is turned-off, it is therefore possible to use a power management scheme which consists in turning-off the circuits as soon as they have accomplished their task [25][26] using a PDB signal considered here external. Thus, assuming that it is possible to compute the multiplication using the proposed circuit and to store the result in a capacitor in less than $10 \mu\text{s}$, the multiplier would be turned-on with a duty cycle of only $250/100\ 000$ (0.25%) since 250 Hz is a sufficient sampling frequency to detect pulses centred around 10 Hz which are synchronized with heart beats in electrocardiograms [27]. In this case, the average power consumption of the proposed analog multiplier would be only $2.28 \mu\text{W}$ without considering the additional power consumption required by the PDB generation circuit. Tab. IV compares the designed multiplier with other works.

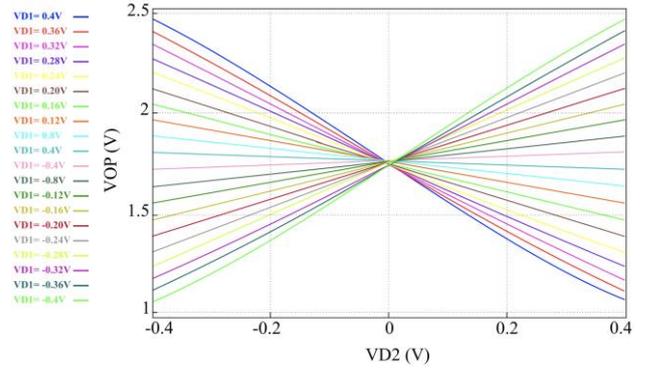


Fig. 2. DC transfer characteristics of the proposed analog multiplier for a high impedance output load when $VD1$ and $VD2$ are independent.

TABLE II. SIMULATED DISTRIBUTION OF K FOR A HIGH IMPEDANCE OUTPUT LOAD, WHEN $VD1$ AND $VD2$ ARE INDEPENDENT

$VD1$ and $VD2$ range	μ_K	σ_K	c_{V-K} (%)
$[-100 \text{ mV}; +100 \text{ mV}]$	4.51	0.12	2.59
$[-200 \text{ mV}; +200 \text{ mV}]$	4.54	0.18	3.86
$[-400 \text{ mV}; +400 \text{ mV}]$	4.60	0.26	5.72

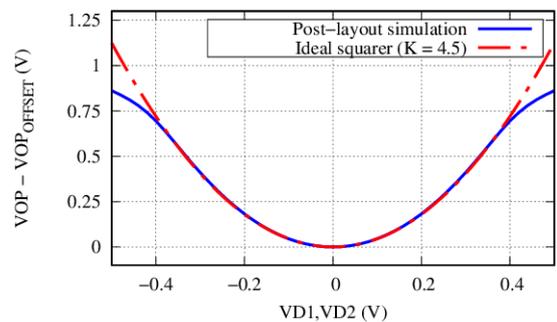


Fig. 3. DC transfer characteristic of the proposed analog multiplier for a high impedance output load when $VD1$ is equal to $VD2$.

TABLE III. SIMULATED DISTRIBUTION OF K FOR A HIGH IMPEDANCE OUTPUT LOAD WHEN $VD1$ IS EQUAL TO $VD2$.

VD1 and VD2 range	μ_K	σ_K	c_{V-K} (%)
[-100 mV;+100 mV]	4.49	6.48e-3	0.14
[-200 mV;+200 mV]	4.50	18.9e-3	0.42
[-400 mV;+400 mV]	4.50	51.2e-3	1.14

IV. ANALOG IMPLEMENTATION OF THE SQUARE FUNCTION

As indicated in the introduction, the usual nonlinear transformation used in an energy detector is the square function. In this section, the designed multiplier is also used to implement the square function by an analog manner. However, the designed multiplier has a single output but two differential inputs. To use it as an analog square function which has a single input, op-amp based subtractors with $R=100\text{ k}\Omega$ have been implemented on chip before the multiplier as shown on Fig. 4. They also allow the single input having an offset of $VDD/2$ (1.65 V) to be transformed to a symmetrical input around $VDD/2$. Furthermore, $V1P$ and $V2P$ as well as $V1N$ and $V2N$ have been connected together to have $VD1$ equal to $VD2$ and thus, to use the multiplier as a square function. Finally, op-amp based followers have been implemented to isolate the square function from input source and output load. It can be noted that all used op-amps are standard IPs of the $0.35\text{ }\mu\text{m}$ AMS design kit, which have led to a core area of 0.9 mm^2 for the full squarer. The obtained square function is also not optimal in terms of space and power consumption since its goal is just to highlight the multiplier performances in terms of input voltage range and precision.

The DC transfer characteristic of the implemented square function has been measured and compared to the ideal response of a square function having a gain of 3.5 in Fig. 5. It appears that the curves are close to each other for $VD1$ range [-400 mV;400 mV]. However, compared to the post-layout simulations of the stand-alone multiplier, the gain has decreased from 4.5 to 3.5 due to process variations and the additional load introduced by the op-amp based functions. About the distribution of K , it appears that the measured relative standard deviation c_{V-K} of the gain K has increased from 1.14% to 2.93% for the $VD1$ range [-400 mV;400 mV] according to Tab. V. Moreover, unlike post-layout simulations of the stand-alone multiplier, c_{V-K} increases for as the $VD1$ range decreases. These both phenomena are due to the observed output noise when $VD1$ is near to 0 V since the square of a near zero value is lower than this near zero value. Finally, transient response of the squarer for a 1 kHz triangular voltage input is shown in Fig. 6 and follows well the DC characteristic. In addition, the impulse response of the squarer is given in Fig. 7 and shows an overshoot of 66% and a response time defined at 5% around the final output step equals to $5\text{ }\mu\text{s}$. Unfortunately, the power consumption of the multiplier alone has not been verified since other circuits are connected on the same VDD pin. Nevertheless, the measured active (resp. stand-by) power consumption of the square function shown in Fig. 4 is 5.31 mW (resp. 1.00 nW).

TABLE IV. MULTIPLIER COMPARISON WITH OTHER WORKS

Ref	Tech. (nm)	VDD (V)	Input range	Bandwidth	Power cons.
[12]	90	1.2	$\pm 60\text{ mV}$	331 kHz @ $5\text{ k}\Omega/10\text{ pF}$	$6.92\text{ }\mu\text{W}$
[28]	250	± 1	$\pm 0.75\text{ V}$	16 MHz @ $1\text{ k}\Omega/10\text{ pF}$	0.326 mW
[29]	350	2	$\pm 40\text{ nA}$	Neural range	$7.2\text{ }\mu\text{W}$
This work	350	3.3	$\pm 400\text{ mV}$	100 kHz @ $10\text{ k}\Omega/10\text{ pF}^a$	$908\text{ }\mu\text{W}^b$ 16.5 pW^c

^a 1dB bandwidth
^b Active power consumption
^c Stand-by power consumption

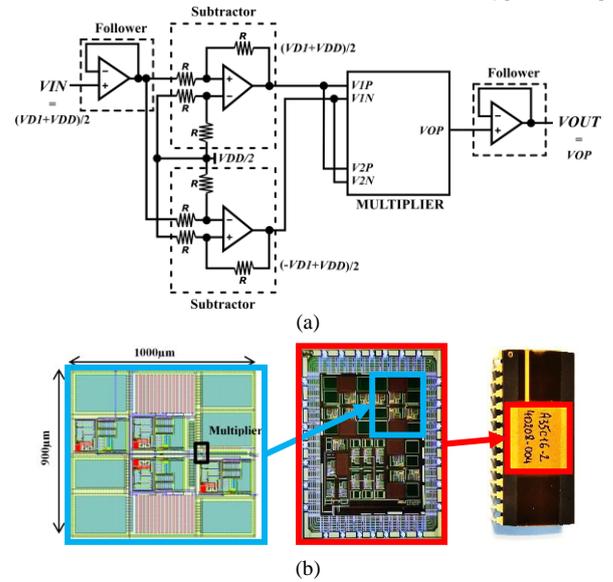


Fig. 4. Implemented square function based on the designed multiplier: schematic (a) ; layout implementation, chip photography and package photography (b).

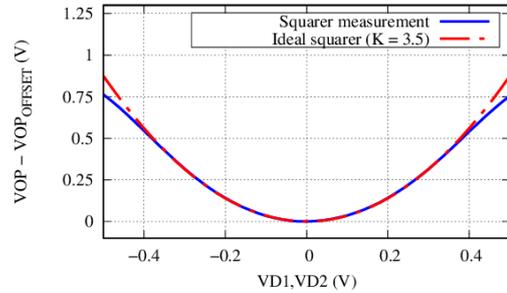


Fig. 5. DC transfer characteristic of the designed analog square function based on the proposed multiplier for a high impedance output load.

TABLE V. MEASURED DISTRIBUTION OF K FOR A HIGH IMPEDANCE OUTPUT LOAD WHEN $VD1$ IS EQUAL TO $VD2$

VD1 and VD2 range	μ_K	σ_K	c_{V-K} (%)
[-100 mV;+100 mV]	3.59	210e-3	5.86
[-200 mV;+200 mV]	3.56	136e-3	3.83
[-400 mV;+400 mV]	3.52	103e-3	2.93

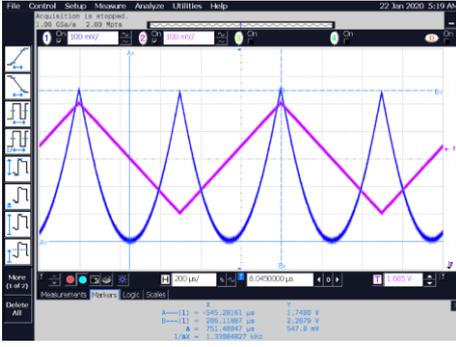


Fig. 6. Transient response of the analog square function for a 1 kHz triangular voltage input (0.4 Vpp around $V_{DD}/2=1.65$ V) on a high impedance output load.

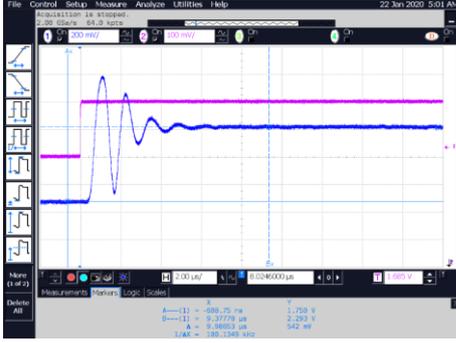


Fig. 7. Impulse response of the analog square function for a 1kHz square voltage input ($V_{LOW} = V_{DD}/2 = 1.65$ V, $V_{HIGH} = V_{DD}/2 + 0.2 = 1.85$ V) on a high impedance output load.

V. THE TEAGER ENERGY OPERATOR

Considering the context of energy detection, the square function can be replaced by other nonlinear transformations. One of them is the TEO which is defined considering continuous time as follows:

$$\psi[x(t)] = [x'(t)]^2 - x(t) \cdot x''(t) \quad (65)$$

where $\psi[x(t)]$ represents the energy of $x(t)$, $x'(t)$ and $x''(t)$ being respectively the first and second derivatives of $x(t)$.

A. TEO discrete time definition

Eq. 65 is generally defined in discrete time for digital computing such as in [17] as follows:

$$\psi[x(n)] = x(n)^2 - x(n+1) \cdot x(n-1) \quad (66)$$

which leads to a non-causal system. Although this is common in digital systems, this is not the case for analog ones where causal systems are preferred. Moreover, this formulation implicitly uses frequencies normalized by the sampling frequency which hides effects of the sampling frequency on the TEO response magnitude such as in [14].

To define it in discrete time using a causal equation, and especially without using normalized frequencies, it is firstly necessary to discretize the time by replacing t by $n \cdot T_s$ where n is the sample number and T_s the sampling period. Eq. (65) can also be written as follows:

$$\psi[x(n \cdot T_s)] = [x'(n \cdot T_s)]^2 - x(n \cdot T_s) \cdot x''(n \cdot T_s). \quad (67)$$

Next, since the first derivative of $x(n \cdot T_s)$ can be written:

$$x'(n \cdot T_s) = \frac{x(n \cdot T_s) - x([n-1] \cdot T_s)}{T_s}, \quad (68)$$

the second derivative of $x(n \cdot T_s)$ which is equal to:

$$x''(n \cdot T_s) = \frac{x'(n \cdot T_s) - x'([n-1] \cdot T_s)}{T_s}, \quad (69)$$

can be expressed as follows:

$$x''(n \cdot T_s) = \frac{x(n \cdot T_s) - 2 \cdot x([n-1] \cdot T_s) + x([n-2] \cdot T_s)}{T_s^2}. \quad (70)$$

Then, by injecting now (68) and (70) in (67), the TEO can be defined in discrete time as follows:

$$\psi[x(n \cdot T_s)] = \frac{[x([n-1] \cdot T_s)]^2 - x(n \cdot T_s) \cdot x([n-2] \cdot T_s)}{T_s^2} \quad (71)$$

and also depends on the sampling period T_s .

B. Effect of the sampling frequency on the TEO response magnitude

To show the effect of the sampling frequency on the TEO response magnitude, it is possible to consider a sinusoidal input signal which can be defined as follows:

$$x(n \cdot T_s) = A \cos(2\pi f \cdot n \cdot T_s) \quad (72)$$

where A and f are respectively its magnitude and its frequency. By injecting (72) in (71), the output of the TEO can be written considering discrete time as follows:

$$\psi[x(n \cdot T_s)] = \left[\frac{A}{T_s} \sin(2\pi f \cdot T_s) \right]^2. \quad (73)$$

It can be noticed that the result is independent of n and therefore the TEOs output signal is constant whatever the considered discretized time. In addition, it provides a continuous signal whose amplitude is directly proportional to the amplitude of the squared input sinusoid, which is proportional to its energy. The output of the TEO as expressed in (73) is shown in Fig. 8 as a function of the sampling frequency F_s for A equal to 1 and a fixed frequency f equal to 10 Hz (this value corresponds approximately to the central frequency of heartbeat-synchronized pulses in electrocardiograms [27]).

However, this is not its only particularity. Indeed, it can be seen in Fig. 8 that TEO response magnitude depends on the sampling frequency and that it reaches respectively 90% (resp. 95%) of the maximum possible amplitude for a sampling frequencies of $8 \cdot f$ (resp. $11 \cdot f$). Thus, the TEO requires at least a sampling frequency about $10 \cdot f$ to keep a high dynamic on its output. In the context of compact battery-powered devices, a good compromise can also be done between TEO response magnitude and power consumption if the frequency of the input signal is known since the less the sampling frequency is, the less the power consumption is.

Finally, to be more familiar with the meaning of the TEO continuous time equation (65) which seems not obvious at first sight, the limit computation of (73) when the sampling period T_s tends to zero can be done and is equal to:

$$\lim_{T_s \rightarrow 0} \psi[x(n \cdot T_s)] = [A \cdot 2\pi f]^2. \quad (74)$$

Therefore, if a high sampling frequency is used, the TEO will amplify the energy of the high-frequency components proportionately to their squared frequency. Thus, the TEO highlights the energy of the high-frequency components and also acts as a high-pass filter behavior. It is also possible to say that the TEO harmonic response is the same than an amplifier having a gain proportional to its input frequency, followed by a squarer function and an envelope detector.

VI. ANALOG IMPLEMENTATION OF THE TEAGER ENERGY OPERATOR IN DISCRETE TIME

In this section, the designed multiplier is also used here to implement the TEO by an analog manner. However, conversely of previous works [18][19], its discrete time formulation given in (66), which is proportional to (71) for a constant sampling frequency, is implemented instead of its continuous time formulation given in (65). Indeed, derivatives introduced by (65) are more difficult to implement than shifted samples of the input signal introduced by (66). Thus, the new analog approach followed here is to generate the required shifted samples, and to send them into two analog multipliers and one analog subtractor. The used technology is still the CMOS 0.35 μm from AMS with a voltage supply of 3.3 V and the used operational amplifiers have been taken from AMS IP library as for the square function.

A. Differential Shifted Samples Generator Design

As the designed multiplier requires symmetrical voltages with respect to $VDD/2$ on its inputs, a single to differential shifted samples generator shown in Fig. 9 has been designed. Its first stage is a voltage follower which provides a copy of VIN to the subtractors where VIN can be defined as follows:

$$VIN = VDD/2 + VD/2 \quad (75)$$

with VD the voltage to process using the TEO. Next, subtractors generate $VINP$ which is a copy of the VIN node voltage, and $VINN$ which is its symmetrical with respect to $VDD/2$. Thus, they are respectively equal to:

$$VINP = VDD/2 + VD/2 \quad (76)$$

$$VINN = VDD/2 - VD/2. \quad (77)$$

To make a compromise between input impedance of the subtractors, power consumption of the voltage follower, and silicon area of the ASIC, R has been fixed to 100 k Ω . Finally, the $VINP$ and $VINN$ signals goes separately into three sample and hold circuits in series. This allows the three samples required by the discrete time TEO equation (70) to be generated (three for $VINP$ and three for $VINN$). These samples are called $VP(n)$, $VP(n-1)$, $VP(n-2)$, $VN(n)$, $VN(n-1)$, and $VN(n-2)$ which enables identification with (70).

B. TEO Implementation

According to (71), the TEO has been implemented using two instances of designed multiplier, and one subtractor as shown in Fig. 10. To isolate multipliers from the subtractor, voltage followers which provides a copy of their input have been inserted. To keep low silicon area and power consumption, R has been equally fixed to 100 k Ω . Finally, to allow all electronic functions to be turned-off and also reduce

power consumption, a sample & hold circuit has been added on the subtractors output to memorize $VOUT$ when the different parts of the circuit are turned-off.

C. Design and Synchronisation of Sample & Hold Circuits

The sample & hold circuits, used in Fig. 9 and Fig. 10, are the same and shown in Fig. 11. The sample function is realized on a CMOS transmission gate where PMOS and NMOS have the same size. The hold function is obtained with a capacitor of 10 pF. A CMOS inverter has been added to generate $CLK\backslash$ from the clock CLK , both being required by the transmission gate. Finally, a voltage follower is placed on the output in order to minimize capacitor current leakage. To synchronize properly the different sample & hold circuits, it is necessary to control them as shown in Fig. 12. Thus, the first sample & hold circuit which must be enabled is the one driven by $CLK4$ as shown in Fig. 10. Obviously, this supposes that the different $VX(y)$ have properly been initialized one time at least where X can be P , or N and y can be n , $n-1$, or $n-2$. To do this, the sample & hold circuits shown in Fig. 9 have to be activated from the outputs to the inputs using $CLK3$ to $CLK1$.

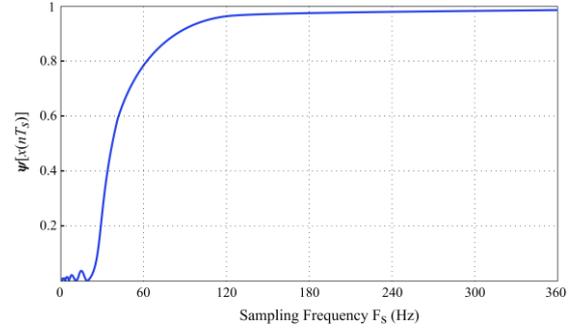


Fig. 8. Representation of the TEO's output according to the sampling frequency F_S , for a sine input signal having a magnitude equal to 1 and a frequency equal to 10 Hz.

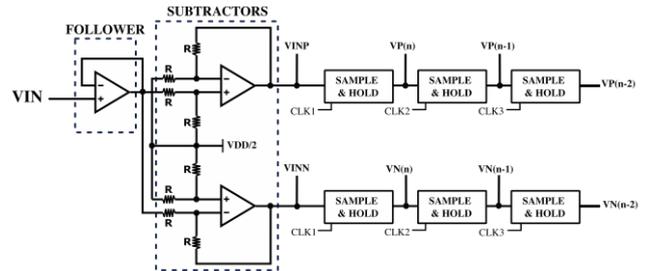


Fig. 9. Design of the single to differential shifted samples generator.

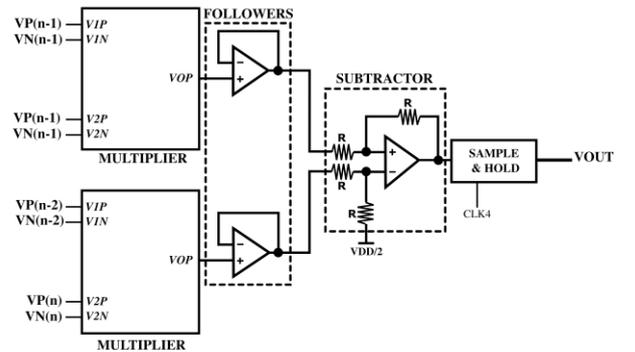


Fig. 10. Design of the Teager Energy Operator.

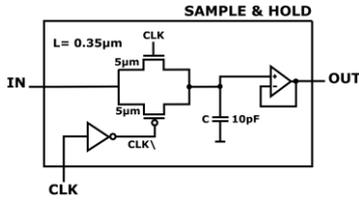


Fig. 11. Design of the sample and hold circuit.

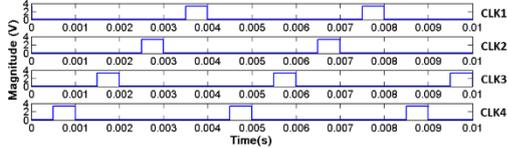


Fig. 12. Clocks synchronization chronogram

D. Post-layout Simulations and Measurement Results

The proposed TEO implementation has been post-layout simulated and manufactured using the 0.35 μm CMOS design kit from AMS as indicated earlier. Its layout is shown in Fig. 13 and has a core area of 2.2 mm^2 . From post-layout simulations, its power consumption is about 6.21 mW (resp. 1.43 nW) when it is turned-on (resp. turned-off). However, this turned-on power consumption has not been optimized since lots of cells come from AMS IP libraries. Fortunately, similarly to the designed multiplier, the global power consumption can be reduced by using a power gating strategy which consists to turned-off circuits as much as possible.

To validate TEO operation before manufacturing, a clean electrocardiogram has been applied on V_{IN} . Results obtained with a sampling frequency of 250 Hz using post-layout simulations are shown in Fig. 14. It shows that the differential shifted samples generator works as well as our expectations and that a peak of 50 mV is obtained on V_{OUT} when a typical pulse synchronized with heartbeats in electrocardiogram, having a peak voltage of 100 mV from its baseline, occurs on V_{IN} .

In Fig. 15, the TEO output V_{OUT} has been measured when an electrocardiogram from MIT-BIH database [30] available on Physionet [31] is applied on V_{IN} . It appears that the TEO generates one peak voltage for each pulse synchronized with heartbeats in the electrocardiogram as expected. Thus, it generates until 250 mV spikes when 200 mV pulses are applied on its input.

E. Comparison with the analog square function

In Fig. 16, the analog square function has been measured using the same electrocardiogram used for Fig. 15. It appears

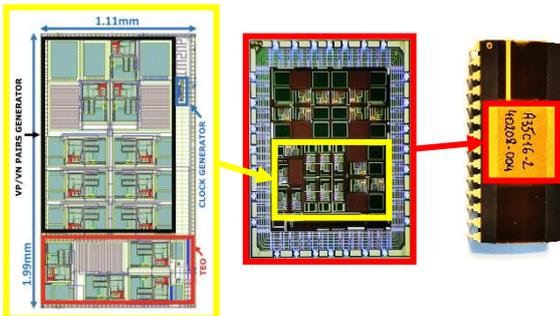


Fig. 13. Layout implementation, chip photography and package photography of the implemented TEO.

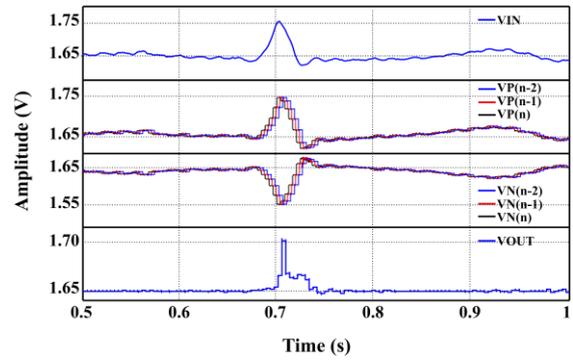


Fig. 14. Post-layout simulations results of the implemented TEO when a pulse synchronized with heartbeats in electrocardiogram occurs on V_{IN} .

that the analog square function also generates one peak voltage for each pulse synchronized with heartbeats in the tested electrocardiogram. Moreover, Fig. 16 shows that it generates until 700 mV spikes when 200 mV pulses are applied on its input. Thus, compared to the TEO, the squarer output dynamic is higher for an input pulse having a fixed magnitude. However, the square function response is the same for all frequencies whereas the TEO is not sensitive to low and slow pulses which can be seen before each high and fast pulses. Finally, the designed analog TEO based on the discrete time equation is compared in Tab. VI to other analog TEOs based on the continuous time equation. Even if the proposed TEO has a higher active power consumption, it can be shutdown most of the time where it consumes only 1.43 nW, thanks to the use of the discrete time equation and the multiplier ability to be easily shutdown.



Fig. 15. Measurement results of the TEO output V_{OUT} (channel 1 in red) when pulses synchronized with heartbeats in electrocardiogram occur on V_{IN} (channel 2 in yellow). Y-axis scale is equal to 100 mV/div for both channels and x-axis scale is equal to 1 s/div.



Fig. 16. Measurement results of the analog square function output (channel 1 in red; Y-axis scale = 200mV/div) when pulses synchronized with heartbeats in electrocardiogram occur on V_{IN} (channel 2 in yellow; Y-axis scale = 100mV/div). X-axis scale is equal to 1s/div.

TABLE VI. TEO COMPARISON WITH OTHER WORKS

Ref.	Tech. (nm)	VDD (V)	Input range	Bandwidth	Power cons.
[18]	350	± 1.65	± 0.9 V	10 Hz – 10.5 kHz	2.72 μ W
[19]	130	0.5	2 mV	12 kHz	0.26 μ W
[32]	130	1	± 1.166 V	100 Hz – 5 kHz	0.96 μ W
[33]	90	-	20 – 350 mV _{pp}	1 GHz	2.6 mW
This work	350	3.3	± 400 mV	100 kHz	6.21 mW ^d ; 1.43 nW ^e

^d. Active power consumption^e. Stand-by power consumption

VII. CONCLUSION

This paper has focused on the design of two analog nonlinear transformations dedicated to energy detection: the square function and the Teager Energy Operator (TEO). Both requiring an analog multiplier, the design equations of a MOS Gilbert cell have been determined in order to operate around the mid supply voltage. Considering this, an analog multiplier, having a differential input range of ± 400 mV, has been designed using an AMS 0.35 μ m technology and a voltage supply (VDD) of 3.3 V. It has a core area of 620 μ m² and offers power-gating capability, which allows a power consumption of 2.28 μ W when a duty cycle of 0.25% is considered. Next, an analog square function and an analog TEO, have been implemented using the designed Gilbert cell. The analog square function has a core area of 0.9 mm² and measurement results have shown that it is able to compute the square value of its differential input voltage with a mean precision of 2.92% in 5 μ s assuming a differential input voltage of ± 400 mV with a common voltage of VDD/2. Moreover, it is able to generate 700 mV spikes when 200 mV pulses are applied on its input. Finally, the designed analog TEO has been implemented using its discrete time equation instead of its continuous time equation since it does not require derivatives computing. It has a core area of 2.2 mm², an active power consumption of 6.21 mW and a standby power consumption of 1.43 nW. Measurement results have shown that it is able to generate only 250 mV spikes when 200 mV pulses are applied on its input but it is less sensitive to low frequency signals.

APPENDIX

In this appendix, the computation which allows equations (22), (35), (36), and (54) to be obtained are detailed.

A. Detailed calculation to obtain (22)

As reminder, (21) is:

$$|I_{DI}| \ll I_1 \quad (21)$$

and can equally be written as follows:

$$|2 \cdot I_{DI}| \ll 2 \cdot I_1 \quad (78)$$

Thus, using (14) and (15) which are:

$$I_1 + I_{DI} = \beta_{3-6} (V_{GS3} - V_{THN})^2 \quad (14)$$

$$I_1 - I_{DI} = \beta_{3-6} (V_{GS4} - V_{THN})^2, \quad (15)$$

(78) becomes:

$$|(V_{GS3} - V_{THN})^2 - (V_{GS4} - V_{THN})^2| \ll (V_{GS3} - V_{THN})^2 + (V_{GS4} - V_{THN})^2. \quad (79)$$

Now, if it is assumed that:

$$(V_{GS3} - V_{THN})^2 > (V_{GS4} - V_{THN})^2 \quad (80)$$

and also according to (20) that:

$$VDI = V_{GS3} - V_{GS4} > 0, \quad (81)$$

(79) becomes:

$$(V_{GS3} - V_{THN})^2 - (V_{GS4} - V_{THN})^2 \ll (V_{GS3} - V_{THN})^2 + (V_{GS4} - V_{THN})^2. \quad (82)$$

This allows to write (23) as follows:

$$0 \ll 2(V_{GS4} - V_{THN})^2 \quad (23)$$

and also (24) which is:

$$V_{THN} \ll V_{GS4}. \quad (24)$$

Next, using (19) which is:

$$VIN = VDD/2 - VDI/2 = V_{GS4} + V_{DSI} + V_{DSO}, \quad (19)$$

V_{GS4} can be written as follows:

$$V_{GS4} = VDD/2 - VDI/2 - V_{DSI} - V_{DSO}. \quad (83)$$

Thus, if V_{GS4} is replaced in (24) by its equation given in (83), it is possible to write:

$$V_{THN} \ll VDD/2 - VDI/2 - V_{DSI} - V_{DSO} \quad (84)$$

which leads to:

$$VDI \ll VDD - 2(V_{DSI} + V_{DSO} + V_{THN}). \quad (85)$$

Now, if it is assumed that:

$$(V_{GS3} - V_{THN})^2 < (V_{GS4} - V_{THN})^2 \quad (86)$$

and also according to (20) that:

$$VDI = V_{GS3} - V_{GS4} < 0, \quad (87)$$

(79) becomes:

$$-(V_{GS3} - V_{THN})^2 + (V_{GS4} - V_{THN})^2 \ll (V_{GS3} - V_{THN})^2 + (V_{GS4} - V_{THN})^2 \quad (88)$$

This allows to write:

$$0 \ll 2(V_{GS3} - V_{THN})^2 \quad (89)$$

and also:

$$V_{THN} \ll V_{GS3}. \quad (90)$$

Next, using (18) which is:

$$VIP = VDD/2 + VDI/2 = V_{GS3} + V_{DSI} + V_{DSO}, \quad (18)$$

V_{GS3} can be written as follows:

$$V_{GS3} = VDD/2 + VDI/2 - V_{DSI} - V_{DSO}. \quad (91)$$

Thus, if V_{GS3} is replaced in (90) by its equation given in (91), it is possible to write:

$$V_{THN} \ll VDD/2 + VDI/2 - V_{DSI} - V_{DSO} \quad (92)$$

which leads to:

$$-VDI \ll VDD - 2(V_{DS1} + V_{DS0} + V_{THN}). \quad (93)$$

Finally, if (85) and (93) are associated, it is possible to write (22) as follows:

$$|VDI| \ll VDD - 2(V_{DS1} + V_{DS0} + V_{THN}). \quad (22)$$

B. Detailed calculation to obtain (35) and (36)

As reminder, (22) and (28) are:

$$|VDI| \ll VDD - 2(V_{DS1} + V_{DS0} + V_{THN}) \quad (22)$$

$$|VDI| \ll VDD - 2(V_{DS2} + V_{DS0} + V_{THN}) \quad (28)$$

and can be rewritten as follows:

$$2V_{DS1} \ll VDD - |VDI| - 2(V_{DS0} + V_{THN}) \quad (94)$$

$$2V_{DS2} \ll VDD - |VDI| - 2(V_{DS0} + V_{THN}) \quad (95)$$

Next, since (34) is:

$$V_{DSX} > V_{DSXsat} = V_{GSX} - V_{THN} \quad (34)$$

where X has to be replaced by 1 or 2 according to the considered transistor is M1 or M2, it is possible to write:

$$V_{DS1} > V_{DS1sat} = V_{GS1} - V_{THN} \quad (96)$$

$$V_{DS2} > V_{DS2sat} = V_{GS2} - V_{THN} \quad (97)$$

which leads to (37) and (38):

$$2V_{DS1sat} \ll VDD - |VDI| - 2(V_{DS0} + V_{THN}) \quad (37)$$

$$2V_{DS2sat} \ll VDD - |VDI| - 2(V_{DS0} + V_{THN}). \quad (38)$$

Using (96) and (97), (37) and (38) can be written as follows:

$$2(V_{GS1} - V_{THN}) \ll VDD - |VDI| - 2(V_{DS0} + V_{THN}) \quad (98)$$

$$2(V_{GS2} - V_{THN}) \ll VDD - |VDI| - 2(V_{DS0} + V_{THN}). \quad (99)$$

Now, thanks to (39) and (40) which are:

$$V2P = VDD/2 + VD2/2 = V_{GS1} + V_{DS0} \quad (39)$$

$$V2N = VDD/2 - VD2/2 = V_{GS2} + V_{DS0} \quad (40)$$

it is possible to formulate V_{GS1} and V_{GS2} as follows:

$$V_{GS1} = VDD/2 + VD2/2 - V_{DS0} \quad (100)$$

$$V_{GS2} = VDD/2 - VD2/2 - V_{DS0}. \quad (101)$$

Finally, using (100) and (101), (98) and (99) becomes:

$$VD2 \ll -|VDI| \quad (102)$$

$$-VD2 \ll -|VDI| \quad (103)$$

which lead to (35) and (36):

$$VD2 \ll -|VDI| \quad (35)$$

$$VD2 \gg |VDI|. \quad (36)$$

Thus, if (81) is assumed which implies that:

$$VDI = V_{GS3} - V_{GS4} > 0, \quad (81)$$

(35) and (36) can be written as follows:

$$VD2 \ll -VDI \quad (104)$$

$$VD2 \gg VDI \quad (105)$$

which cannot simultaneously be true. Now, if (87) is assumed which implies that:

$$VDI = V_{GS3} - V_{GS4} < 0, \quad (87)$$

(35) and (36) can be written as follows:

$$VD2 \ll VDI \quad (106)$$

$$-VD2 \gg VDI \quad (107)$$

which cannot simultaneously be true too.

C. Detailed calculation to obtain (54)

As reminder, (53) is:

$$|I_{D0}| \ll I_0. \quad (53)$$

Using (49) and (50) which are:

$$I_0 = I_1 + I_2 \quad (49)$$

$$I_{D0} = I_1 - I_2, \quad (50)$$

it is possible to write (53) as follows:

$$|I_1 - I_2| \ll I_1 + I_2. \quad (108)$$

Thus, using (45) and (46) which are:

$$I_1 = \beta_{1-2} (V_{GS1} - V_{THN}) V_{DS1} \quad (45)$$

$$I_2 = \beta_{1-2} (V_{GS2} - V_{THN}) V_{DS2}, \quad (46)$$

(108) becomes:

$$\begin{aligned} |(V_{GS1} - V_{THN}) V_{DS1} - (V_{GS2} - V_{THN}) V_{DS2}| \\ \ll \\ (V_{GS1} - V_{THN}) V_{DS1} + (V_{GS2} - V_{THN}) V_{DS2} \end{aligned} \quad (109)$$

Now, if it is assumed that:

$$(V_{GS1} - V_{THN}) V_{DS1} > (V_{GS2} - V_{THN}) V_{DS2} \quad (110)$$

and also according to (57) that:

$$VD2 = V_{GS1} - V_{GS2} > 0, \quad (111)$$

(109) becomes:

$$\begin{aligned} (V_{GS1} - V_{THN}) V_{DS1} - (V_{GS2} - V_{THN}) V_{DS2} \\ \ll \\ (V_{GS1} - V_{THN}) V_{DS1} + (V_{GS2} - V_{THN}) V_{DS2} \end{aligned} \quad (112)$$

and allows to write:

$$0 \ll 2(V_{GS2} - V_{THN}) V_{DS2}. \quad (113)$$

However, since (44) is:

$$V_{GS2} - V_{THN} \gg V_{DS2}/2, \quad (44)$$

(113) can be written as follows:

$$0 \ll 2(V_{GS2} - V_{THN}) \quad (114)$$

and becomes using (101):

$$VD2 \ll VDD - 2(V_{DS0} + V_{THN}). \quad (115)$$

Now, if it is assumed that:

$$(V_{GS1} - V_{THN})V_{DS1} < (V_{GS2} - V_{THN})V_{DS2} \quad (116)$$

and also according to (57) that:

$$VD2 = V_{GS1} - V_{GS2} < 0, \quad (117)$$

(109) becomes:

$$\begin{aligned} & -(V_{GS1} - V_{THN})V_{DS1} + (V_{GS2} - V_{THN})V_{DS2} \\ & \ll \\ & (V_{GS1} - V_{THN})V_{DS1} + (V_{GS2} - V_{THN})V_{DS2} \end{aligned} \quad (118)$$

and allows to write:

$$0 \ll 2(V_{GS1} - V_{THN})V_{DS1}. \quad (119)$$

However, since (43) is:

$$V_{GS1} - V_{THN} \gg V_{DS1}/2, \quad (44)$$

(119) can be written as follows:

$$0 \ll 2(V_{GS1} - V_{THN}). \quad (120)$$

and becomes using (100):

$$-VD2 \ll VDD - 2(V_{DS0} + V_{THN}), \quad (121)$$

Finally, if (115) and (121) are associated, it is possible to write (54) as follows:

$$|VD2| \ll VDD - 2(V_{DS0} + V_{THN}). \quad (54)$$

D. Design equations of the multiplier

As reminder, the circuit is biased as follows:

$$VOP = \frac{VDD}{2} \text{ when } VIP = VIN = V2P = V2N = \frac{VDD}{2}. \quad (1)$$

In this case, transistors MA, MB, M3, M4, M5, and M6 must be in saturation region whereas M0, M1, and M2 must be in linear region. As the multiplier is switched-on when the M0 gate source voltage PDB is equal to VDD, the active current I_0 using the Shockley model is given by:

$$I_0 = \beta_0 \left(VDD - V_{THN} - \frac{V_{DS0}}{2} \right) V_{DS0} \quad (122)$$

with:

$$\beta_x = \alpha_x \frac{W_x}{L_x} \quad (123)$$

where W_x (resp. L_x) is the width (resp. length) of the transistor MX, α_x depends on the charge mobility and the oxide capacitance, and V_{THN} is the threshold voltage of NMOS transistors.

However, since the current I_0 is equally shared between MA and MB, their source-drain current using the Shockley model is equal to:

$$I_{A-B} = \frac{I_0}{2} = \frac{\beta_{A-B}}{2} \left(\frac{VDD}{2} - |V_{THP}| \right)^2 (1 + \lambda_{A-B} \cdot |V_{DSA-B}|) \quad (124)$$

with λ_{A-B} is the channel-length modulation parameter of MA and MB transistors, V_{THP} is the threshold voltage of PMOS

transistors, and V_{DSA-B} is equal to $VDD/2$. The current I_0 is also equally shared between M3, M4, M5, and M6 which leads using the Shockley model to:

$$I_{3-6} = \frac{I_0}{4} = \frac{\beta_{3-6}}{2} (V_{GS3-6} - V_{THN})^2 (1 + \lambda_{3-6} \cdot V_{DS3-6}) \quad (125)$$

with λ_{3-6} (resp. V_{GS3-6} and V_{DS3-6}) is the channel-length modulation parameter (resp. the gate-source and the drain-source voltage) of M3, M4, M5, and M6 where:

$$V_{GS3-6} = V_{DS3-6} = \frac{VDD}{2} - V_{DS1-2} - V_{DS0} \quad (126)$$

with V_{DS0} (resp. V_{DS1-2}) is the drain-source voltage of the transistor M0 (resp. M1 and M2). Considering the used technology, λ is approximatively equal to 0.021 V^{-1} (resp. 0.072 V^{-1}) for a NMOS (resp. PMOS) transistor having a length of $1\mu\text{m}$ and biased using $V_{GS} \approx V_{DS} \approx VDD/2$ (resp. $-V_{GS} \approx -V_{DS} \approx VDD/2$). Finally, the current I_0 is also equally shared between M1, and M2 which allows using the Shockley model to write:

$$I_{1-2} = \frac{I_0}{2} = \beta_{1-2} \left(\frac{VDD}{2} - V_{DS0} - V_{THN} - \frac{V_{DS1-2}}{2} \right) V_{DS1-2}. \quad (127)$$

Considering the following assumptions:

$$VDD - V_{THN} \gg \frac{V_{DS0}}{2} \quad (128)$$

$$1 \gg \lambda_{A-B} \cdot |V_{DSA-B}| \quad (129)$$

$$1 \gg \lambda_{3-6} \cdot V_{DS3-6} \quad (130)$$

$$\frac{VDD}{2} - V_{DS0} - V_{THN} \gg \frac{V_{DS1-2}}{2}, \quad (131)$$

(122), (124), (125), and (127) can be simplified as follows:

$$I_0 = \beta_0 (VDD - V_{THN}) V_{DS0} \quad (132)$$

$$I_{A-B} = \frac{I_0}{2} = \frac{\beta_{A-B}}{2} \left(\frac{VDD}{2} - |V_{THP}| \right)^2 \quad (133)$$

$$I_{3-6} = \frac{I_0}{4} = \frac{\beta_{3-6}}{2} (V_{GS3-6} - V_{THN})^2 \quad (134)$$

$$I_{1-2} = \frac{I_0}{2} = \beta_{1-2} \left(\frac{VDD}{2} - V_{DS0} - V_{THN} \right) V_{DS1-2}. \quad (135)$$

As reminder, the gain of the analog multiplier is equal to:

$$K = \sqrt{\frac{\beta_{3-6} I_0}{2}} \cdot \frac{R_{OUT}}{VDD - 2 \cdot [V_{DS0} + V_{THN}]} \quad (62)$$

with R_{OUT} the multiplier output resistance whose the reciprocal is equal to:

$$\frac{1}{R_{OUT}} = g_{DSA-B} + \frac{2 \cdot g_{DS0} \cdot g_{DS1-2} \cdot g_{DS3-6}}{g_{DS0} (g_{DS1-2} + g_{DS3-6}) + 2 \cdot g_{DS1-2} \cdot g_{DS3-6}} + \frac{1}{R_L} \quad (136)$$

where g_{DS0} is the drain-source conductance of the transistor M0, g_{DSX-Y} is the drain-source conductance of the transistors from MX to MY, and R_L is the resistive load connected to the multiplier output. Since M0, M1, and M2 are biased in the linear region and M3, M4, M5, M6, MA, and MB are biased in the saturation region, g_{DS3-6} and g_{DSA-B} can be considered small compared to g_{DS0} and g_{DS1-2} , which allows to simplify (136) as follows:

$$\frac{1}{R_{OUT}} = g_{DSA-B} + 2 \cdot g_{DS3-6} + \frac{1}{R_L}. \quad (137)$$

Moreover, if the resistive load R_L is an open circuit as in this paper, (137) becomes:

$$\frac{1}{R_{OUT}} = g_{DSA-B} + 2 \cdot g_{DS3-6}. \quad (138)$$

From (124) and (125), g_{DS3-6} and g_{DSA-B} can be written as follows:

$$g_{DSA-B} = \frac{\delta I_{A-B}}{\delta V_{DSA-B}} = \frac{\beta_{A-B}}{2} \left(\frac{VDD}{2} - |V_{THP}| \right)^2 \lambda_{A-B} \quad (139)$$

$$g_{DS3-6} = \frac{\delta I_{3-6}}{\delta V_{DS3-6}} = \frac{\beta_{3-6}}{2} (V_{GS3-6} - V_{THN})^2 \lambda_{3-6}. \quad (140)$$

Assuming (129) and (130), (139) and (140) becomes:

$$g_{DSA-B} = \frac{I_0}{2} \lambda_{A-B} \quad (141)$$

$$g_{DS3-6} = \frac{I_0}{4} \lambda_{3-6} \quad (142)$$

which allows (138) to be written as follows:

$$\frac{1}{R_{OUT}} = \frac{I_0}{2} (\lambda_{A-B} + \lambda_{3-6}). \quad (143)$$

Using (143) and (62), the multiplier gain can be written as follows:

$$K = \sqrt{\frac{2\beta_{3-6}}{I_0}} \cdot \frac{1}{VDD - 2 \cdot [V_{DS0} + V_{THN}]} \cdot \frac{1}{\lambda_{A-B} + \lambda_{3-6}} \quad (144)$$

which leads using (134) to:

$$K = \frac{1}{V_{GS3-6} - V_{THN}} \cdot \frac{1}{VDD - 2 \cdot [V_{DS0} + V_{THN}]} \cdot \frac{1}{\lambda_{A-B} + \lambda_{3-6}}. \quad (145)$$

Finally, since higher V_{DS0} and V_{DS1-2} are, lower the gain K is, the minimum gain K_{MIN} of the multiplier can be expressed as follows:

$$K_{MIN} = \frac{1}{\frac{VDD}{2} - V_{THN}} \cdot \frac{1}{VDD - 2 \cdot V_{THN}} \cdot \frac{1}{\lambda_{A-B} + \lambda_{3-6}}. \quad (146)$$

Thus, if the multiplier is biased according to (1), it can be noted that the minimum gain of the multiplier depends only on the supply voltage, the threshold voltage of NMOS transistors, and the channel-length modulation parameter of NMOS and PMOS transistors when they are biased with $|V_{GS}|=|V_{DS}|=VDD/2$.

E. Design procedure of the multiplier

To size the MOS transistors of the proposed multiplier biased according to (1), a preliminary work consists to extract, in addition to the threshold voltage of NMOS transistors, the channel-length modulation parameter λ_X of NMOS and PMOS transistors when they are biased with $|V_{GS}|=|V_{DS}|=VDD/2$ for several lengths L_X . Indeed, this parameter highly depends on the MOS length and so the used MOS length will highly impact the multiplier gain.

The next step is to choose the targeted gain. However, it must be noted that for a fixed output dynamic range, the more the multiplier gain is, the less the input dynamic range is.

Indeed, in this context, the input voltage range for which a multiplier works truly as a multiplier is inversely proportional to its gain since high input voltages lead to multiplier saturation. For this work, since ECG front-ends can typically provide ± 100 mV single voltage, the targeted gain has been fixed to 5 in order to have:

$$VDI = K \cdot VDI \cdot VD2 \text{ when } VDI = VD2 = 2 \cdot 100 \text{ mV}. \quad (147)$$

Thus, the multiplier gain is voluntary low in order to have a sufficient input voltage range but avoids equally the saturation of the proposed energy detectors based on this multiplier. For the used technology and a length of $1 \mu\text{m}$, λ is approximatively equal to 0.021 V^{-1} (resp. 0.072 V^{-1}) for a NMOS (resp. PMOS) transistor if $V_{GS} \approx V_{DS} \approx VDD/2$ (resp. $-V_{GS} \approx -V_{DS} \approx VDD/2$). Since the NMOS threshold voltage is about 0.52 V , the minimum gain K_{MIN} can be estimated using (146) to 4.21. To simplify the design procedure, a length of $1 \mu\text{m}$ has been equally set for M0, M1, and M2.

To size the width of the MOS transistors, a way consists to solve the mathematical optimization problem based on the following equations introduced in the subsection D of the appendix:

$$I_0 = \beta_0 (VDD - V_{THN}) V_{DS0} \quad (132)$$

$$\frac{I_0}{2} = \frac{\beta_{A-B}}{2} \left(\frac{VDD}{2} - |V_{THP}| \right)^2 \quad (133)$$

$$\frac{I_0}{4} = \frac{\beta_{3-6}}{2} \left(\frac{VDD}{2} - V_{DS1} - V_{DS0} - V_{THN} \right)^2 \quad (134)$$

$$\frac{I_0}{2} = \beta_{1-2} \left(\frac{VDD}{2} - V_{DS0} - V_{THN} \right) V_{DS1-2}. \quad (135)$$

The goal is also to find the values of W_0 , W_{1-2} , W_{3-6} and W_{A-B} which verify:

$$\frac{\frac{I_0}{\beta_0 (VDD - V_{THN})}}{V_{DS0} \text{ from (133)}} + \frac{I_0}{2\beta_{1-2} \left(VDD - \frac{I_0}{\beta_0 (VDD - V_{THN})} - V_{THN} \right)} = \frac{VDD}{2} - V_{THN} - \sqrt{\frac{I_0}{2\beta_{3-6}}} \quad (148)$$

V_{DS1} from (136) and (133)
 $V_{DS0} + V_{DS1}$ from (135)

and which allow to minimize I_0 (to minimize the power consumption) in addition to V_{DS0} and V_{DS1} while keeping I_0 , V_{DS0} , and V_{DS1-2} strictly positive. Obviously, the values of W_0 , W_{1-2} , W_{3-6} , W_{A-B} must be compatible with the used technology.

To quickly find a solution without complex programming, it is proposed here to arbitrary set a low value for V_{DS0} and V_{DS1} and to determine the associated width ratios W_{A-B}/W_{3-6} , W_0/W_{3-6} , and W_{1-2}/W_{3-6} . It is also possible to determine which width is the smallest width and a first simulation can be done by setting the smallest width equals to a large width with an appropriate number of fingers (for example $25 \mu\text{m}$). Then, the other widths must be set using the ratios computed previously. Next, the widths ratios can be tuned around their initial values to reach the targeted performances. All the widths can also be

decreased by multiplying each one by the same factor lower than 1 until the smallest width is equal to the minimum width allowed by the used technology. This will decrease the power consumption but will modify other parameters such as the output slew rate or the multiplication precision. It is also necessary to stop the procedure when the targeted gain or other parameters decrease under the targeted performances. The same procedure can be repeated using different values of V_{DS0} and V_{DS1-2} and the final design must be selected from the different obtained ones according to the targeted specifications.

To illustrate the procedure, the following assumptions on V_{DS0} , and V_{DS1-2} are done:

$$V_{DS0} + V_{DS1-2} = \gamma \cdot VDD \quad (149)$$

$$V_{DS0} = \eta \cdot VDD \quad (150)$$

Using (133) and (134), it is possible to determine the W_{A-B}/W_{3-6} ratio as follows:

$$\frac{W_{A-B}}{W_{3-6}} = \frac{\alpha_N \left(\frac{1}{2} - \gamma - \frac{V_{THN}}{VDD} \right)^2}{\alpha_P \left(\frac{1}{2} - \frac{|V_{THP}|}{VDD} \right)^2} \quad (151)$$

It can be noted that this ratio only depends on the sum of V_{DS0} and V_{DS1-2} . Next, using (132) and (134), it is possible to determine the W_0/W_{3-6} ratio as follows:

$$\frac{W_0}{W_{3-6}} = \frac{\left(1 - 2\gamma - \frac{2V_{THN}}{VDD} \right)^2}{2\eta \left(1 - \frac{V_{THN}}{VDD} \right)} \quad (152)$$

Finally, using (134) and (135), it is possible to determine the W_{1+2}/W_{3-6} ratio as follows:

$$\frac{W_{1-2}}{W_{3-6}} = \frac{\left(1 - 2\gamma - \frac{2V_{THN}}{VDD} \right)^2}{2(\gamma - \eta) \left(1 - 2\eta - \frac{2V_{THN}}{VDD} \right)} \quad (153)$$

Considering the following values for the used technology:

$$\begin{aligned} VDD &= 3.3 \\ V_{THN} &= 0.52 \\ V_{THP} &= 0.77 \\ \alpha_N &= 70e-6 \\ \alpha_P &= 28e-6 \end{aligned} \quad (154)$$

and the following parameters for V_{DSX} voltages:

$$\begin{aligned} \gamma &= 1/10 \\ \eta &= \gamma/3 \end{aligned} \quad (155)$$

the obtained width ratios are:

$$\begin{aligned} \frac{W_{A-B}}{W_{3-6}} &= 4.13 \approx 4 \\ \frac{W_0}{W_{3-6}} &= 4.19 \approx 4 \\ \frac{W_{1-2}}{W_{3-6}} &= 2.85 \end{aligned} \quad (156)$$

Thus, it can be deduced that the smallest width is W_{3-6} and a starting set of width values is:

$$\begin{aligned} W_{3-6} &= W \\ W_{A-B} &= 4 \cdot W \\ W_0 &= 4 \cdot W \\ W_{1-2} &= 2.85 \cdot W \end{aligned} \quad (157)$$

where the initial value of W must be set to a large value as indicated previously (here $25 \mu\text{m}$ with 10 fingers). Next, for the proposed design, the width ratio W_{1-2}/W_{3-6} have been tuned to 2 to adjust V_{DS0} , V_{DS1-2} and also the gain of the proposed multiplier. Finally, W , and also every MOS width, has been proportionally decreased according to the selected width ratios until getting the minimum bias current I_0 which allows to obtain a multiplier with the targeted performances (gain, precision, slew rate, etc.). For this multiplier, the procedure has been stopped to $W = 2.5 \mu\text{m}$ which allows to minimize the derivative of K with respect to W . However, it can be noted that it exists a value of W from which the gain begins to highly decrease. This particular value of W can be selected if the power consumption must be optimized for a particular gain.

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