A novel BIST for monitoring aging/temperature by self-triggered scheme to improve the reliability of STT-MRAM

Y. Zhou, H. Cai, M. Zhang, L.A.B. Naviner, J. Yang

Version of Record: https://www.sciencedirect.com/science/article/pii/S0026271420304388
Manuscript_5e862b78379067032a5f969a09298ae2

A Novel BIST for Monitoring Aging / Temperature by Self-Triggered Scheme to Improve the Reliability of STT-MRAM

Y. Zhou [a], H. Cai [a,b,*], M. Zhang [a], L.A.B. Naviner [b], J. Yang [a]

[a] *National ASIC System Engineering Center, Southeast University, Nanjing, 210096*
[b] *Télécom Paris, 19 place Marguerite Perey Palaiseau, France, 91120*

Abstract –This paper proposes a novel methodology to design high reliable STT-MRAM, with self-activated built-in-self-test (BIST) against aging/temperature-induced degradation. During sensing operation, Tunnelling magnetoresistance (TMR) is monitored, and real-time BIST is activated prior to permanent damage in Magnetic tunnel junction (MTJ) stack. To evaluate the feasibility of the test scheme, the proposed technique was involved in MRAM array implementation using 28-nm CMOS and 40-nm MTJ. HSPICE MOS Reliability Analysis (MOSRA) is used to evaluate the amount of electrical stress to the actual device aging degradation. Compared with previous periodical BIST method, the proposed self-triggered BIST saves ~31.1% cumulative power consumption over 12 years. And the proposed technique can improve reliability in the wear-out failure period.

1. Introduction

Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM) is a prospective candidate in terms of access efficiency, scalability, data retention and endurance [1, 2]. Non-volatile data stored in magnetic tunnel junction (MTJ) is represented as bi-stable magnetization states with asymmetry switching property [3]. The 1T-1MTJ bit-cell design is the most widely-adopted bit-cell structure [2-6], comprising an MTJ device serially connected with an access NMOS transistor (see Fig. 1). Two ferromagnetic layers constitute MTJ, the pin layer (PL) and the free layer (FL), which are isolated by a thin oxide layer. The direction of the FL magnetization determines the MTJ state, as parallel (P) or anti-parallel (AP) to the PL magnetization. The middle layer as tunnel barrier serves as an insulating non-magnetic spacer between the FL and PL. During "P" state writing operation, WL and BL are pulled up to supply voltage and SL is grounded, thus leading to a current flowing from BL to SL. In contrast, an AP state writing operation requires the opposite current through the MTJ device.

STT-MRAMs in MCU [7], last level cache [8], Internet of things [9] and space applications [10] show strict requirements for reliability. Unfortunately, MRAM bit-cell is vulnerable to aging mechanisms and temperature fluctuations due to iterative access with high currents [11-13]. The perpendicular magnetic anisotropy (PMA) of the MTJ device is obtained from the hybridization of atoms near the pin, fixed and barrier layers. However, the defects and corresponding fault models of STT-MRAM are not as extensively explored as in SRAM [14, 15], there is a growing need for defect and fault analysis [16]. Built-in-self-test (BIST) technique provides the capability for high fault coverage testing, simultaneously relaxes the reliance on external testing equipment [17], BIST generally combines with built-in self-repair (BISR) to improve chip yield.

Several BIST studies were proposed to aim at defects after manufacturing [12, 16]. Subtle failures often grow over time, and a substantial fraction of their population can escape the initial test and screening process, e.g., aging and temperature-drift defects. These defects formation over time need to be temperature-drift test, but it will bring unnecessary power consumption and performance loss. Due to process variation, manufacturing defects and different using frequencies, the MRAM bit-cells on a same chip may not have uniform aging degree and same response to temperature drift. It is necessary

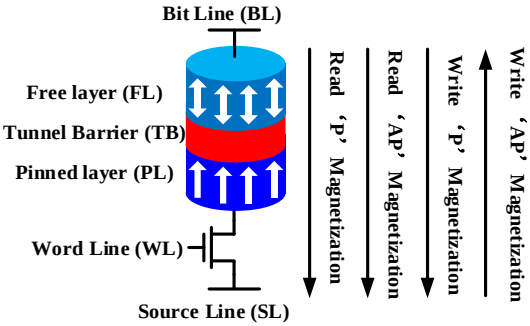

Fig. 1. Write and read operations of 1T-1MTJ cell.

to propose a monitoring mechanism to find the random faults during the chip working, and activate the BIST circuit to analyse and repair the faults. The main highlights of this work are summarized as follows:

- A real-time BIST triggered scheme with aging and temperature-drift monitoring, and cross sensing amplifier (SA) are used to detect error bit-cell and overcome tunnelling magnetoresistance (TMR) degradation.
- Aging and temperature drift induced degradation/failure are estimated. Aging behavior of 1T-1M MRAM bit-cell is simulated based on experimental results. The detection of TMR degradation utilizes SA is analysised by 10^5 Monte Carlo simulations to evaluate flag trigger function.

2. Preliminaries

Random/permanent failure of MRAM caused by aging and temperature effect imposes a large burden in testing circuit [12, 13, 18]. When a large driving current flows into bit-cell, the temperature of the corresponding NMOS transistor and MTJ tend to raise up, and the Joule heating due to the flowing current will impact the device performance.

MRAM sensing margin can be significantly limited by aging and temperature fluctuations. Fig. 2 illustrates the distribution of R_P and R_{AP} under different conditions. As the resistance difference between the two states is about twice of R_P, the non-overlapping region is quite narrow. When the temperature increases, R_P almost keeps the same, while the degraded R_{AP} leads to resistance distributions even closer [2, 19, 20]. Furthermore, resistance distributions of R_P and R_{AP} can

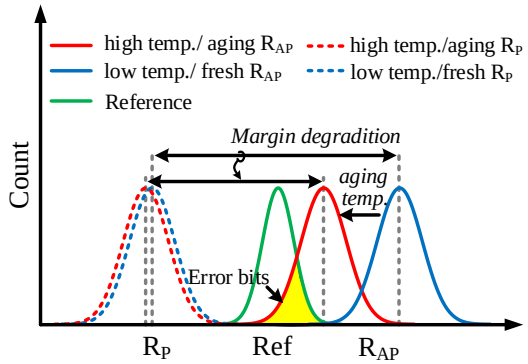

Fig. 2. Resistance distributions change with aging and temperature variations, narrowing sensing margin.

be shifted due to process variation, resulting in the occurrence of error bits, demonstrated as the overlap between the distribution of R_{AP} and reference. The limited sensing margin caused by aging is similar with that caused by temperature variations, challenging STT-MRAM reliability.

2.1. Aging effects on STT-MRAM

During reading and writing operations, STT-MRAM bit-cells experience aging caused by the applied high current [21, 22, 23], leading to a decrease of reliability. Bit-cells with large conductance generate large currents during writing operation, which change their internal and ambient temperature and thus incur thermal issues. These thermal issues not only aggravate aging of these STT-MRAM bit-cells further but also result in an accuracy discrepancy between bit-cell source and reference source. Bit-cell aging defect formation can impact both the access transistor and the MTJ device.

Aging effects in CMOS have been extensively reported, such as wear-out failures due to oxide wear-out, hot-electrons or bias temperature instability. The access transistors are susceptible to aging because of high write voltage and repeated operations. The common mechanism observed in transistors is the gate-oxide breakdown, which causes a short connection at the gate-source or gate-drain interfaces. This leads to decreased impedance between the bit-line and ground, which affects all the bit-cells sharing the bit-line.

The main aging mechanisms of MTJ are the TMR degradation and soft/hard breakdown phenomenon. At each write/read operation the tunnel barrier is exposed to an electrical stress which might cause a TMR decreasing gradually until breakdown, which is one of the most prominent failure mechanisms in MTJ devices [24, 25]. The behavior of the MTJ after breakdown is with ultra-low resistance and fixed state, leading to permanent functional failure. Scaling with constant write energy demands to decrease in the MgO barrier thickness and this would lead to reliability issues due to thin dielectric material. Two types of dielectric breakdown mechanisms occur in the MTJ stacks [26]: hard and soft breakdown. Hard breakdown in the dielectric material is induced by the high electric field across the dielectric. The lifetime of ideal dielectric barrier undergoing hard breakdown can be predicted based on the time-dependent dielectric breakdown equation [21, 23, 27]:

$$TF \propto e^{\frac{\Delta H_0}{k_B T} - \Gamma \cdot E_{OX}} \tag{1}$$

where TF is the time-to-failure, ΔH_0 is the activation energy, E_{OX} is the electric field across the oxide barrier, and Γ is the field acceleration parameter. k_B is the Boltzmann constant and T is temperature.

Soft breakdown occurs due to the formation of pin-holes during the dielectric deposition process. These pinholes can form conductive paths across the dielectric layer, which act as resistors in parallel to the MTJ. The defects affect the PMA interfacial region and degrade the MTJ stack resistance and TMR. The pinhole growth mechanism is explained in detail in [28, 29]. It occurs in 3 phases to result in the eventual barrier breakdown in MTJ. Firstly, there is no degradation at the junction with applied bias voltage/current. Secondly, the pin-hole area keeps increasing, the MTJ junction area decreasing with the increase in the applied current, and TMR is decreased. Finally, the pin-hole occupies most of the junction area, making the MTJ device behave like a resistor. The pin-holes grow in size due to the Joule heating of the conductive path formed across dielectric over time. During the early stages, MTJ device parameter deviations can be observed as TMR degradation, R_P variation, TMR bias dependant slope at AP state, switching voltage, and switching time. Symptoms of pin-hole formed in the MTJ are exhibited in the electrical characteristics [29], where the degraded Resistance-Area (RA) and TMR due to pin-hole formed can be described by [29, 30]

$$RA_{eff} = \frac{A_0}{\frac{A_0(1-A_{ph})}{RA_{df}} + \frac{A_0 \cdot A_{ph}}{RA_{bd}}} \tag{2}$$

$$TMR_{eff} = \frac{TMR_{df}\,(\mathrm{RA}_{eff} - \mathrm{RA}_{bd})}{RA_{df} - A_{bd}} \tag{3}$$

Here A_{ph} is the normalized pinhole area with respect to the cross-sectional area A of the MTJ device; RA_{eff} and TMR_{eff} are the effective RA and TMR parameters of the MTJ stack, respectively. RA_{bd} is the resultant RA after breakdown of the MTJ device. A_{ph} correspond to the area of the pinhole formed. TMR_{df} and A_0 correspond to the initial TMR and area of the junction.

2.2. Thermal effects on STT-MRAM

Joule heating caused by the current passing through the STT-MRAM bit-cell leads to temperature fluctuations, thereby affecting the drivability of the NMOS transistor and the characteristics of the MTJ, including its resistance value, magnetic stability, the required switching current and the switching time. The temperature dependence of NMOS access transistor drivability can be expressed as [31]:

$$I = \beta \times \frac{(V_{gs} - V_{th})V_{ds} - \frac{a}{2}V_{ds}^2}{1 + \frac{1}{v_{sat}L}V_{ds}} \tag{4}$$

$$\beta = \mu_0(T_r)\left(\frac{T}{T_r}\right)^{-k_\mu} \times \frac{C_{ox}}{1 + U_0\left(V_{gs} - V_{th}\right)}\frac{W}{L} \tag{5}$$

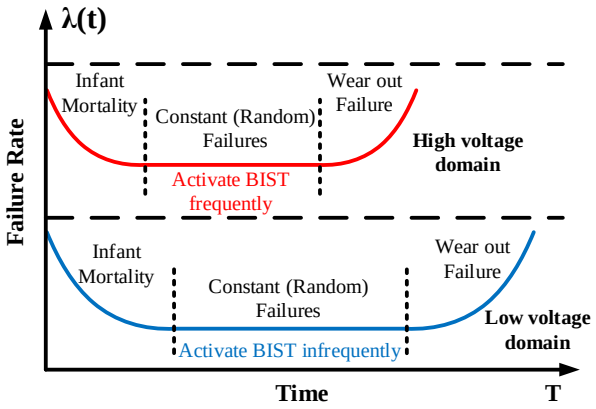

Fig. 3. The classical bathtub curve, λ(t) indicates failures rate, T indicates STT-MRAM working time.

U_0 is the vertical filed mobility reduction coefficient, C_{ox} is the gate oxide capacitance per unit area, a is the body-effect coefficient, v_{sat} is carrier velocity saturation, T_r is room temperature and $\mu_0(T_r)(T/T_r)^{-k\mu}$ is the electron mobility at absolute temperature. Since mobility is reduced with increased temperature, the drivability of the MOS transistor is degraded at high temperature. That is, the generated current becomes small under the same biasing condition.

Secondly, the temperature dependence of MTJ resistance shows a linear rule, when increasing the temperature from the low temperature to high temperature, the junction resistance at antiparallel state of an MTJ with MgO barrier decreases [32]. This phenomenon can be evaluated with the model provided by [20]. The conductance of the junction can be calculated by:

$$G(\theta) = G_T\left\{1+\cos(\theta)P_1P_2\right\} + G_{SI} \qquad (6)$$

Where $\theta = 0°$ or $180°$ for parallel or antiparallel state, respectively. G_T is the prefactor for direct elastic tunneling and can be given by $G_T=G_0CT/\sin(CT)$. Here G_0 is a constant and $C=1.387\times10^{-4}d/(\sqrt{\phi})$, with barrier width ($d$) in A, and barrier height (ϕ) in eV. P_1 and P_2 are the effective tunneling electron spin polarizations of P_1 the P_2 two ferromagnetic layers. The temperature dependence of and can be expressed as $P(T)=P_0(1-\beta T^{\alpha})$, where β is a constant and $1<\alpha<2$. G_{SI} is a smaller second conductance due to assisted, spin-independent tunneling which is proportional to $T^{1.35\pm0.15}$. In contrast, the MTJ resistance at the parallel state (R_P) has a much weaker temperature dependence, because the majority spin channel tunneling dominates the overall conductance.

In general, the temperature and aging can shift the MTJ resistance distribution. As shown in Fig. 2, when the temperature increases or aging occurs, R_P almost keeps the same, while R_{AP} degrades, making the resistance distributions even closer [2, 20-23, 32].

3. Proposed self-activated BIST by monitoring Scheme

The failure rate of storage follows the bathtub curve as shown in Fig. 3 [33]. The curve can be divided into infant mortality, constant failure, and wear-out failure period. Specifically, According to the discussion of thermal effects on STT-MRAM, the higher the working voltage is, the more Joule heating the circuit accumulates under the same memory access times, and the greater the probability of failure. Conventional

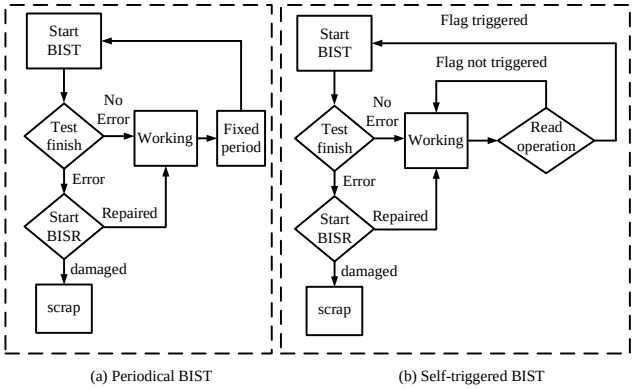

Fig. 4. Comparison on detecting aging/temperature drift between conventional BIST and the proposed self-activated BIST (a) Flow chart for conventional aging test by BIST. (b) Flow chart for proposed Self-activated BIST by Monitoring Scheme.

BIST studies can detect the defects that occur in the earlier infant mortality. Since then, aging failure shows randomness and unpredictability.

Due to the unpredictability of aging failure, conventional tests for aging detection were periodically performed. In low voltage applications, BIST is activated less frequently than in high voltage implementation. Activating BIST too frequently causes a large number of unnecessary chip accesses, which results in large energy consumption. Fig.4 (a) shows the flowchart for conventional aging test, it starts with testing all the bit-cells in the array. Then, the test results are checked whether there is error bits in the array. If yes, BISR is started to repair the error bits; if not, the chip keeps on working until the BIST is activated again after a period of operation time. In order to promptly detect faults and avoid unnecessary test, we propose self-activated BIST flow as shown in Fig.4 (b). During the read operation, TMR is detected. Once TMR is decreased, BIST unit is activated in real time. Fig.5 illustrates the block diagram of proposed design, the BIST is enabled by external signal and error bit flag. The redundant columns are used for fault replacement by BISR.

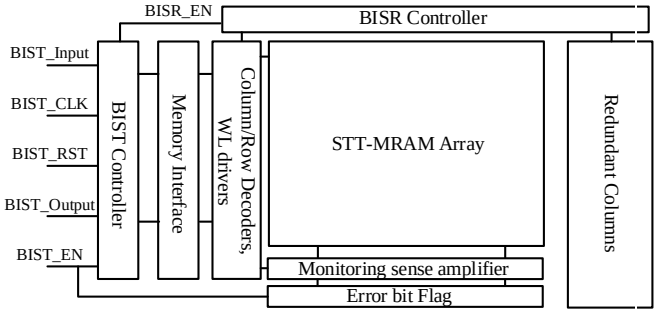

Fig. 5. Design Overview of proposed Self-activated BIST by Aging/Temperature Monitoring Scheme.

When the MTJ is at P/AP state, the voltage difference is generated on bit-line. Then the data stored in the memory cell can be detected by comparing the bit-line voltage to a reference voltage, which is usually preset to $V_{REF} = 0.5(V_P+V_{AP})$ using SA. The voltage difference of SA (denoted as sense margin) is normally used to evaluate read performance. Sense margin can be expressed as $SM=\min(V_{AP}-V_{REF}, V_{REF}-V_P)$. The temperature fluctuation induced variations of the MTJ resistance and NMOS transistor driving current can make the generated V_P or V_{AP} deviated from the designed values and hence affect the sense margin.

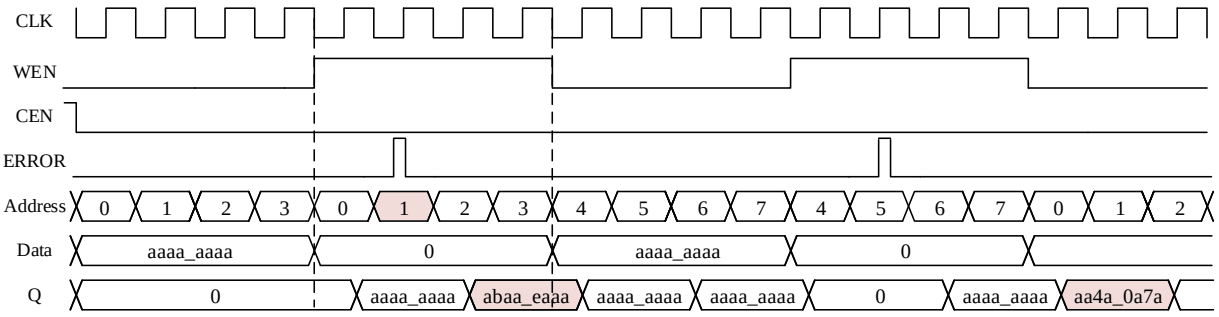

Fig. 7. Simulation waveform showing error bit detection.

In order to detect the TMR degradation, a monitoring sense amplifier (MSA) is proposed as shown in Fig.6 (a). Our previous work reported that weak MRAM bit-cells can be detected using cross sensing SA [34]. A switch-controlled multiplexer (SW1/SW2) at the input of the typical voltage SA to flip input offset, and successive sensing enable signal (SAE) are implemented. If the results (output1/output2) of adjacent sensing operations are different, it indicates that both sensing results are correct and the flag is activated by XOR. Fig.6 (c) shows the degradation of input voltage difference with TMR decreasing. It should be noticed that if the flag is not activated in the reading cycle, the error bit is located and BIST starts. In order to distinguish whether the fault is caused by temperature drift or aging, the traditional March algorithm is improved.

4. Simulation Results

Table I - Parameters of the used STT-MTJ compact model

Parameters	Description	Default Value
ΔH_0	Activation energy	0.8eV
Γ	Field acceleration parameter	1.7 cm/MV
β	Shape parameter	1.5
k_B	Boltzmann constant	$8.625 \cdot 10^{-5}$ eV/K
T_0	Ambient temperature	300 K
t_{OX}	Thickness of oxide barrier	0.85nm
TMR	Tunnel magnetoresistance ratio	150%
Area	MTJ surface	40nm·40nm·π/4
t_{sl}	Thickness of free layer	1.3nm
V_{sl}	Volume of free barrier	Area·t_{sl}

The proposed scheme is realized in a 256×32 STT-MRAM array and simulated with a 28 nm CMOS process. Table I lists the parameters of the MTJ compact model [21]. To simulate the aged performance of bit-cells, the aging TMR is set to 75%. The simulation waveform is shown in Fig. 7. Access controllers firstly write data into the addresses from '80b0000' to '80b0011', then read the data from these addresses. When the system accesses the date in the '80b0001', the error signal is triggered and BIST starts. The change trends of MSA detecting bit-error rate (BER) relying on different temperature and TMR are shown in Fig. 8, with the temperature increasing and the TMR decreasing, the detecting BER is improved.

The detection of TMR degradation utilizing MSA is analysised by Monte Carlo transient simulations to evaluate Flag trigger function as shown in Fig. 9. Notice that TMR is set to 150%. The response time of Flag is varied due to different BL swing. The probability of Flag triggered at the third period is 12.2%. The late triggered tail bits indicates the low-TMR bit-cells, which are sensitive to aging effects.

The TSMC 28nm standard cell was applied to perform

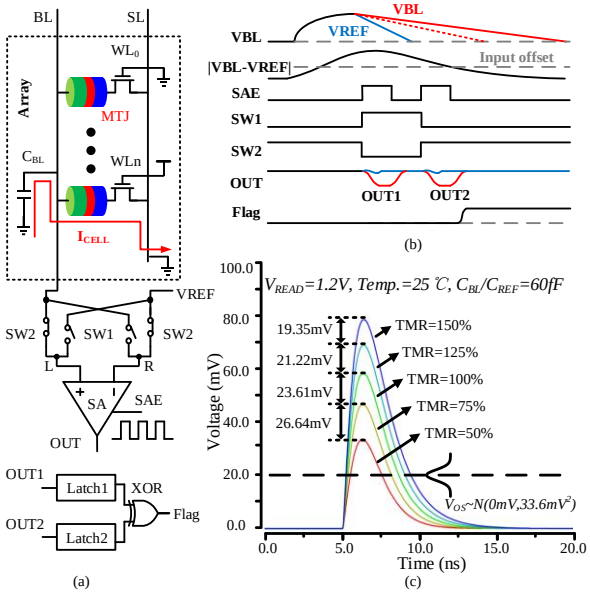

Fig. 6. (a) Proposed MSA Structure, a multiplexer consisting of SW1 and SW2 is used to flip the inputs. (b) Simulated transient behavior where SA outputs the correct data at the third sensing cycle, at the same time, the reading operation is completed. Control signal SW1 is reverse to SW2. (c) Under the influence of aging and temperature drift, the degradation of input voltage difference with TMR decreasing

reliability and performance analysis using the built-in aging MTJ/CMOS models integrated into Synopsys HSPICE [35]. MOSFET Model Reliability Analysis (MOSRA) was used to predict the longterm reliability and performance of the device [36]. BTI induced MRAM performance degradation are simulated based on the conventional periodical BIST and the proposed self-activated BIST. The comparisions of energy consumption are demonstrated in Fig. 10. Here, we setup the periodical BIST method using the March-C algorithm. Each test needs about 1×10^6 pJ energy consumption, and 10 periodic tests are performed each year. The cumulative energy consumption of periodical BIST increases linearly over time. For the proposed self-activated BIST, there is no error bit occurrance and BIST is not avtivated in the infant mortality period. During the constant failure period, the bit error rate and cumulative power consumption increase gradually. Finally, when entering into the wear-out failure period, BER is siginicantly increased, and the traditional periodical BIST cannot guarantee the reliability of the STT-MRAM. Compared with the conventional periodical BIST method, the proposed self-triggered BIST saves ~31.1% cumulative power consumption over 12 years.

Table II compares the proposed method with other counter aging/thermal reliability works. Time based reliability

Table II – Comparison with other counter aging/thermal works

	[5]	[6]	[29]	[30]	[31]	[32]	[33]	This work
Feature	BIST detect	Failure resilience	BIST detect	BIST detect	off-chip test	BIST detect	Distribute aging/ thermal stress	Embedded in read operation
Application	STT-MRAM	MeRAM/ MRAM	Logic	Logic	SRAM	Logic	RRAM	STT-MRAM
Objectives	Aging	Aging	Aging	Aging	Aging	Aging	Aging/ Thermal	Aging/ Thermal
Method	Periodic identify	Pre-design	Periodic identify	Periodic identify	Periodic identify	Periodic identify	Software training	Real-time monitor

degradation of solid state devices leads to inevitable degradation mechanism, which effects logic circuit [37, 38, 40], volatile memory [39] and nonvolatile memory [12, 13, 41], reduces carrier mobility and translates into performance degradation. Periodically testing chip can prevent the challenge of aging to chip reliability. However, due to the randomness of aging, it is impossible to define the test cycle reasonably, which limits design space exploration between test cost and reliability issues. The proposed scheme not only ensures the reliability, but also saves the cost.

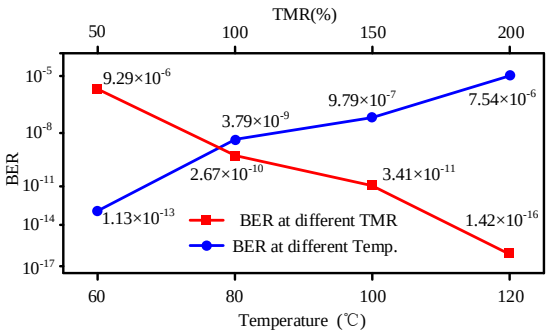

Fig. 8. Simulated bit error rate for 1 Mb STT-MRAM across TMR/Temperature variation.

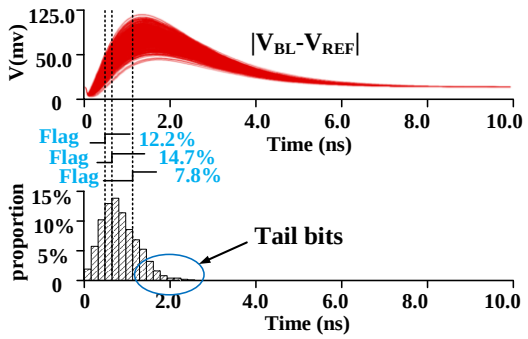

Fig. 9. The 10^4 times Monte Carlo simulation results of Flag-trigger of the AP state read in the SS corner, 25℃.

The typical STT-MRAM bit-cell size is 6.3×10^{-2} μm^2. In our design a 4-1 column MUX is used so that one monitoring sense amplifier is shared by 4 columns. Compared with the conventional scheme with voltage-mode sense amplifier, when the number of bit-cells per BL is 512, and 512 columns in the array, the layout area overhead of the proposed technique is 2.9%.

5. Conclusion

The scheme to periodically enable BIST to alleviate aging and temperature drift leads to power dissipations and chip damage. In this work, we demonstrate the self-activated BIST methodology along with the error bit detection technique to provide a reliability enhancement design in STT-MRAM. The technique can be used for alerting the system regarding the fault formation, allowing time for repairing operation before permanent damage of the MTJ stack. A real-time monitoring method is used to involve a detection phase in the sensing operation, which not only ensures the reliability but also saves the cost.

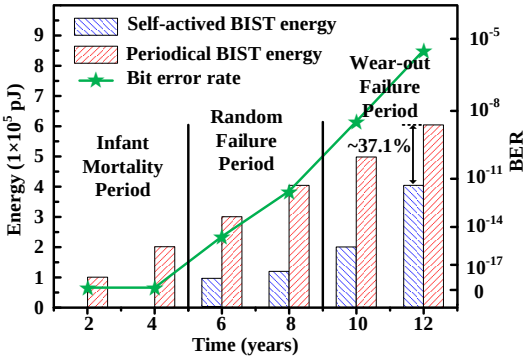

Fig. 10. Comparison of cumulative energy consumption between self-activated BIST and periodical BIST over 12 years based on HSPICE MOSRA simulation model.

Acknowledgment

This work is supported in part by National Key R&D Program of China under Grant 2018YFB2202800 and National Natural Science Foundation of China under Grant 61904028.

References

[1] C. Chapper et al., The emergence of spin electronics in data storage, Nature Mater., vol. 6, no. 11, pp. 813–823, Nov. 2007. https://doi.org/10.1038/nmat2024

[2] Q. Dong et al., A 1-Mb 28-nm 1T1MTJ STT-MRAM With Single-Cap Offset-Cancelled Sense Amplifier and In Situ Self-Write-Termination, in IEEE J. Solid-State Circuits, vol. 54, no. 1, pp. 231-239, Jan. 2019. https://doi.org/10.1109/JSSC.2018.2872584

[3] D. Shum et al., CMOS-embedded STT-MRAM arrays in 2x nm nodes for GP-MCU applications, 2017 Sym. VLSI Tech., 2017, pp. T208-T209. https://doi.org/10.23919/VLSIT.2017.7998174

[4] C. J. Lin et al., 45nm low power CMOS logic compatible embedded STT MRAM utilizing a reverse-connection 1T/1MTJ cell, 2009 IEEE Int. Electron Devices Meeting (IEDM), Baltimore, MD, 2009, pp. 1-4. https://doi.org/10.1109/IEDM.2009.5424368

[5] Y. M. Lee et al., Highly scalable STT-MRAM with MTJs of top-pinned structure in 1T/1MTJ cell, Symp. on VLSI Tech., 2010, pp.

49-50. https://doi.org/10.1109/VLSIT.2010.5556123
[6] R. Dorrance et al., Scalability and Design-Space Analysis of a 1T-1MTJ Memory Cell for STT-RAMs, in IEEE Transactions on Electron Devices, vol. 59, no. 4, pp. 878-887, April 2012. https://doi.org/10.1109/TED.2011.2182053
[7] Y. K. Lee et al., Embedded STT-MRAM in 28-nm FDSOI Logic Process for Industrial MCU/IoT Application, 2018 IEEE Symposium on VLSI Technology, Honolulu, HI, 2018, pp. 181-182. https://doi.org/10.1109/VLSIT.2018.8510623
[8] G. Hu et al., "Spin-transfer torque MRAM with reliable 2 ns writing for last level cache applications," 2019 IEEE Int. Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019, pp. 2.6.1-2.6.4. https://doi.org/10.1109/IEDM19573.2019.8993604
[9] T. Yang et al., A 28nm 32Kb embedded 2T2MTJ STT-MRAM macro with 1.3ns read-access time for fast and reliable read applications, 2018 IEEE International Solid - State Circuits Conference - (ISSCC), San Francisco, CA, 2018, pp. 482-484. https://doi.org/10.1109/ISSCC.2018.8310394
[10] O. Gonçalves et al., Radiation Hardened MRAM-Based FPGA, in IEEE Transactions on Magnetics, vol. 49, no. 7, pp. 4355-4358, July 2013. https://doi.org/10.1109/TMAG.2013.2247744
[11] D. Halupka et al., Negative-resistance read and write schemes for STT-MRAM in 0.13 µm CMOS, in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2010, pp. 256–257. https://doi.org/10.1109/ISSCC.2010.5433943
[12] G. Radhakrishnan et al., Monitoring Aging Defects in STT-MRAMs, in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (Early Access). https://doi.org/10.1109/TCAD.2020.2982145
[13] H. Cai et al., Addressing Failure and Aging Degradation in MRAM/MeRAM-on-FDSOI Integration, in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 1, pp. 239-250, Jan. 2019. https://doi.org/10.1109/TCSI.2018.2854277
[14] W. K. Chien et al., The Competing Aging Effects on SRAM Operating Life Tests, in IEEE Transactions on Device and Materials Reliability, vol. 19, no. 2, pp. 416-425, June 2019. https://doi.org/10.1109/TDMR.2019.2916481
[15] F. Ahmed et al., Reliable cache design with on-chip monitoring of NBTI degradation in SRAM cells using BIST, 2010 28th VLSI Test Symposium (VTS), Santa Cruz, CA, 2010, pp. 63-68. https://doi.org/10.1109/VTS.2010.5469614
[16] I. Yoon, A. Chintaluri and A. Raychowdhury, "EMACS: Efficient MBIST architecture for test and characterization of STT-MRAM arrays," 2016 IEEE ITC, Fort Worth, TX, 2016, pp. 1-10. https://doi.org/10.1109/TEST.2016.7805834
[17] I. Voyiatzis et al., Input Vector Monitoring Concurrent BIST Architecture Using SRAM Cells, in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 7, pp. 1625-1629, July 2014. https://doi.org/10.1109/TVLSI.2013.2278439
[18] G. Hu et al., Key parameters affecting STT-MRAM switching efficiency and improved device performance of 400°C-compatible p-MTJs, 2017 IEEE Int. Ele. Devices Meeting (IEDM), pp. 38.3.1-38.3.4. https://doi.org/10.1109/IEDM.2017.8268515
[19] X. Liu et al., Thermal stability of magnetic tunneling junctions with MgO barriers for high temperature spintronics, Appl. Phys. Lett., vol. 89, no. 2, p. 023504, 2006.
[20] X. Bi et al., STT-RAM Cell Design Considering CMOS and MTJ Temperature Dependence, in IEEE Transactions on Magnetics, vol. 48, no. 11, pp. 3821-3824, Nov. 2012,. https://doi.org/10.1109/TMAG.2012.2200469
[21] Y. Wang et al., Compact Model of Dielectric Breakdown in Spin-Transfer Torque Magnetic Tunnel Junction, in IEEE Transactions on Electron Devices, vol. 63, no. 4, pp. 1762-1767, April 2016. https://doi.org/10.1109/TED.2016.2533438
[22] R. H. Koch et al., Time-resolved reversal of spintransfer switching in a nanomagnet, Phys. Rev. Lett., vol. 92, p. 088302, Feb. 2004. https://doi.org/10.1103/PhysRevLett.92.088302
[23] J. W. McPherson et al., Time dependent dielectric breakdown physics—Models revisited, Microelectron. Rel., vol. 52, nos. 9–10, pp. 1753–1760, Sep./Oct. 2012. https://doi.org/10.1016/j.microrel.2012.06.007
[24] K. C. Chun et al., A Scaling Roadmap and Performance Evaluation of In-Plane and Perpendicular MTJ Based STT-MRAMs for High-Density Cache Memory, in IEEE Journal of Solid-State Circuits, vol. 48, no. 2, pp. 598-610, Feb. 2013. https://doi.org/10.1109/JSSC.2012.2224256
[25] Noguchi, H. et al., A 3.3 ns-access-time 71.2 µW/MHz 1 Mb embedded STT-MRAM using physically eliminated read-disturb scheme and normally-off memory architecture, IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, February 2015. https://doi.org/10.1109/ISSCC.2015.7062963
[26] B. Oliver et al., Two breakdown mechanisms in ultrathin alumina barrier magnetic tunnel junctions, Journal of applied physics 95, 1315 (2004). https://doi.org/10.1063/1.1636255
[27] K. Hosotani et al., Effect of self-heating on time-dependent dielectric breakdown in ultrathin MgO magnetic tunnel junctions for spin torque transfer switching magnetic random access memory, Jpn. J. Appl. Phys., vol. 49, no. 4S, pp. 04DD15-1–04DD15-6, 2010. https://doi.org/10.1143/JJAP.49.04DD15
[28] L. Hua et al., Barrier breakdown mechanism in nano-scale perpendicular magnetic tunnel junctions with ultrathin MgO barrier, AIP Advances, Vol. 8, Issue. 5, 2018. https://doi.org/10.1063/1.5007656
[29] H. Cai et al., Breakdown Analysis of Magnetic Flip-Flop With 28-nm UTBB FDSOI Technology, in IEEE Transactions on Device and Materials Reliability, vol. 16, no. 3, pp. 376-383, Sept. 2016. https://doi.org/10.1109/TDMR.2016.2584140
[30] L. Wu et al., Electrical Modeling of STT-MRAM Defects, 2018 IEEE International Test Conference (ITC), pp. 1-10, 2018. https://doi.org/10.1109/TEST.2018.8624749
[31] B. Sheu et al., Bsim: Berkeley short-channel igfet model for mos transistors, IEEE J. Solid-State Circuits (JSSC), vol. 22, no. 4, pp. 558–566, Apr. 1987. https://doi.org/10.1109/JSSC.1987.1052773
[32] X. Liu et al., Thermal stability of magnetic tunneling junctions with mgo barriers for high temperature spintronics, Appl. Phys. Lett., vol. 89, no. 2, pp. 023504, 2006. https://doi.org/10.1063/1.2219997
[33] Guoqiao Tao et al., On intrinsic failure rate of products with error correction, 2005 IEEE International Integrated Reliability Workshop, S. Lake Tahoe, CA, 2005, pp. 4. https://doi.org/10.1109/IRWS.2005.1609566
[34] Y. Zhou et al., A Self-Timed Voltage-Mode Sensing Scheme With Successive Sensing and Checking for STT-MRAM, in IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 5, pp. 1602-1614, May 2020. https://doi.org/10.1109/TCSI.2019.2960028
[35] Synopsys, MOS Device Aging Analysis with HSPICE and CustomSim, no. August, pp. 1–5, 2011.
[36] B. Tudor et al., MOSRA: An efficient and versatile MOS aging modeling and reliability analysis solution for 45nm and below, 2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology, Shanghai, 2010, pp. 1645-1647. https://doi.org/10.1109/ICSICT.2010.5667399
[37] P. R. Savanur et al., A BIST approach for counterfeit circuit detection based on NBTI degradation, 2015 IEEE International Symposium on DFTS, Amherst, MA, 2015, pp. 123-126. https://doi.org/10.1109/DFT.2015.7315148
[38] M. Sadi et al., BIST-RM: BIST-assisted reliability management of SoCs using on-chip clock sweeping and machine learning, 2016 IEEE International Test Conference (ITC), Fort Worth, TX, 2016, pp. 1-10. https://doi.org/10.1109/TEST.2016.7805862
[39] F. Ahmed et al., Reliable cache design with on-chip monitoring of NBTI degradation in SRAM cells using BIST, 2010 28th VLSI Test Symposium (VTS), Santa Cruz, CA, 2010, pp. 63-68. https://doi.org/10.1109/VTS.2010.5469614
[40] F. Firouzi et al., Re-using BIST for circuit aging monitoring, 2015 20th IEEE European Test Symposium (ETS), Cluj-Napoca, 2015, pp. 1-2. https://doi.org/10.1109/ETS.2015.7138768
[41] A. Rubio et al., Reliability issues in RRAM ternary memories affected by variability and aging mechanisms, 2017 IEEE IOLTS, 2017, pp. 90-92. https://doi.org/10.1109/IOLTS.2017.8046238