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### WET and Siconi<sup>®</sup> cleaning sequences for SiGe epitaxial regrowth

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## Abstract

SiGe channels can be used to boost the hole mobility and tailor the threshold voltage shift in advanced p-type Metal Oxide Semiconductor Field Effect Transistors. An efficient removal of SiGe oxides prior to the low temperature Selective Epitaxial Growth (SEG) of SiGe:B in the Sources/Drains regions of such devices is then mandatory. The H<sub>2</sub> bake that precedes SEG, carried out at temperatures typically lower than 650°C to avoid islanding or shape change, requires a very efficient removal of surface contaminants (such as C, F, O...), beforehand. As germanium is very reactive in the air, Siconi<sup>®</sup> in-situ surface preparation schemes are likely to be of use on SiGe surfaces with such thermal budget constraints. Recently, a new surface preparation strategy based on i) a wet chemical oxide formation followed by ii) a standard NH<sub>3</sub>/NF<sub>3</sub> remote plasma Siconi<sup>®</sup> process was evaluated. In order to use such a scheme for the fabrication of devices, we study here the impact of that surface preparation on the epitaxial regrowth of Si<sub>0.60</sub>Ge<sub>0.40</sub> on Si<sub>0.60</sub>Ge<sub>0.40</sub> films (in terms of oxygen removal efficiency, resulting morphology and so on). We show that such surface preparations yield drastically reduced interfacial contamination, with surfaces which can be rough after epitaxial re-growth, however. Thanks to an in-depth analysis of the interplay between surface preparation and growth parameters, an innovative process sequence is proposed that yields smooth, high-quality films.

## 1. Introduction

Electron and hole mobilities several times higher than in bulk, unstrained Si, are mandatory in advanced Metal Oxide Semiconductors Field Effect Transistors (MOSFETs) [1]. Compressively strained SiGe, with a Ge concentration typically around 30%, is for instance used to that end in the channel of 14 nm technology node p-type Fully Depleted Silicon-On-Insulator devices [2]. A Selective Epitaxial Growth (SEG) of tens of nm of heavily in-situ boron doped SiGe is performed in the Sources/Drains (S/D) regions of such devices. It is used to lower the contact resistance, have enough material for germano-salicidation and maintain (or increase) the compressive strain in the SiGe channel under the gate. Surface preparation prior to SiGe:B SEG is particularly tricky on SiGe surfaces, which are very reactive in the air. Starting surfaces should indeed be smooth at the atomic scale and free of any contaminants (such as O, C or F) prior to epitaxy. The minimization of Queue-time (Q-time, i.e. the amount of time spent in the air after removal of native oxide in single wafer wet cleaning tools) is thus more critical on SiGe than on silicon.

Surface preparation prior to epitaxy typically consists in “HF-last” wet sequences, which yield surfaces free from native oxide. However, industrial cluster tools have nowadays remote plasma *in-situ* pre-clean chambers to convert native oxides into salts, which are sublimated at low temperatures. Just after, wafers are transferred to the epitaxy chamber under ultra-pure N<sub>2</sub>; surface re-oxidation is thus completely avoided [3]–[6]. Usually, those wet or dry surface treatments are followed by an *in-situ* H<sub>2</sub> bake in the epitaxy chamber to remove the remaining contaminants [7]. This bake, conducted at temperatures typically 650°C and higher, can be deleterious to the SiGe channels of 14 nm node devices (and beyond), as they are thin and prone to faceting or moat recess at the edges of S/D regions / de-wetting (when on top of SiO<sub>2</sub>) / shape change (SiGe fins or SiGe layers cladding Si fins) and so on. Complementary MOS circuits might also be negatively impacted, as they are processed sequentially [6]. An efficient removal of contaminants with wet and/or in-situ surface preparation protocols and a low thermal budget (i.e. no more than a few minutes at temperatures of at most 650°C) is thus essential during the fabrication of advanced MOSFETs. Remote plasma using NH<sub>3</sub> and NF<sub>3</sub> (the so-called “Siconi<sup>®</sup>” process) is currently used for silicon surface preparation (with a maximum temperature of 180°C). Recently, we assessed its efficiency on SiGe surfaces. We showed that Siconi<sup>®</sup> enabled to remove GeO<sub>2</sub> and SiO<sub>2</sub> but was less efficient on GeO<sub>x</sub> [8]. This residual GeO<sub>x</sub> contamination after Siconi<sup>®</sup> was reduced thanks to the use beforehand of wet oxidation generating on

SiGe a SiO<sub>2</sub> rich surface oxide. In the current study, we continue that investigation by assessing the performances of various (i) wet, (ii) Siconi<sup>®</sup> and (iii) “wet-Siconi<sup>®</sup>” sequences on SiGe 40% surfaces with an epitaxial regrowth at reduced temperatures (under 650°C). With this new study, we i) highlight the high oxide and contamination removal efficiency of some sequences, ii) highlight a detrimental impact of some surface preparation schemes on surface morphology and iii) propose a solution to avoid surface roughening and have smooth, high quality films, in the end.

## 2. Experimental details

### Surface preparation conditions

In this work, 15 nm thick SiGe 40% layers were epitaxially grown at 600°C, 20 Torr on 300 mm bulk Si(001) wafers in a Reduced Pressure – Chemical Vapor Deposition tool from Applied Materials. The deposited thickness was lower than the critical thickness for plastic relaxation; SiGe films were thus fully compressively-strained. Standard 300 mm FOUPs (Entegris) were used for wafer storage in the clean room. Wet treatments were performed in a 300 mm single-wafer DNS SU 3100 tool. Various wet cleaning sequences (**Table 1**) based on the combination of standard Front-End chemistries with efficient rinse steps such as 1) diluted HF/HCl, 2) diluted, cold or hot Standard Cleanings 1 (SC1), i.e. NH<sub>4</sub>OH:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O solutions or 3) ozonated (O<sub>3</sub>) rinses were evaluated.

Chemical solutions	Chemical ratio	Treatment temperature	Time treatment	Rinse/Dry steps
HF/HCl	HF/HCl/H <sub>2</sub> O X/Y/98 (1<X, Y<10)	Ambient (22°C)	30 seconds	deionized Water rinse and N <sub>2</sub> dry
Cold or Hot SC1	NH <sub>4</sub> OH/H <sub>2</sub> O <sub>2</sub> /H <sub>2</sub> O X/Y/80 (1<X, Y<10)	Between 20 and 100°C	30 seconds	deionized Water rinse and N <sub>2</sub> dry
O <sub>3</sub> rinse	Ozone >10ppm	Ambient (22°C)	60 seconds	deionized Water rinse and N <sub>2</sub> dry

**Table 1:** Experimental process conditions for the wet cleaning sequences used in the DNS SU 3100 tool. In X/Y/98 or X/Y/80 ratios, X is the chemistry solution volume of HF or NH<sub>4</sub>OH, Y the chemistry solution volume of HCl or H<sub>2</sub>O<sub>2</sub>, and 98 or 80 the chemistry solution volume of water. The “1 < X, Y < 10” notation means that X is below 1 and Y below 10.

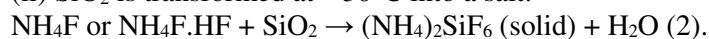
Meanwhile, exposure to a NH<sub>3</sub>/NF<sub>3</sub> remote plasma (followed by a low temperature salt sublimation step at T = 180°C) was performed at 3 Torr in a controlled atmosphere (H<sub>2</sub>, He, Ar) Siconi<sup>®</sup> chamber connected to the Applied Materials Centura cluster tool.

In the case of SiO<sub>2</sub>, Siconi<sup>®</sup> chemical reactions are as follows [8]:

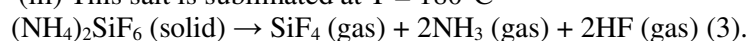
(i) Etchants are generated in a remote plasma cavity:



(ii) SiO<sub>2</sub> is transformed at ~30°C into a salt:

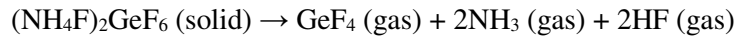


(iii) This salt is sublimated at T = 180°C



In the case of a Ge surface, GeO<sub>2</sub> can react with NH<sub>4</sub>F.HF to generate (NH<sub>4</sub>)<sub>2</sub>GeF<sub>6</sub> [9]. This ammonium hexafluorogermanate salt was shown to sublimate at 220°C [10]. Temperatures lower than that were not investigated, however. It is likely than the Siconi<sup>®</sup> process conditions mentioned above

yields  $(\text{NH}_4)_2\text{GeF}_6$  salts which sublime at  $180^\circ\text{C}$  thanks to the following reaction, i.e. that an efficient removal of  $\text{SiO}_2$  and  $\text{GeO}_2$  is feasible in it.



### Characterization

Several techniques were used to assess the quality of the SiGe pre-epitaxy surface preparation process.

Film thickness after re-epitaxy was determined thanks to X-Ray reflectivity (XRR) in an automated Jordan Valley Semiconductor JVX5200 tool (with a convergent X-Ray beam and a 1024 pixels CCD detector). Tapping-mode Atomic Force Microscopy measurements were carried out in a Bruker FastScan tool in order to estimate the SiGe roughness after exposure to chemicals or re-epitaxy. The AFM root mean square (rms) roughness values given in this paper were extracted from  $10 \times 10 \mu\text{m}^2$  scans performed on the center or at mid radius of the wafers. The roughness uniformity on the wafer was also controlled by haze, i.e. light diffusion measurements in a KLA Tencor SP2 tool.

Contaminant removal efficiency of the different treatments was studied by Secondary Ion Mass Spectrometry (SIMS). A TOF SIMS 5 tool from ION TOF was used for the SIMS analysis. C and O were analyzed by negative ion detection with a Cesium sputter ion beam. The 14.5 KeV  $\text{Cs}^+$  primary ion beam was raster scanned over a  $50 \times 50 \mu\text{m}^2$  area, while an optical and electronic gating limited the area for signal to a circle with a  $10 \mu\text{m}$  diameter. A long pumping time, a liquid nitrogen trap as well as a high sputter rate (at the expense of depth resolution) were used to lower the detection limits of the various elements. Depth calibration was obtained from crater measurement by stylus profilometry. The error bars on SIMS concentrations in the following were  $\pm 10\%$ , typically.

## 3. Results and discussion

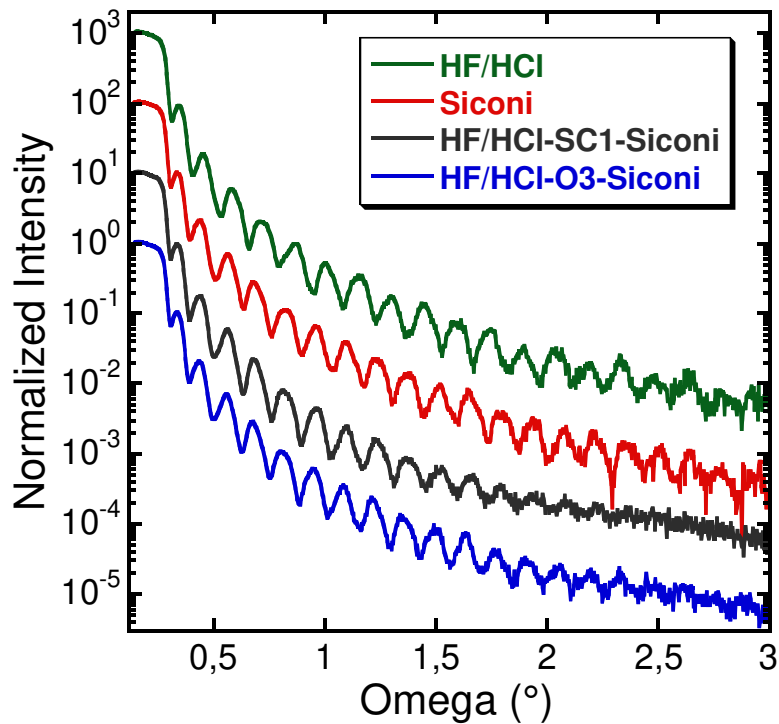
In the following, we have evaluated different (i) wet, (ii) Siconi<sup>®</sup> and (iii) “wet-Siconi<sup>®</sup>” sequences on 15 nm thick  $\text{Si}_{0.6}\text{Ge}_{0.4}$  layers with two Q-times, less than 15 min or 8 hours, between the wet cleaning and the Siconi<sup>®</sup> process. Without any air break, the Siconi<sup>®</sup> process was followed by wafer transfer under ultra-pure  $\text{N}_2$  to the epitaxy chamber and, there, a 20 Torr  $\text{H}_2$  bake (at a temperature inferior or equal to  $650^\circ\text{C}$ ) and a re-epitaxy at  $600^\circ\text{C}$ , 20 Torr of another 15 nm of  $\text{Si}_{0.6}\text{Ge}_{0.4}$ . The purpose of such a low thermal budget was to minimize its impact on contaminant removal efficiency and allows a proper benchmark of the various sequences probed. We first of all quantified the interest of using a chemical oxide-Siconi<sup>®</sup> sequence (previously evidenced by XPS [8]) in terms of interfacial contamination (SIMS and XRR) and film quality (Haze and AFM). The second goal of this study was to demonstrate the efficiency of such sequences in the real conditions of a 300mm industrial production line (FOUP processing of 25 wafers), with then tens of minutes up to a few hours Q-times between wet cleaning and loading in the inert environment of an epitaxial cluster tool. A Q-time of 8 hours seemed reasonable to show the robustness of the process in a production line.

### 3.1 Influence of surface preparations on interfacial contamination

#### Surface preparation using Q-time = 15 minutes

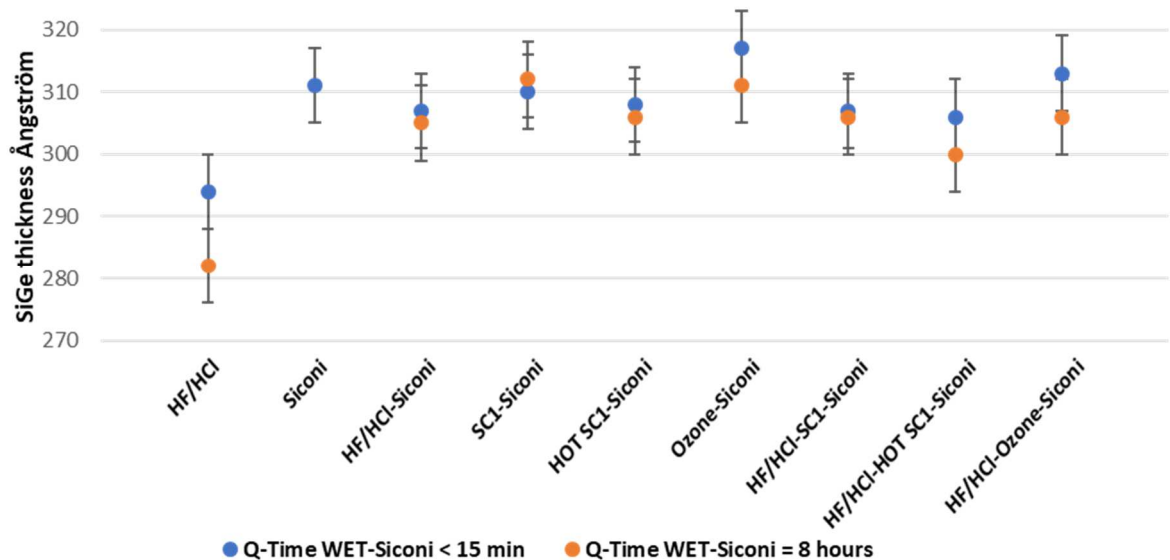
$\text{Si}_{0.60}\text{Ge}_{0.40}$  layers were, after the various chemical treatments (**Table 1**), loaded in the  $\text{N}_2$ -purged load-locks of the epitaxy cluster tool, subjected to the Siconi<sup>®</sup> process then transferred (under  $\text{N}_2$ ) to the epitaxy chamber where re-epitaxy was performed. Under those conditions, the exposure time of deoxidized surfaces to the air (between wet treatment and wafer loading in the load-locks), did not exceed 15 minutes. After  $\text{Si}_{0.60}\text{Ge}_{0.40}$  epitaxial regrowth, wafers were measured by X-Ray Reflectivity. Selected profiles can be found in **Figure 1**. Above the critical angle for total external reflection (at around  $0.13^\circ$ ), X-Rays propagate into the SiGe/Si stacks. Thickness fringes are due to constructive then destructive interferences between X-Rays reflected by the surface and at the SiGe/Si interface. Their angular spacing is inversely proportional to the overall SiGe layer thickness, while

their intensity is proportional to the density difference between Si and  $\text{Si}_{0.60}\text{Ge}_{0.40}$ , which is high ( $\rho(\text{Si}) = 2.33 \text{ g cm}^{-3}$ , to be compared with  $\rho(\text{Si}_{0.60}\text{Ge}_{0.40}) = 3.53 \text{ g cm}^{-3}$ ). The lack, at high incidence angles, of thickness fringes for HF/HCl-SC1-Siconi and, to a lesser extent, HF/HCl/O<sub>3</sub>-Siconi schemes is due to rough surfaces, as evidenced in Figure 7. Meanwhile, the smooth surfaces associated with HF/HCl and Siconi surface preparations (see Figure 4) result in the presence of thickness fringes at high incidence angles.



**Figure 1 :** X-Ray Reflectivity curves after the re-epitaxy of nominally 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  on top of 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  after various surface preparations with a Q-Time less than 15 minutes.

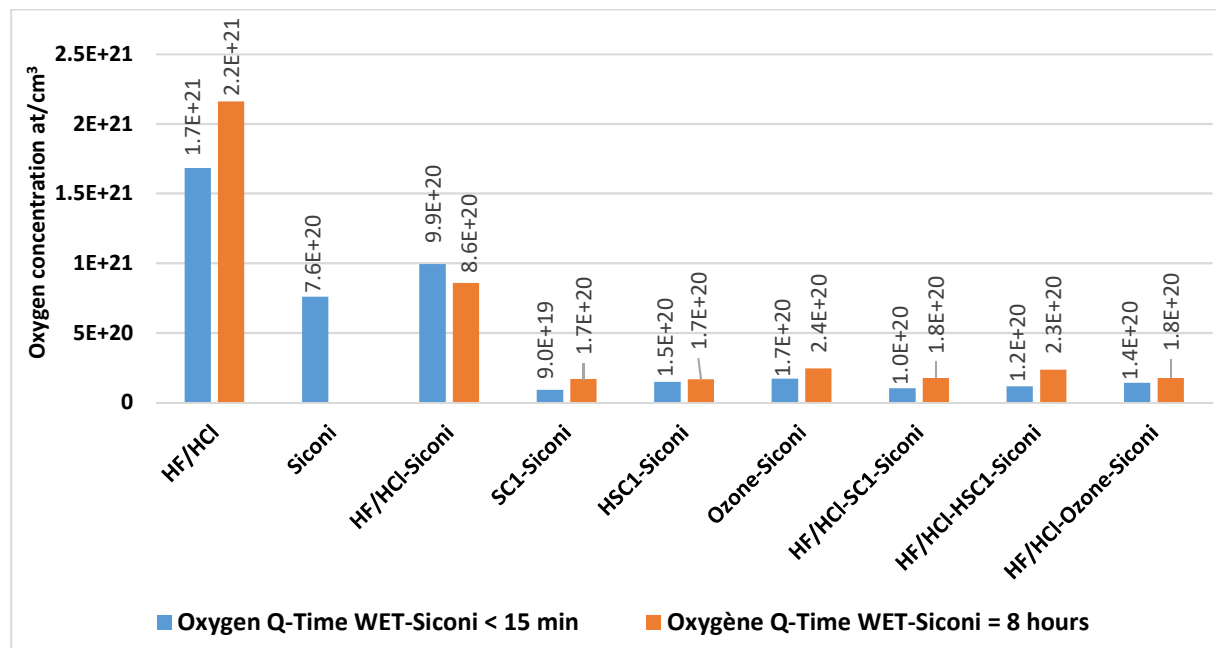
The thicknesses of the resulting bilayers are provided in **Figure 2** as a function of the surface preparation scheme used.



**Figure 2:** Thickness from XRR after the 600°C re-epitaxy of nominally 15 nm of Si<sub>0.60</sub>Ge<sub>0.40</sub> on top of 15 nm of Si<sub>0.60</sub>Ge<sub>0.40</sub> after various surface preparations with a Q-Time either less than 15 minutes or 8 hours.

The average thicknesses of the SiGe bi-layers are quite similar for Siconi<sup>®</sup>-based surface preparations, with a mean value of 310 Å. By contrast, the HF/HCl treatment yields a bi-layer thickness around 295 Å (i.e. 15 Å less than the other schemes evaluated). As a consumption of the initial SiGe layer with HF/HCl is highly unlikely (it would also have happened for the HF/HCl – Siconi sequence, then), this sharp SiGe thickness decrease is attributed to a lower thickness of the "upper" SiGe layer. A HF/HCl chemical treatment followed by air exposure most likely results in a delay before epitaxial growth proceeds (i.e. a growth retardation). This would be due to the presence of oxygen contamination on the starting surfaces, as highlighted for instance in Refs. [11]–[13].

SIMS depth profiling was performed in order to quantify the oxygen contamination at the interface for the various surface preparations probed (**Figure 3**).



**Figure 3:** Interfacial Oxygen concentration at the SiGe/SiGe interface for various surface preparations with Q-Times under 15 minutes or lasting 8 hours.

**HF/HCl:** a re-epitaxy after a HF/HCl wet treatment has the highest interfacial oxygen concentration of all. As noticed in our recent publication [8], deoxidized SiGe surfaces are very sensitive to re-oxidation. Even with a very short exposure to the air (<15 minutes), we have the highest amount of interfacial oxygen of all schemes (i.e.  $1.7 \cdot 10^{21}$  at/cm<sup>3</sup>). This high oxygen concentration confirms XRR thickness findings, with a growth delay with HF/HCl. A H<sub>2</sub> bake under 650°C is not sufficient to remove all oxygen residues on the starting SiGe surface after a “HF-Last” wet cleaning. This is fully in line with Ref. [7] findings, which showed that, to get rid of interfacial oxygen, temperatures superior or equal to 775°C should be used for the H<sub>2</sub> bakes, be it on Si or SiGe surfaces. In the current trend towards epitaxies at lower and lower temperatures, this type of surface preparation is clearly not performant enough.

**Siconi<sup>®</sup> and HF/HCl-Siconi<sup>®</sup>:** Epitaxial re-growths performed after Siconi<sup>®</sup> on native oxide and HF/HCl-Siconi<sup>®</sup> treatments result in relatively similar oxygen interfacial concentrations, which are still quite high ( $> 7.6 \cdot 10^{20}$  at/cm<sup>3</sup>). These results are consistent with XPS results in our recent study [8], which indicated that i) the Siconi<sup>®</sup> oxide removal process was not totally efficient on SiGe (imperfect removal of germanium sub-oxides, notably) ii) re-oxidation upon exposure to the air after a HF/HCl process resulted in an oxidation front made of germanium sub-oxides which cannot be completely removed with Siconi<sup>®</sup>. Silicon and germanium atoms, which are initially in a diamond

lattice with Si-Si, Si-Ge or Ge-Ge bonds, progressively oxidize at the oxidation front, with the formation of Si-O and Ge-O bonds with Si-Si, Si-Ge, Ge-Si or Ge-Ge “back” bonds [14], [15]. It is well known in the literature that  $\text{NH}_4\text{HF}$  and  $\text{HF}$  chemistries (used during the Siconi<sup>®</sup> process) have very little impact on the latter types of bonds. We thus believe that sub oxides with back bonds are not transformed into  $\text{SiF}_6(\text{NH}_4)_2$  and  $\text{GeF}_6(\text{NH}_4)_2$  salts during the Siconi<sup>®</sup> process, with therefore no sublimation and thus removal from the starting surface. The use of a Siconi<sup>®</sup> process does not solve by itself all the problems on SiGe surfaces which are sensitive indeed to surface oxidation.

**"Chemical oxide-Siconi<sup>®</sup>":** In agreement with our previous study [8], SIMS data (**Figure 3**) show that wet processes producing Si-rich chemical oxides (SC1, H(ot) SC1 and Ozone) combined with a Siconi<sup>®</sup> process drastically reduce interfacial oxygen contamination (between  $1.02 \cdot 10^{20}$  and  $1.41 \cdot 10^{20}$  at/cm<sup>3</sup>). In Ref. [8], we explained that SC1 or O<sub>3</sub>-based solutions oxidize the surface by generating silicon and germanium oxides. While silicon oxides dissolve very slowly (generating the chemical oxide layer), Ge oxides are "pulled out" of the oxide, as they dissolve quite rapidly. This results in the formation of a SiO<sub>2</sub>-rich chemical oxide. This is likely the reason why the oxide removal efficiency on SiGe surfaces is higher with Siconi<sup>®</sup>, then, as the amount of germanium sub-oxides (which are difficult to remove with Siconi<sup>®</sup> processes) is lower after dips in SC1 or ozone.

SIMS results confirm our previous result and show the interest of using "chemical oxidation-Siconi<sup>®</sup>" type sequences. This first series of tests was performed by doing in a row "wet cleaning", wafer transfer in the load-locks, Siconi<sup>®</sup> then re-epitaxy, i.e. with surface exposures to the air less than 15 minutes, typically. However, and as already mentioned above, a 300mm industrial production line uses Front Opening Unified Pods (or FOUPs) with 25 wafers which are cleaned one by one with a process duration of a few minutes, typically. This means that the Q-time between wet treatment and epitaxy varies between less than 15 minutes and more than one hour, typically. It might also be that wafers need to be cleaned a few hours prior to loading in the epitaxy tool because of various production constraints (multiple tools availability and so on). To evaluate the robustness of the various surface preparation processes evaluated in section 3.1, we have carried out the same epitaxial re-growth than before, with this time the wafers staying for 8 hours in the FOUP after wet treatments and prior to loading in the inert environment of the epitaxial cluster tool.

### 3.2 Impact of Q-time on the oxygen contamination

The same XRR measurements as before were performed after re-epitaxy on the SiGe bi-layers, this with a Q-time of 8 hours. Thicknesses are provided in **Figure 2**.

All Siconi<sup>®</sup> - based sequences tested resulted in total SiGe thicknesses close to 310 Å, as for 15 min. Q times. Meanwhile, a HF/HCl treatment results in a combined thickness of 282 Å after 8 hours, to be compared with 295 Å for a 15 minutes Q time. This is likely due to a further growth delay induced by an even higher amount of interfacial oxygen with 8 hours Q-times, which is quite logical [13]. **Figure 3** shows the interfacial oxygen concentrations (at/cm<sup>3</sup>) after the use of various surface preparations with 8 hours or less than 15 minutes Q-times.

- **HF/HCl:** Epitaxial re-growth after a HF/HCl treatment results in the highest oxygen interfacial contamination. An increase of the Q-time between HF/HCl and epitaxy amplifies this phenomenon (from  $1.7 \cdot 10^{21}$  cm<sup>-3</sup> (15 min.) up to  $2.1 \cdot 10^{21}$  cm<sup>-3</sup> (8 hours)). This is fully in line with a re-oxidation after exposure to the air of “HF-last” SiGe surfaces and the growth delays observed with this type of surface preparation.

- **HF/HCl-Siconi<sup>®</sup>:** Epitaxial re-growths after HF/HCl-Siconi<sup>®</sup> treatments have nearly the same oxygen interfacial contamination whatever the Q-time ( $9.9 \cdot 10^{20}$  cm<sup>-3</sup> (15 min.)  $\leftrightarrow$   $8.6 \cdot 10^{20}$  cm<sup>-3</sup> (8 hours)). This shows the Siconi<sup>®</sup> inability of properly eliminating germanium sub-oxides present on re-oxidation fronts after a HF/HCl treatment followed by some exposure to the air.

- **"Chemical oxidation-Siconi<sup>®</sup>":** There is a slight increase in the oxygen concentration with "chemical oxide-Siconi<sup>®</sup>" treatments after 8 hours Q-times compared to less than 15 minutes (on average,  $2 \cdot 10^{20}$  cm<sup>-3</sup> to be compared with  $1.3 \cdot 10^{20}$  cm<sup>-3</sup>). The oxygen concentrations at the SiGe/SiGe

interface remain very low compared to HF/HCl based sequences, however, and differences between short and long queue times modest indeed compared to “HF/HCl” only, for instance ( $0.7 \times 10^{20} \text{ cm}^{-3} \leftrightarrow 4.8 \times 10^{20} \text{ cm}^{-3}$ ). Besides a considerable gain in terms of oxygen removal efficiency, sequences calling upon the formation of chemical oxides reduce by a factor of more the 6 the impact of air exposure on oxygen interfacial contamination, which is a major advantage given the amount of time wafers spent inside a FOUP after wet cleaning (and prior to Siconi<sup>®</sup>) in a production line

To conclude, SIMS and XRR data showed that the high air reactivity of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  surfaces after HF/HCl wet cleanings resulted in very high interfacial oxygen levels and growth delays. Although there was no growth delays anymore after the use of Siconi<sup>®</sup>-based sequences, large interfacial oxygen concentration differences were evidenced by SIMS depending on the wet cleaning used beforehand. Siconi<sup>®</sup> only and HF/HCl-Siconi<sup>®</sup> treatments yielded intermediate interfacial oxygen concentrations (lower than HF/HCl only, but definitely higher than with wet oxidizing). These oxygen levels show once again the inability of Siconi<sup>®</sup> of eliminating germanium sub-oxides. Our strategy of forcing the formation of  $\text{SiO}_2$ -rich chemical oxides on SiGe surfaces resulted in the lowest oxygen interfacial contaminations by far, overcoming the Siconi<sup>®</sup> weakness. These results confirm the conclusions of our recent paper [8] and are in line with recent studies by M. Labrot et al [6], [14], which showed a better oxide removal efficiency on  $\text{Si}_{0.73}\text{Ge}_{0.27}$  surfaces with "HF-RCA-Siconi<sup>®</sup>" sequences (RCA, which stands for Radio Corporation of America, is made of dips in SC1 and SC2 ( $\text{H}_2\text{O}_2:\text{HCl}:\text{H}_2\text{O}$ ) solutions). In addition, the still low oxygen concentrations of "chemical oxide-Siconi<sup>®</sup>" sequences with 8-hour Q-times showed the robustness of this strategy. Beyond interfacial contamination, the morphology of the bi-layers is a good indicator of the epitaxial re-growth quality. Having smooth bi-layers is mandatory for use in advanced transistors.

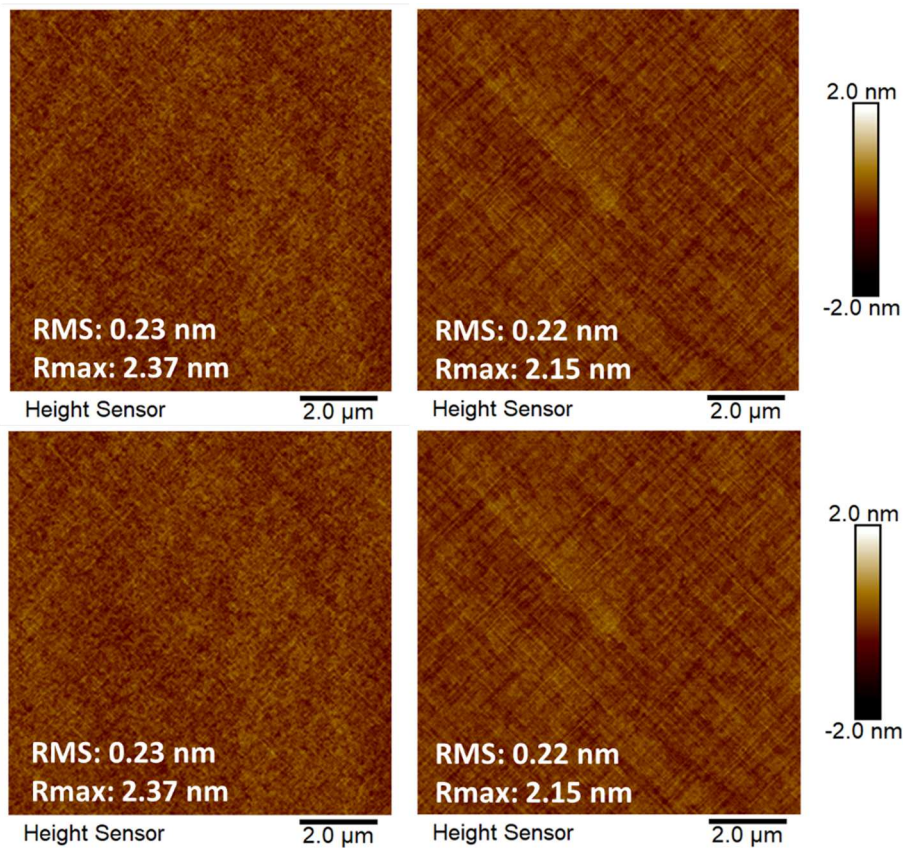
### 3.3 Morphological impact

We used "haze" (mapping at the wafer scale) and AFM (local roughness measurements) to characterize the impact of various surface preparations on the morphological quality of epitaxial re-growths.

#### HF/HCl and Siconi<sup>®</sup> only surface preparations

Haze is homogeneously low over the whole surface of those wafers (around 3 parts per million or ppm).  $10 \mu\text{m} \times 10 \mu\text{m}$  AFM images of those surfaces after epitaxial regrowth with, beforehand, HF/HCl or Siconi<sup>®</sup> only treatments, are provided in **Figure 4**. AFM scans do not show the presence of any specific defects (such as islands or pits). The root mean square roughness at the center and mid-radius of these wafers are low (0.2 nm). There is however a  $\langle 110 \rangle$  structuring of the surface in both cases akin to a "cross-hatch". Such a surface feature is due to the propagation of the threading arms of  $60^\circ$  misfit dislocations on  $\{111\}$  planes, leaving in their wake small “plough” lines on the surfaces. This is likely due to an overall  $\text{Si}_{0.60}\text{Ge}_{0.40}$  thickness after epitaxial re-growth slightly higher than the critical thickness for plastic relaxation, which is close to 30 nm for 40% of Ge [15]–[17]. The thickness of the bilayer is not the only parameter dictating the appearance (or not) of misfit dislocations. Indeed, as described in the literature [18]–[20], an initially defective SiGe surface (i.e. which is rough or with the presence of oxides on top) may result in a misfit dislocations density increase. The small size and the high density of “plough” lines on the surface is due to the reduced velocity of the threading arms of those misfit dislocations. This is due to the epitaxial re-growth temperature, which is low indeed ( $600^\circ\text{C}$ ), with therefore less energy to have step bunching and therefore long spatial wavelength, high amplitude surface undulations. Those reduced-quality bi-layers might be due to the high concentrations of residual oxygen after those surface preparations.

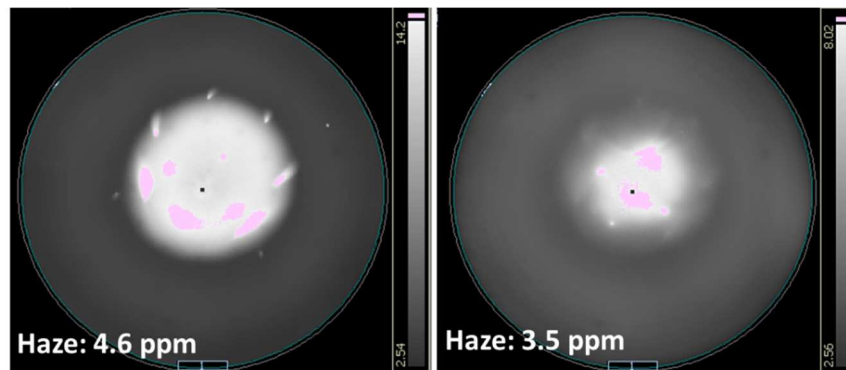




**Figure 4:** 10  $\mu\text{m}$  x 10  $\mu\text{m}$  AFM images after epitaxial re-growth of nominally 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  on top of 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  with, beforehand, HF/HCl (left) or Siconi<sup>®</sup> only (right) surface preparations. Top row: wafer center, bottom row: mid radius.

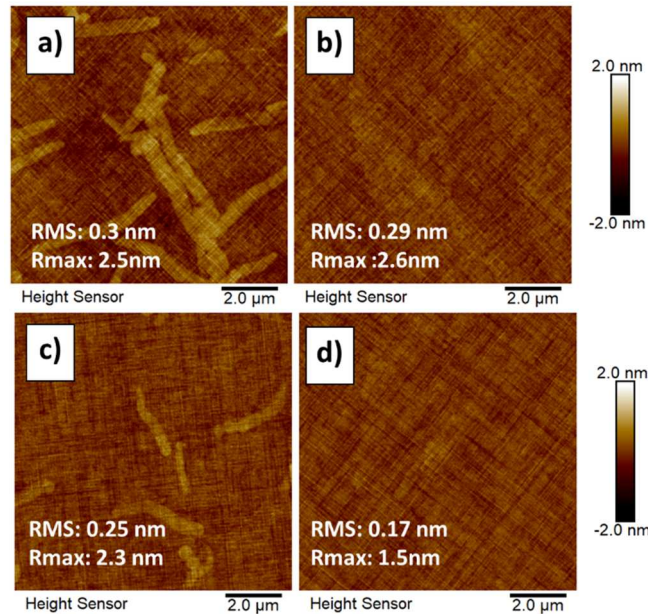
### HF/HCl-Siconi<sup>®</sup> sequences

Haze maps of the SiGe surfaces after HF/HCl-Siconi<sup>®</sup> sequences then epitaxial re-growths are provided in **Figure 5**. There are two distinct zones on the wafers, a central one with a high haze value and an outer one, with a lower haze value. HF/HCl-Siconi<sup>®</sup> sequences with 8-hour Q-times have a lower average haze value (3.5 ppm) than with 15 minutes Q-times (4.6 ppm). In addition, HF/HCl-Siconi<sup>®</sup> sequences with an 8-hour Q-time show a lower contrast between the central and the periphery area than with a 15 minutes Q-time. This shows that air exposure partly suppress roughening resulting from the use of HF/HCl-Siconi<sup>®</sup> sequences.



**Figure 5:** Haze maps of the wafers after the epitaxial re-growth of nominally 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  on top of 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  with, beforehand, a HF/HCl-Siconi<sup>®</sup> surface preparation scheme and Q-times either less than 15 minutes (left) or 8 hours long (right).

AFM measurements were performed in the two areas of the wafers (**Figure 6**). AFM images at the edge of the wafers are similar to those with Siconi<sup>®</sup> alone (low surface roughness and numerous small dimensions <110> ‘plough’ lines because of plastic strain relaxation). AFM images in the center of the wafers show, besides the presence <110> ‘plough’ lines, elongated patterns. Their density is smaller with 8 hours Q-times than 15 minutes Q-times. Haze and AFM measurements both indicate that air exposure between HF/HCl and Siconi<sup>®</sup> reduces the amount of defects stemming from the use of HF/HCl-Siconi<sup>®</sup> sequences.



**Figure 6:** 10  $\mu\text{m}$  x 10  $\mu\text{m}$  AFM images after the epitaxial re-growth of nominally 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  on top of 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  with, beforehand, a HF/HCl-Siconi<sup>®</sup> surface preparation scheme and Q-times either less than 15 minutes (top row images) or 8 hours long (bottom row images). a) and c): wafer center, b) and d): wafer edge.

The HF/HCl-Siconi<sup>®</sup> sequence was also performed on 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  without any epitaxial regrowth afterwards. The same kind of elongated defects were present in the center of the wafers, meaning that those patterns did not appear during re-epitaxy. They might be due to droplet formation on SiGe surfaces (which are more hydrophilic than Si surfaces, anyway) during rinsing and / or drying steps, resulting in local oxidation and therefore the formation of patterns on the surface after Siconi<sup>®</sup>. The lower defects density with 8 hours instead of less than 15 minutes Q-times supports our hypothesis that defects are due to water marks on the surface after HF/HCl. Indeed, when the Siconi<sup>®</sup> process is implemented directly (<15 minutes), the oxidized zones, where droplets were present, are preferentially deoxidized, generating the patterns observed by AFM. When the SiGe surface is left to the air for 8 hours after HF/HCl, oxidation is more homogeneous, attenuating the differences between areas under droplets and the rest of the surface. As shown in the literature [21], [22], the presence of water mark defects appearing during rinsing and/or drying steps on hydrophobic surfaces can be limited through the use of an isopropanol solution (IPA) during rinsing to reduce the surface tension.

### Chemical Oxide-Siconi<sup>®</sup> sequences with a Q-time <15 min

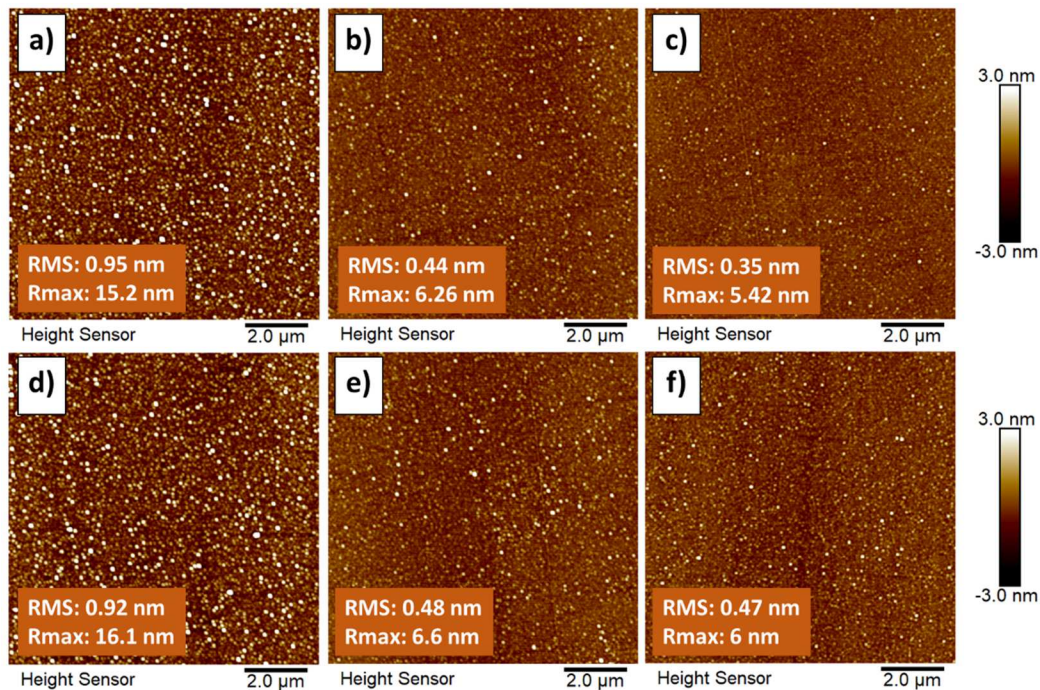
As for HF/HCl and Siconi only, the haze maps after SiGe epitaxial regrowth with different "chemical oxide-Siconi<sup>®</sup>" surface preparations are spatially homogenous at the wafer scale. Haze value with Chemical oxide-Siconi<sup>®</sup> (around 5 ppm) sequences are definitely higher than with HF/HCl or Siconi<sup>®</sup> only (around 3 ppm). This clearly indicates that these surfaces are rougher.

As seen in **Figure 7**, a SiGe 40% re-epitaxy after "chemical oxide-Siconi<sup>®</sup>" treatments results in rough surfaces, with the presence of a high density of islands-type defects uniformly distributed on the surface. AFM images do not allow at this stage to understand either the nature or the



source of those 3D defects. The epitaxially re-grown SiGe 40% layers are thus most likely of poor crystalline quality, which was unexpected given the superior performances of such treatments in terms of oxygen removal efficiency and lack of growth delay. Without re-epitaxy, 15 nm thick SiGe 40% films are free of defects and perfectly smooth after the use of “chemical oxide – Siconi<sup>®</sup>” surface treatments, however [8]. It should also be remembered that bi-layers are smooth after the use of HF/HCl or Siconi<sup>®</sup> only, as clearly demonstrated in **Figure 4**.

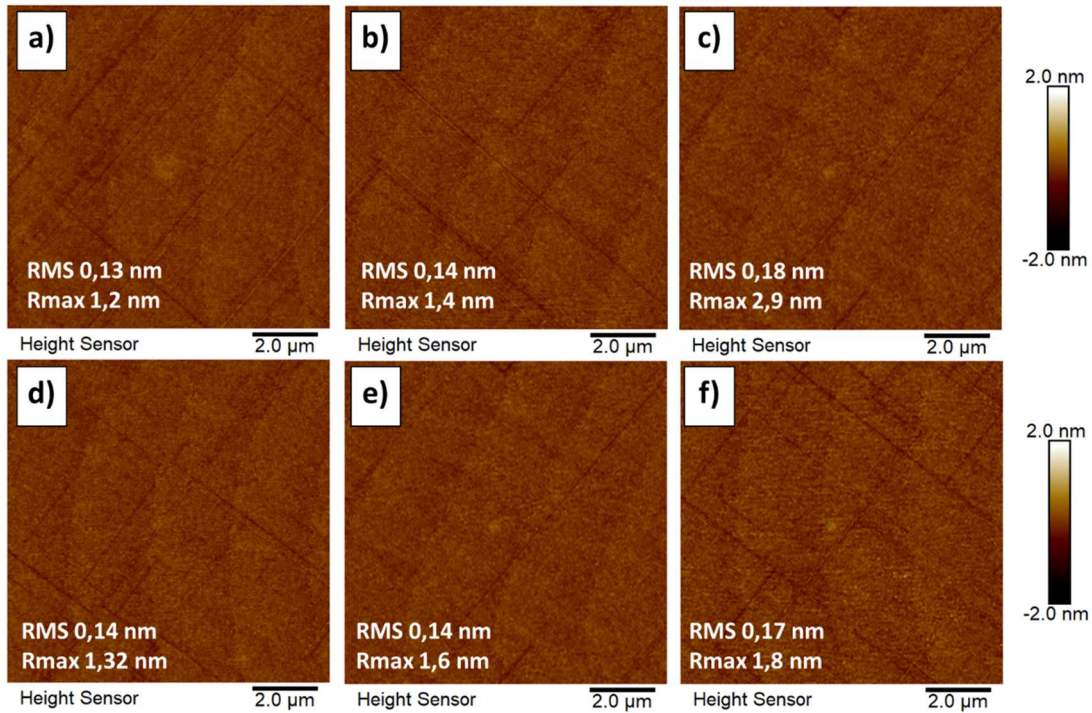
This defective surface state after re-epitaxy is obviously not compatible with device integration. Although we are convinced that "chemical oxide-Siconi<sup>®</sup>" surface preparations are very promising on SiGe alloys sensitive to re-oxidation, certain areas of shadow remain at that stage in the understanding of the "surface preparation-epitaxy" interaction.



**Figure 7:** 10 μm x 10 μm AFM images after the epitaxial re-growth of nominally 15 nm of Si<sub>0.60</sub>Ge<sub>0.40</sub> on top of 15 nm of Si<sub>0.60</sub>Ge<sub>0.40</sub> with, beforehand, different surface preparations and a Q-Time <15 minutes; a) SC1-Siconi, b) Hot-SC1-Siconi<sup>®</sup>, c) Ozone-Siconi<sup>®</sup>, d) HF/HCl-SC1-Siconi, e) HF/HCl-hot SC1-Siconi<sup>®</sup> and f) HF/HCl-ozone-Siconi<sup>®</sup>

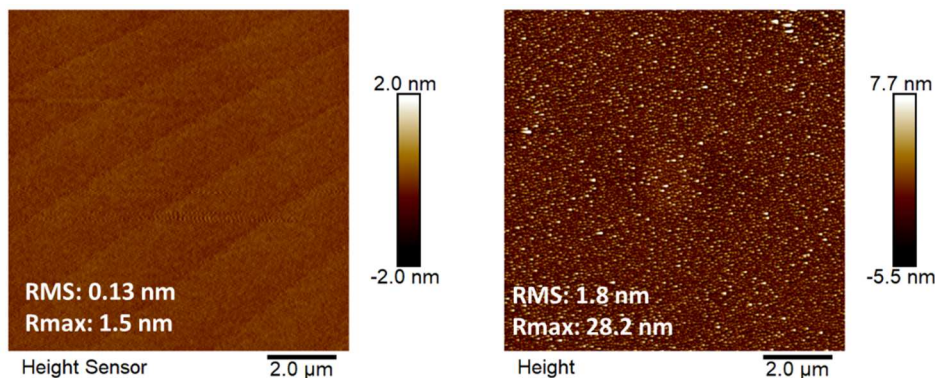
### Chemical oxide-Siconi<sup>®</sup> sequences with a Q-time of 8 hours

Haze measurements after SiGe epitaxial re-growth with different "chemical oxide-Siconi<sup>®</sup>" surface preparations and Q-times of 8 hours were homogenous over the wafer surfaces. Haze values were low (around 1ppm), in marked contrast with samples with Q-times less than 15 minutes, meaning that the surfaces were flat. This was confirmed with AFM, with low rms roughness values whatever the wet cleaning used (**Figure 8**). In the case of an Ozone-Siconi<sup>®</sup> surface preparation, AFM measurements show the presence of numerous medium-sized dislocation “plough” lines. This is likely due to a slight crystalline quality deterioration of the bi-layer. Only a few elongated dislocation “plough” lines (synonymous with a better crystalline quality) were by contrast observed with the other types of surface preparations. This might be due to different germanium oxide depletions and therefore different chemical oxides with SC1 or ozone. It should however be noticed that this difference disappears as soon as the native oxide on SiGe is removed prior to the oxidizing step thanks to HF/HCl.



**Figure 8:** 10  $\mu\text{m}$  x 10  $\mu\text{m}$  AFM images after the epitaxial re-growth of nominally 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  on top of 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  with, beforehand, different surface preparations and a 8 hours Q-Time; a) SC1-Siconi, b) Hot SC1-Siconi<sup>®</sup>, c) Ozone-Siconi<sup>®</sup>, d) HF/HCl-SC1-Siconi, e) HF/HCl-Hot SC1-Siconi<sup>®</sup> and f) HF/HCl-ozone-Siconi<sup>®</sup>

These morphological results after "chemical oxide-Siconi<sup>®</sup>" surface preparations are quite surprising. We explored the potential causes of this formation of the 3D defects after re-epitaxy. New experiments were performed to characterize the impact the  $\text{H}_2$  annealing prior to epitaxy had on a  $\text{Si}_{0.60}\text{Ge}_{0.40}$  surface with a "HF/HCl-chemical oxide-Siconi<sup>®</sup>" conditioning and a Q-time less than 15 minutes. To that end, we imaged the surfaces of 15 nm thick  $\text{Si}_{0.60}\text{Ge}_{0.40}$  films with a "HF/HCl-SC1-Siconi" sequence (and a Q-time of less than 15 minutes) with or without the use afterwards of a 2 minutes  $\text{H}_2$  bake (at a temperature inferior or equal to  $650^\circ\text{C}$ ). AFM images of the two types of surfaces are provided in **Figure 9**. While the SiGe surface is smooth after the "HF/HCl-SC1-Siconi" sequence, it definitely roughens after the  $\text{H}_2$  bake, with rms and Z ranges values 15 times higher, typically!



**Figure 9:** 10  $\mu\text{m}$  x 10  $\mu\text{m}$  AFM images of 15 nm thick  $\text{Si}_{0.60}\text{Ge}_{0.40}$  layers with, beforehand, a "HF/HCl-SC1-Siconi<sup>®</sup>" surface preparation without (left) or with (right) a low temperature  $\text{H}_2$  bake afterwards (right)

It is well known that the growth of Ge on Si(001) might result, because of the compressive strain in Ge, in a Stranski-Krastanov growth, with the formation of a wetting layer with numerous islands on top [25]. If high Ge content SiGe layers are grown at high temperatures, they might undulate in order to elastically relax the built-in compressive strain [26]. Beyond that, germanium has a much lower de-wetting and agglomeration temperature than silicon. P.P. Zhang *et al.* explained that this de-wetting temperature drop (to a value as low as 700°C) was due to a weakening of the chemical bonds and an increase of deformations in the crystalline lattice because of the presence of germanium atoms [27].

The 3D defects evidenced in **Figures 7 and 9** are therefore likely due to an islanding of the top part of the starting SiGe layer during the H<sub>2</sub> bake. We however need to understand why this islanding is present only with "chemical oxide-Siconi<sup>®</sup>" surface preparations. During the *thermal* oxidation of SiGe layers [28], [29], silicon is preferentially oxidized, with an accumulation of germanium under the thermal oxide (Ge enrichment or "snowplow" effect). Given the high thermal budget used (tens of minutes up to hours at temperatures above 900°C, typically), germanium atoms under the oxidation front then diffuse into the SiGe layer underneath. Although our oxidizing solutions are implemented at much lower temperatures (Room Temperature up to 100°C), we believe that the preferential oxidation of silicon also results in the presence of a high amount of germanium atoms in the first few monolayers under the oxidation front. Indeed, Ge atoms will not diffuse into the SiGe layer given the very low process temperature.

We thus explain 3D defects formation as follows: exposure to oxidizing chemistries results in the presence of a few Ge-rich monolayers under the SiO<sub>2</sub> chemical layer. If the Siconi<sup>®</sup> treatment is performed with a Q-time minimization (<15 min), the chemical oxide will be efficiently removed, leaving those Ge-rich monolayers on the extreme surface. The latter will be sensitive to the H<sub>2</sub> bake and will be prone to islanding, resulting in 3D defects. Unpublished X-ray Photoelectron Spectroscopy studies have shown that SC1 and Ozone-based chemical oxides on SiGe surface change upon lengthy air exposures. When a chemical oxide on top of a SiGe layer is exposed to the air for a certain amount of time, 8 hours in Figure 9 case, the top Ge-rich monolayers will be oxidized. The Siconi<sup>®</sup> process used afterwards will then remove not only the chemical oxide but also the germanium-enriched top layer (which was oxidized upon lengthy air exposure). The deoxidized SiGe surface, devoid of any germanium-enriched layers, is less sensitive to thermal budget and does not roughen during the H<sub>2</sub> bake.

### **New epitaxial recovery strategy**

Our studies showed that "chemical oxide-Siconi<sup>®</sup>" treatments were the only ones yielding low levels of oxygen interfacial contamination. However, these sequences generated surfaces prone to roughening, with the formation of islands during the low thermal budget H<sub>2</sub> anneal which preceded epitaxy. These islands have a deleterious impact on the quality of SiGe layers grown on top. In order to inhibit SiGe surface roughening after "chemical oxide-Siconi<sup>®</sup>" sequences, we have evaluated the interest of injecting dichlorosilane (DCS) together with H<sub>2</sub> during the various stages of the 20 Torr bake.

DCS was selected as a Si precursor (instead of silane or disilane, for instance) as the Si homo-epitaxial growth rate is very low for temperatures inferior or equal to 650°C [30]. It indeed increases exponentially with the growth temperature, with an activation energy of 2.52 eV, reaching 5 Å/min. only at 650°C. Sending DCS on a SiGe surface will result in a growth rate which is at first high, as Ge atoms on the surface catalyze the desorption of H atoms passivating the surface. Getting away from that interface and reaching a full Si coverage (after the deposition of a few monolayers) will result in Si growth rates which slow down dramatically as H passivation is definitely higher, then [31].

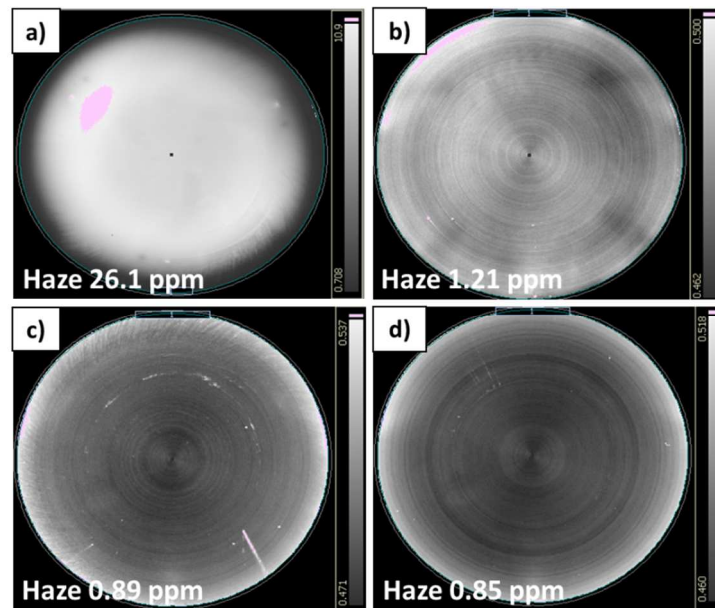
This injection of DCS during the H<sub>2</sub> bake aims to encapsulate the Ge-rich top surface with a few monolayers of Si, protecting it from islanding. Such a strategy was conclusively used by us in the 2000s to passivate (compressively-strained) Ge surfaces with Si prior to MOSFET fabrication [19], [31].



The H<sub>2</sub> bake we have used before is divided into three steps:

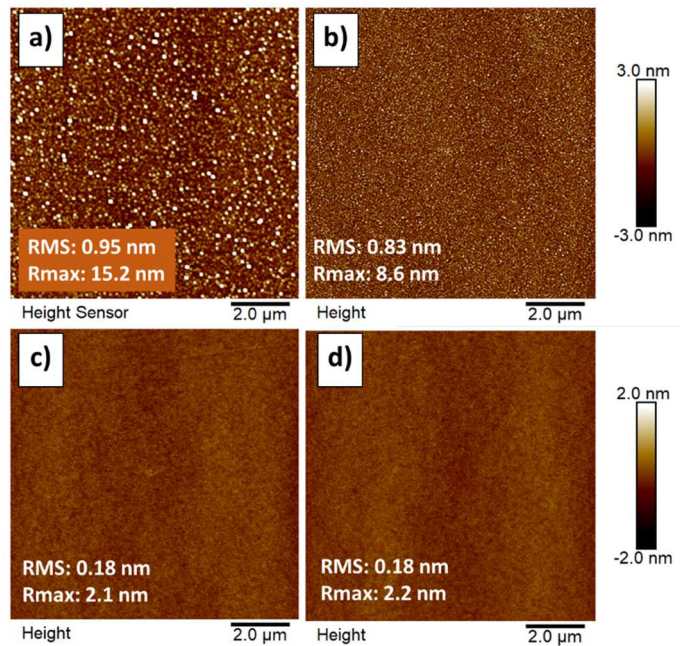
- (i) Temperature stabilization (at ~ 500°C for 30s) after wafer loading into the epitaxy chamber.
- (ii) Temperature ramping-up (2°C/sec)
- (iii) 2 minutes H<sub>2</sub> bake at a temperature inferior or equal to 650°C.

After a "HF/HCl-SC1-Siconi<sup>®</sup>" surface preparation with a Q-time less than 15 minutes, we have injected dichlorosilane during 1) the temperature stabilization only (i), 2) the temperature stabilization then the ramping-up (i + ii), 3) the temperature stabilization, the ramping-up then the H<sub>2</sub> bake itself (i + ii + iii). **Figure 10** shows the corresponding haze maps.



**Figure 10:** Haze maps after the epitaxial re-growth of nominally 15 nm of Si<sub>0.60</sub>Ge<sub>0.40</sub> on top of 15 nm of Si<sub>0.60</sub>Ge<sub>0.40</sub> with, beforehand, a "HF/HCl-SC1-Siconi<sup>®</sup>" surface preparation with a Q-time <15 minutes and dichlorosilane injection at various stages of the H<sub>2</sub> bake that precede epitaxy: a) without any injection during that bake, b) DCS injection during temperature stabilization, c) DCS injection during the temperature stabilization then the ramp-up and d) DCS injection during the temperature stabilization, the ramp-up and the 2 minutes H<sub>2</sub> bake (at T ≤ 650°C).

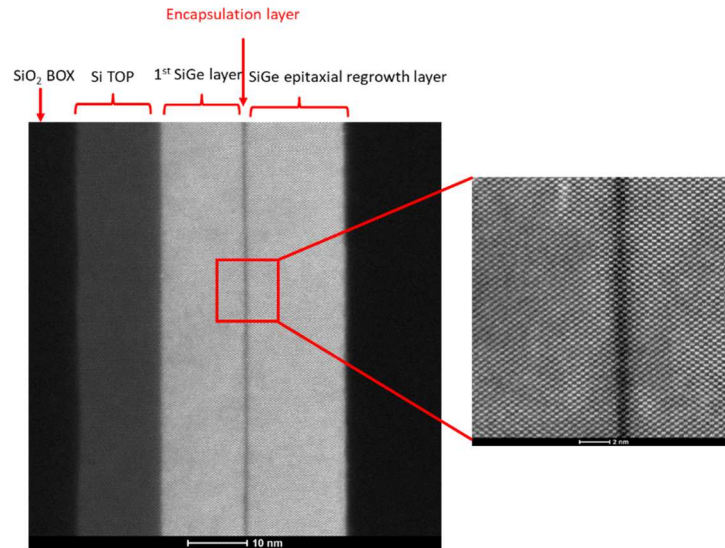
It is obvious that the injection of the DCS during the various stages of the H<sub>2</sub> bake greatly reduces haze values and therefore the surface roughness, as confirmed by the AFM images shown in **Figure 11**.



**Figure 11:** 10  $\mu\text{m}$  x 10  $\mu\text{m}$  AFM images after the epitaxial re-growth of nominally 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  on top of 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  with, beforehand, a "HF/HCl-SC1-Siconi<sup>®</sup>" surface preparation with a Q-time <15 minutes and dichlorosilane injection at various stages of the  $\text{H}_2$  bake that precedes epitaxy: a) without any injection during that bake, b) DCS injection during temperature stabilization, c) DCS injection during the temperature stabilization then the ramp-up and d) DCS injection during the temperature stabilization, the ramp-up and the 2 minutes  $\text{H}_2$  bake itself (at  $T \leq 650^\circ\text{C}$ ).

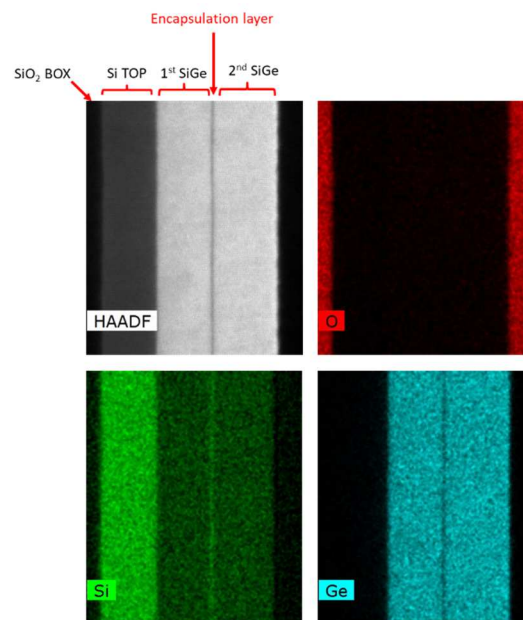
Although the surface roughness decreases upon the injection of DCS during temperature stabilization, AFM images nevertheless show the presence of small 3D defects which have a negative impact on roughness. DCS injection during temperature stabilization, ramp-up (and the  $\text{H}_2$  anneal itself) results by contrast in smooth surfaces without islands anymore. Those surfaces are also free of any "plough" lines coming from the propagation of the threading arms of misfit dislocations, indicating that bi-layers have a very good crystalline quality thanks to the injection of DCS prior to re-epitaxy.

Cross-sectional TEM observations were performed on the bi-layer with DCS injection during the temperature stabilization then the ramping-up. Images can be found in **Figure 12**. The roughly 1 nm thick silicon-rich encapsulation layer between the two SiGe layer can easily be seen, together with the Silicon-On-Insulator substrate on which the starting SiGe 40% layer was grown (in order to be closer to actual Fully Depleted - Silicon-On-Insulator devices). The SiGe layer grown on top is free of extended defects at the TEM scale, with a perfect extension of the atomic columns between the various layers of the stack.



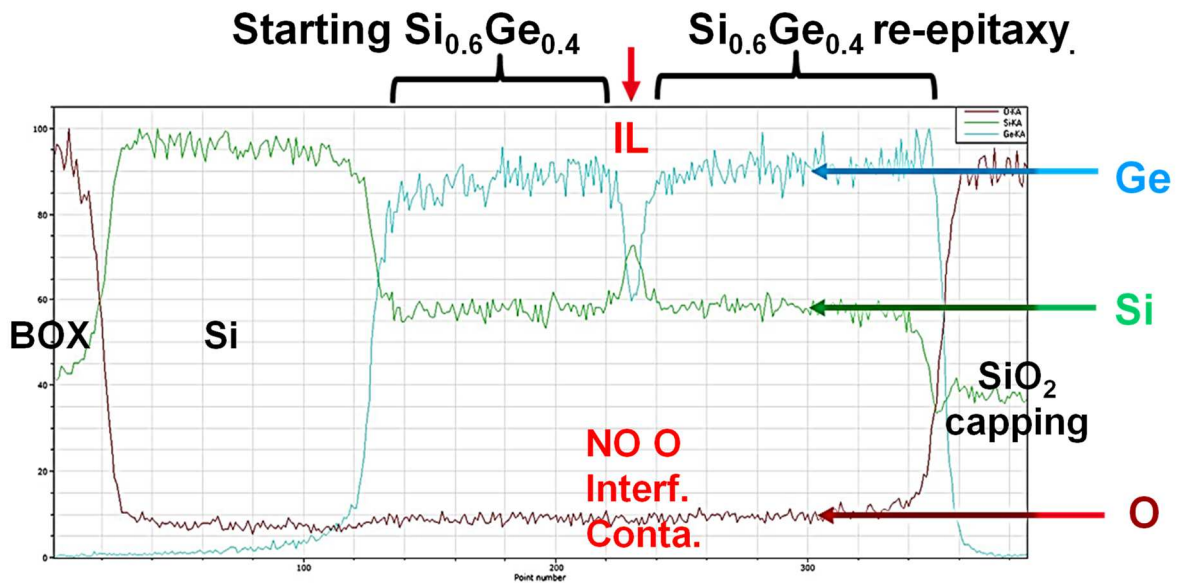
**Figure 12:** Cross-sectional STEM-HAADF (high-angle annular dark field) image after the epitaxial re-growth of 17 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  on top of 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  (itself on a SOI substrate) with, beforehand, a "HF/HCl-SC1-Siconi<sup>®</sup>" surface preparation with a Q-time <15 minutes and dichlorosilane injection during the temperature stabilization then the ramp-up.

EDX maps can be found in **Figure 13**. We do not observe oxygen at the interface. The passivation layer between the two SiGe 40% layer is also easily seen. It should also be noticed that, when looking at the silicon and germanium elemental maps, the Si-rich encapsulation layer seems to be a SiGe alloy with a Ge content in the 20% to 30% range (hence the denomination "Si-rich" encapsulation layer adopted in the manuscript). Those findings are confirmed by the EDX depth profiling of O, Si and Ge in that stack (see **Figure 14**). Individual layers can clearly be seen, with a lack of O interfacial contamination.



**Figure 13:** High Angle Annular Dark Field cross-sectional TEM image together with O, Si and Ge EDX maps after the epitaxial re-growth of 17 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  on top of 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  (itself on a SOI substrate) with, beforehand, a "HF/HCl-SC1-Siconi<sup>®</sup>" surface preparation with a Q-time <15 minutes and dichlorosilane injection during the temperature stabilization then the ramp-up.





**Figure 14:** O, Si and Ge EDX depth profiles after the epitaxial re-growth of 17 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  on top of 15 nm of  $\text{Si}_{0.60}\text{Ge}_{0.40}$  (itself on a SOI substrate) with, beforehand, a "HF/HCl-SC1-Siconi<sup>®</sup>" surface preparation with a Q-time <15 minutes and dichlorosilane injection during the temperature stabilization then the ramp-up. IL stands for interfacial (or encapsulation) layer.

Thanks to haze, TEM, EDX and SIMS measurements, we have thus shown that Si encapsulation enabled us to suppress islanding during the  $\text{H}_2$  bake, yielding smooth SiGe/SiGe stacks free of defects.

### Conclusions:

In this study, we have shown the ability of "chemical oxide-Siconi<sup>®</sup>" sequences of removing SiGe native oxides. Such sequences yielded low thermal budget epitaxial regrowth without any delay and with an oxygen interfacial contamination 10 times lower than with standard "HF-last" wet cleanings (after a 2 minutes  $\text{H}_2$  bake at a temperature lower than or equal to  $650^\circ\text{C}$ ). Such sequences resulted in SiGe surfaces more sensitive to islanding, however. This was likely due to the formation of a few Ge-rich monolayers under the chemical  $\text{SiO}_2$  layers after dips in SC1 ( $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ ) or  $\text{O}_3$  solutions. To avoid islanding issues, a dichlorosilane-based passivation was performed during the low thermal budget  $\text{H}_2$  bake to generate a thin capping layer (less than 1nm) on SiGe. The resulting  $\text{Si}_{0.60}\text{Ge}_{0.40} / \text{Si} / \text{Si}_{0.60}\text{Ge}_{0.40}$  stacks were smooth and free of any significant amount of O interfacial contamination or extended defects.

Furthermore, we have shown that several types of wet cleaning can be used for the chemical oxidation for SiGe (followed by the removal of the chemical oxide in the Siconi<sup>®</sup> chamber). This might have a major importance on germanium rich SiGe alloys (i.e. with a Ge content above 40%). Indeed, SiGe etch rates in SC1 and Hot SC1 solutions are, for high Ge contents, definitely higher than etch rates in ozone. The use of "ozone-Siconi<sup>®</sup>" sequences would then reduce SiGe layer consumption compared to "(Hot) SC1 / Siconi<sup>®</sup>) sequences. All this knowledge on SiGe oxide removal will be of use for the integration of SiGe in advanced devices.

### Acknowledgments

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## References:

- [1] O. Weber, E. Josse and M. Haond, « (Invited) 14nm FDSOI Technology for High-Speed and Energy-Efficient CMOS », *ECS Trans.*, vol. 66, n° 5, pp. 37-42, 2015.
- [2] G. Höck, E. Kohn, C. Rosenblad, H. von Känel, H.-J. Herzog and U. König, « High hole mobility in Si<sub>0.17</sub>Ge<sub>0.83</sub> channel metal–oxide–semiconductor field-effect transistors grown by plasma-enhanced chemical vapor deposition », *Appl. Phys. Lett.*, vol. 76, pp. 3920-3922, 2000.
- [3] Y. J. Chabal, G. S. Higashi, K. Raghavachari and V. A. Burrows, « Infrared spectroscopy of Si(111) and Si(100) surfaces after HF treatment: Hydrogen termination and surface morphology », *J. Vac. Sci. Technol. A*, vol. 7, pp. 2104-2109, 1989.
- [4] X. Zhang, E. Garfunkel, Y. J. Chabal, S. B. Christman and E. E. Chaban, « Stability of HF-etched Si(100) surfaces in oxygen ambient », *Appl. Phys. Lett.*, vol. 79, pp. 4051-4053, 2001.
- [5] S. Rivillon, Y. J. Chabal, F. Amy and A. Kahn, « Hydrogen passivation of germanium (100) surface using wet chemical preparation », *Appl. Phys. Lett.*, vol. 87, pp. 253101, 2005.
- [6] M. Labrot, F. Cheynis, D. Barge, P. Müller and M. Juhel, « Low thermal budget for Si and SiGe surface preparation for FD-SOI technology », *Appl. Surf. Sci.*, vol. 371, pp. 436-446, 2016.
- [7] A. Abbadie, J. M. Hartmann, P. Holliger, M. N. Séméria, P. Besson and P. Gentile, « Low thermal budget surface preparation of Si and SiGe », *Appl. Surf. Sci.*, vol. 225, pp. 256-266, 2004.
- [8] P. E. Raynal *et al.*, « Wet and Siconi® cleaning sequences for SiGe p-type metal oxide semiconductor channels », *Microelectron. Eng.*, vol. 187-188, pp. 84-89, 2018.
- [9] *Handbook of electrochemistry*, vol. Microelectrode array. 2007.
- [10] I. Ban, M. Kristl, M. Drogenik and A. Popovič, « Hydroxylammonium fluorogermanates », *Thermochim. Acta*, vol. 419, pp. 253-257, 2004.
- [11] T. O. Sedgwick, P. D. Agnello and D. A. Grützmacher, « Effects of Trace Surface Oxidation in Low Temperature Epitaxy Grown from Dichlorosilane », *J. Electrochem. Soc.*, vol. 140, pp. 3684-3688, 1993.
- [12] P. D. Agnello et T. O. Sedgwick, « Inhibition of Silicon Oxidation during Low Temperature Epitaxial Growth », *J. Electrochem. Soc.*, vol. 139, pp. 1140-1146, 1992.
- [13] M. R. Goulding, « The selective epitaxial growth of silicon », *Mater. Sci. Eng. B*, vol. 17, pp. 47-67, 1993.
- [14] A. Dkhissi *et al.*, « Evidence of the Ge nonreactivity during the initial stage of SiGe oxidation », *Appl. Phys. Lett.*, vol. 94, 041912, 2009.
- [15] Y. B. Kim, M. Tuominen, I. Raaijmakers, R. de Blank, R. Wilhelm and S. Haukka, « Initial Stage of the Ultrathin Oxide Growth in Water Vapor on Si ( 100 ) Surface », *Electrochem. Solid-State Lett.*, vol. 3, pp. 346-349, 2000.
- [16] M. Labrot *et al.*, « Improvement of etching and cleaning methods for integration of raised source and drain in FD-SOI technologies », *Microelectron. Eng.*, vol. 180, pp. 56-64, 2017.
- [17] H. Chen, Y. K. Li, et al. "Crosshatching on a SiGe film grown on a Si(001) substrate studied by Raman mapping and atomic force microscopy", *Physical Review B*, vol. 65, pp. 2333031-2333034, 2002.
- [18] J. M. Hartmann, A. Abbadie and S. Favier, « Critical thickness for plastic relaxation of SiGe on Si(001) revisited », *J. Appl. Phys.*, vol. 110, n° 8, p. 083529, 2011.
- [19] J.M. Hartmann, A. Abbadie, N. Cherkashin, H. Grampeix and L. Clavelier, "Epitaxial growth of Ge thick layers on nominal and 6° off Si(0 0 1); Ge surface passivation by Si", *Semicond. Sci. Technol.* 24, 055002, 2009.
- [20] B. Gallas *et al.*, « Influence of misfit and threading dislocations on the surface morphology of SiGe graded-layers », *J. Cryst. Growth*, vol. 201-202, pp. 547-550, 1999.
- [21] J. M. Hartmann, Y. Bogumilowicz, A. Abbadie, F. Fillot and T. Billon, « Impact of the H<sub>2</sub> bake temperature on the structural properties of tensily strained Si layers on SiGe », *J. Cryst. Growth*, vol. 310, pp. 2493-2502, 2008.
- [22] E. A. Stach *et al.*, « Effect of the surface upon misfit dislocation velocities during the growth and annealing of SiGe/Si (001) heterostructures », *J. Appl. Phys.*, vol. 83, pp. 1931-1937, 1998.
- [23] M. Katsuhido, T. Kishimoto and A. Izumi, « Non-IPA wafer drying technology for single-spin wet cleaning », *Electrochemical Society Proceeding*, vol. 26 pp. 57-63, 2003.

- [24] K. Miya, T. Kishimoto and A. Izumi, "Effective Rinse Aiming at Water-Mark-Free Drying for Single-Spin Wet Cleaning Process", *Solid State Phenomena*, vol. 103-104, pp. 79–82, 2005.
- [25] J.M. Hartmann, F. Bertin, G. Rolland, M.N. Séméria and G. Bremond, "Effects of the temperature and of the amount of Ge on the morphology of Ge islands grown by reduced pressure–chemical vapor deposition", *Thin Solid Films*, vol. 479, p. 113, 2005.
- [26] L. Masarotto, J.M. Hartmann, G. Bremond, G. Rolland, A.M. Papon and M.N. Séméria, "Reduced pressure–chemical vapor deposition of high Ge content Si/SiGe superlattices for 1.3 mm photo-detection", *Journal of Crystal Growth*, vol. 255, p. 8, 2003.
- [27] P. P. Zhang *et al.*, « Influence of germanium on thermal dewetting and agglomeration of the silicon template layer in thin silicon-on-insulator », *J. Physics D: Appl. Phys.*, vol. 42, p. 175309, 2009.
- [28] N. Sugiyama *et al.*, « Temperature effects on Ge condensation by thermal oxidation of SiGe-on-insulator structures », *J. Appl. Phys.*, vol. 95, pp. 4007-4011, 2004.
- [29] F. K. LeGoues, R. Rosenberg, T. Nguyen, F. Himpsel and B. S. Meyerson, « Oxidation studies of SiGe », *J. Appl. Phys.*, vol. 65, pp. 1724-1728, 1989.
- [30] J.M. Hartmann, V. Benevent, J.F. Damlencourt and T. Billon, "A benchmarking of silane, disilane and dichlorosilane for the low temperature growth of group IV layers", *Thin Solid Films*, vol. 520, p. 3185, 2012.
- [31] Y. Bogumilowicz, J.M. Hartmann, N. Cherkashin, A. Claverie, G. Rolland and T. Billon, "SiGe virtual substrates growth up to 50% Ge concentration for Si/Ge dual channel epitaxy", *Materials Science and Engineering B*, vol. 124–125, p. 113, 2005.
- [32] A. Abbadie, J.M. Hartmann, C. Di Nardo, T. Billon, Y. Campidelli and P. Besson, "An efficient wet-cleaning of SiGe virtual substrates and of thick, pure Ge layers on Si(001) after a chemical mechanical planarization step", *Microelectronic Engineering*, vol. 83, p. 1986, 2006.