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A chopper negative-R Delta-Sigma ADC for audio MEMS sensors

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Abstract: This paper presents a proposed low-noise and high-sensitivity Internet of Thing (IoT) system based on an M&NEMS microphone. The IoT device consists of an M&NEMS resistive accelerometer associated with an electronic readout circuit, which is a silicon nanowire and a Continuous-Time (CT) ΔΣ ADC. The first integrator of the ΔΣ ADC is based on a positive feedback DC-gain enhancement two-stage amplifier due to its high linearity and low-noise operations. To mitigate both the offset and 1/*f* noise, a suggested delay-time chopper negative-R stabilization technique is applied around the first integrator. A 65-nm CMOS process implements the CT ΔΣ ADC. The supply voltage of the CMOS circuit is 1.2-V while 0.96-mW is the power consumption and 0.1-mm^2 is the silicon area. The M&NEMS microphone and ΔΣ ADC complete circuit are fabricated and measured. Over a working frequency bandwidth of 20-kHz, the measurement results of the proposed IoT system reach a signal to noise ratio (SNR) of 102.8-dB. Moreover, it has a measured dynamic range (DR) of 108-dB and a measured signal to noise and distortion ratio (SNDR) of 101.3-dB.

Keywords: M&NEMS sensor; ΔΣ ADC; chopper negative-R; IoT; 1/*f* noise; SNR.

1. Introduction

In recent years, a new system called the Internet of Things (IoT) has increasingly gained ground. IoT depicts a large network of interconnected sensors and objects that are uniquely addressable, built on common networking protocols, the subject of which is the Internet. The IoT system is focused on the pervasive existence of objects surrounding individuals capable of weighing, deducting, recognizing, and even altering their environment. It is based on intelligent and interconnected nodes within a complex and extensive network infrastructure [1]. It is typically defined by small real-world objects, widely dispersed, with minimal storage and processing power, suggesting reliability, efficiency, protection, and privacy issues. It is driven by recent developments in different devices and technologies for communication. This refers to complicated devices like cell phones and basic items like clocks, thermostats, clothing, etc, that are used every day [2]. These objects can connect and interact with their neighborhood, operating as sensors or actuators. Wireless Sensor Networks (WSNs) are self-configured, infrastructure-free wireless networks that monitor physical or environmental conditions such as sound, temperature, vibration, motion, pressure, or pollutants and cooperatively pass their data through the network to a central location or sink where the data can be observed and analyzed. A wireless sensor network typically consists of hundreds of thousands of sensor nodes [3]. Radio signals allow the sensor nodes to communicate with one another. Sensing and computing devices, radio transceivers, and power components are all included in a wireless sensor node [4]. Sensors and actuators are the key building blocks of the IoT system. They monitor the state of their environment; obtain information on temperature, movement, position, etc. They form a network usually

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composed of a potentially large number of nodes. These sensors have to face many communication problems such as security and confidentiality, mobility, short-range, reliability, robustness, scalability, and resources.

Micro-Electro-Mechanical Systems (MEMS) circuits integrate sensors, mechanical elements, actuators, and electronic circuits in the same silicon substrate. Nowadays, there is an immensely high demand for the MEMS market. Therefore, audio applications commonly use MEMS microphones owing to their fundamental requirements, which consist of small size, low-power consumption, high sound quality, high sensitivity, and reliability. For the MEMS microphone, the main goal of the design and optimization of its electronic circuits is to improve the audio performances. Among these audio performances, it is necessary to increase the signal-to-noise ratio (SNR), the total harmonic distortion (THD), the dynamic range (DR), and the low-power consumption. Based on their output, two categories of MEMS microphones exist namely the analog MEMS microphone and the digital MEMS microphone. The CMOS chip of the digital MEMS microphone integrates an Analog to Digital Converter (ADC) in the objective to generate a digital output. As a result, the complete circuit is easily integrated with modern digital systems. Due to its high resolution, inherent linearity, and wide dynamic range; the audio application uses Delta-Sigma (ΔΣ) ADC [5]. The ΔΣ ADC sampling frequency is very high compared to the Nyquist rate being an oversampled converter. Due to their high resolution, applications working in the low to medium bandwidth extensively use ΔΣ ADCs [6], such as MEMS microphone [7], audio systems [8], sensing applications [9] and wireless communications [10]. Recent trends in the mobile microphone market are targeting 70 dB A-weighted signal-to-noise ratio (SNR) at 94dB sound pressure level (SPL) and higher acoustic overload points. In the readout circuit of microphones, an ADC having a dynamic range (DR) far above 100dB A-weighted can meet this condition. In addition, a high value of signal-to-noise and distortion ratio (SNDR) is also preferred so as to preserve the fidelity of acoustic signal source at high sound pressure levels above 94dB SPL. However, to reduce the power consumption of digital circuits including application processor in mobile devices, the supply voltage is getting lower, and thus interface circuits such as the ADC having high DR and SNR should also be designed to operate at a low supply voltage.

Audio systems have traditionally using multibit ΔΣ ADC often based on a switched capacitor circuit [11]. Continuous-time (CT) solutions, on the other hand, are becoming extremely prevalent for low bandwidth ADC applications. ADC is commonly used for audio applications because of its high SNR, reduced power consumption, and high resolution [12]. In the last decade, deep-submicron CMOS technology has become a solution for continuous scaling, low cost, and low power devices. The bias voltage, however, becomes very low, under one-Volt, reducing the signal swing as low as analog circuit supply voltage limits (i.e. CT filters). The ADC depicts a very important interface separating the analog and the digital circuit. When designing a CMOS system, the ADC circuit and the CMOS digital circuit are implemented with the same CMOS process. Therefore, the reduction of the ADC's power consumption is inevitable. The main goal is to decrease the ADC's supply voltage. However, the drawback of this technique is the degradation of ADC performance. If the signal swing of the system is decreased, its noise floor must be decreased to keep the same circuit dynamic range. Therefore, reducing the supply voltage for high-resolution audio systems leads to a serious distortion problem.

High performance and high-resolution audio systems are based on a ΔΣ ADC owing to its high linearity [12]. This characteristic is obtained by integrating the oversampling technique with the inherent single-bit linear quantizer. Non-idealities of building blocks, however, strongly influence its efficiency. If a nanometer CMOS technique is used, the performance seems even worse. The restriction of their headroom function induced by the reduction of the bias voltage affects the working devices [13]. Moreover, the figure-of-merit (FOM) of the implemented circuit is affected. Furthermore, the ΔΣ ADC designed with this technology needs a low SNR and low-noise floor with the same dynamic range. The output is then impacted and the energy consumption is increased [14]. The most critical parameter for designing a ΔΣ ADC with high resolution is to increasing its linearity.

The goal of this paper is to implement an IoT device consisting of an M&NEMS microphone and an ADC that has a high peak-SNR, high peak SNDR, and high Schreier's FOM. The CMOS architecture of a

ΔΣ ADC is particularly chosen. Besides, proposed electronic circuits to improve performances are designed and discussed. We have adopted the Low-Energy Adaptive Clustering Hierarchy (LEACH) as the communication protocol of the data transmission among sensor nodes. LEACH includes randomized rotation of the high-energy cluster-head position such that it rotates among the various sensors in order to not drain the battery of a single sensor. LEACH performs local data fusion to "compress" the amount of data being sent from the clusters to the base station, further reducing energy dissipation and enhancing system lifetime. The whole IoT device is designed and manufactured in a 65-nm CMOS process. Measurement results are analyzed and compared with the state-of-the-art. The paper sections are arranged as follows; a description of the manufactured M&NEMS microphone is presented in Section 2. Section 3 gives the specifics of the ΔΣ ADC implementation. Section 4 explains the suggested chopper negative-R solution for reducing the first integrator's flicker noise. The measurement results and analysis of the proposed IoT system are described in section 5. Finally, Section 6 becomes to conclude our proposed IoT system.

2. MEMS microphone design

[t1]To detect acoustic vibrations, nanowire microphones use piezo-resistivity. They reflect the latest generation and the newest technology of the M&NEMS piezoresistive sensors that have already been developed in the CEA-Leti. The strength of this proposed M&NEMS piezoresistive sensor is that silicon-based nanowires are used to produce an electrical output response [15]. The silicon nanowire microphone combines an integrated mechanical system of components in movement, like other M&NEMS sensors. To generate a high nanowires mechanical stress, the architecture of this mechanical component is carefully established. The development of the M&NEMS resistive sensor is carried out in the cleanroom of the CEA-Leti, as defined in Fig. 1. Two stacked wafers are part of the microphone, as shown in Fig. 2. The wafer on the top has vents for outlets. These events represent acoustic guides through which the incident acoustic wave circulates. The bottom wafer contains electrical input-output contacts, microstructures that bring silicon nanowires under tension-compression, and inlet vents for access to the nanowire resistors. The proposed M&NEMS piezoresistive sensor depicts an invention done by CEA-Leti [16]. A diaphragm located between the top wafer and the bottom wafer represents the M&NEMS microphone. For M&NEMS implementation, the top and the bottom wafer are used, respectively, as a cap and a base. To achieve effective sound pressure amplification and a good static pressure's equalization, the acoustic sound vents and the two wafers will be etched. The microphone acts as follows; when a disturbance appears, the actuation of the pressure spread through the acoustic inlet vents in the bottom wafer and moves to the diaphragm. The actuation of the pressure then varies in proportion to the differential pressure in the top wafer between the inlet and outlet vents. It is conceivable to multiply the inlet vents, the outlet vents, and the diaphragms to build an efficient M&NEMS piezoresistive sensor.

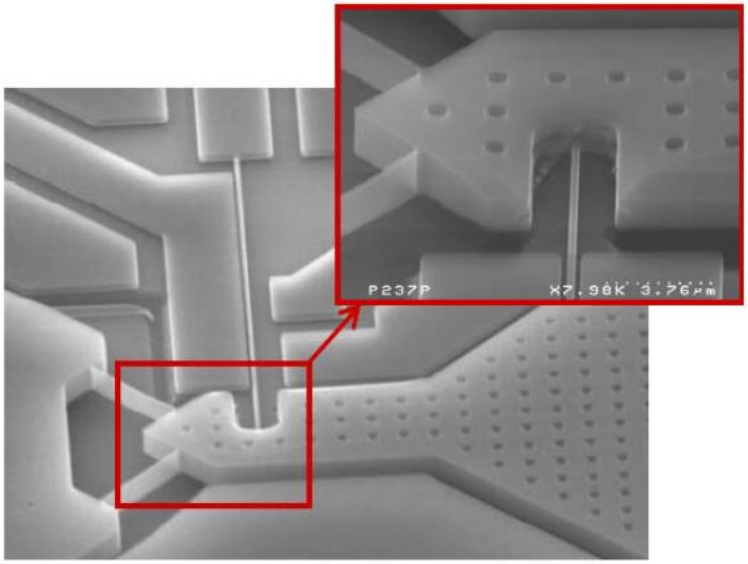
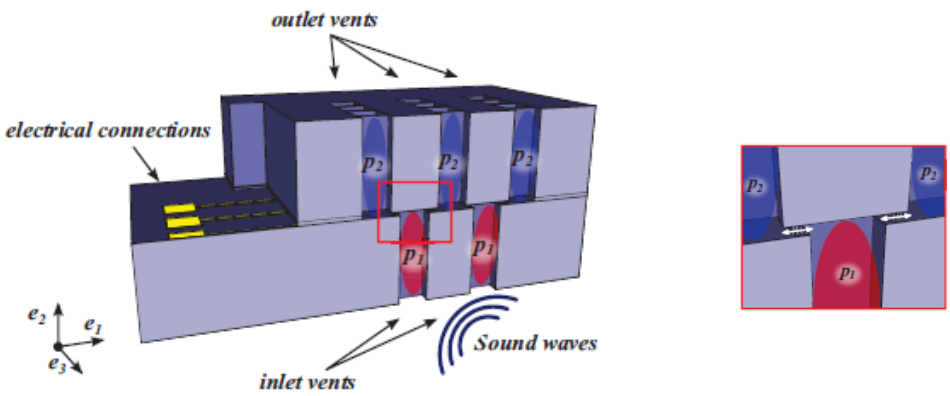


Figure 1: SEM photograph of the M&NEM based nanowire sensor.



(a) (b)

Figure 2: Cross-section of the M&NEMS microphone. (a) Sensing elements and acoustic configuration. (b) Nanowire position is indicated by the white arrows and in-plane microstructures displacement.

A sound wave pressure attacks the inlet vents. The piezoresistive effect causes the silicon nanowire resistance to be varied according to the applied stress. A piezoresistive phenomenon is present in the doped crystalline silicon. Consequently, in M&NEMS sensors, this phenomenon is widely used as a detection process. The implementation of piezoresistors into silicon membranes enables the microphone to detect the overall sound pressure by generating a piezoresistive effect. By the selective deposition technique of the doped silicon substrate, piezo resistors may be embedded into silicon membranes. Besides, the selective doping approach of the silicon membrane may be implemented in the fabrication or diffusion process [17]. Therefore, since the detected stress is spread over the complete surface of the membrane, the optimization of the M&NEMS sensor reflects to optimize the stress of the internal piezo resistors. Piezo resistors must be mounted in regions of the highest stress [18]. Furthermore, the thickness of the microphone membrane and the thickness of the piezoresistor must have a significant proportion [19]. Consequently, in the center

of the membrane side, maximum tensional longitudinal stress appears. Moreover, in the center of the M&NEMS sensor membrane, there is another maximum compressional stress.

If acceleration is sensed, then a rotational movement acts automatically on the seismic mass. By respecting the rotational axis, this rotational movement is achieved. The resulting inertial force is then used to create longitudinal or tension stress in the nanogage section. The nanogauge stress makes the creation of a resistance change proportional to the inertial force due to the piezoresistive effect. A lever effect factor amplifies the resistance difference. The lever effect is the resulting distance separating the axis of rotation and the seismic mass center, divided by the resulting distance separating the rotation axis and the nanogauge position. In addition, by having trenches and a boss, the special membrane features will create stress concentration regions [20]. A p-n junction between the interfaces of membrane-piezoresistors is then formed when the piezoresistors are embedded into the membrane. This junction produces a current for leakage. The piezoresistor bias current is higher at room temperature than the leakage current, which can be ignored. The leakage current also increases if the temperature increases, and it can affect the sensor response [21].

The architecture of the suspended nanowires is adopted to design the M&NEMS resistive accelerometer. The p-type piezoresistive effect of silicon nanowires was studied [22]. Compared to bulk silicon, the piezoresistive effect greatly improves at the nanoscale. Hence, for more robust MEMS sensors, silicon nanowires are very effective. 1.5 x 1.5 x 0.6 mm^3 is the average size of the M&NEMS piezoresistive sensor. Four microbeams depict the M&NEMS sensor. They are mounted between the inlet and outlet vents. The M&NEMS microbeam shifts rotationally according to the applied stress.

The proposed concept uses a membrane able to move in the plane of the substrate and not out of plane. The first advantage of the proposed concept is the decorrelation of the acoustic part and the detection part, which enables to optimize them independently. The second advantage is the same fabrication process for both microphones and accelerometers, which enables either to co-integrate these two sensors on the same chip or to use the same technological platform for these two components. The MEMS fabrication is carried out at CEA-LETI clean room with typical micro-electronic process. MEMS microphone exhibits 30 dB of Equivalent Input Noise (EIN) with a resolution of 95 nV/bits. Analytical calculation shows that 74 dB SNR (Signal to Noise Ratio) could be achieved with biasing current of 100 μA and readout circuit featuring 6 nV/√Hz input referred noise.

3. Implementation of the ΔΣ ADC circuit

Audio applications including hearing aids implant involve large dynamic range and low power consumption. Acoustic vibration lower than 30 dB SPL (Sound Pressure Level) must be resolved while sound pressure over 110 dB SPL must not generate harmonic distortion. Commercially available digital output MEMS microphones feature 30 dB SPL of equivalent input referred noise, power consumption lies in the mA range with supply voltage of 2.5 V. The proposed M&NEMS microphone targets input referred noise of 5 dB SPL lower than commonly used MEMS microphones. For high sensitivity of the microphone, the system was designed with a tradeoff between, noise performance, and power consumption where an optimal repartition of the current budget between the sensor bias and the analog front-end building blocks has to be achieved.

Two topologies are used to implement the ΔΣ ADC. The first one is the distributed feedforward topology. The second one is a distributed feedback topology. The signal in the output of the sensor is connected to the loop filter of the feedback topology. Therefore, large swings are introduced in the integrator by this input component. Therefore, the amplifier needs high linearity. This problem is very hard in low-voltage electronic architecture. The two-voltage components of the CMOS transistor, which are the threshold voltage and the drain to the source voltage, do not meet the same external bias voltage. On the other hand, a specific behavior is generated by feedforward topology [23]. In this topology, the shaped quantization noise depicts the only available noise component in the loop filter input. The direct feeding of the integrator's outputs and the input signal to the quantizer allows achieving this main advantage. Moreover, the quantizer output is connected to the input of the first integrator. Cascaded continuous time integrator

feed-forward sigma delta seems to be the best ADC topology to accomplish the involved trade off. First, continuous time integrator provides intrinsic anti-aliasing filtering saving filter stage power consumption; second, feed-forward implementation reduces integrators output swing requirement making amplifier design easier; third, unlike switched capacitor integrator, amplifier settling time requirement is relaxed, so as the saved power budget can be allocated to input stage in favor of noise performance.

The voltage fluctuations into the integrators are widely mitigated if there is no signal coming from the sensor. Therefore, both the linearity and the slew rate of the amplifier are improved, while a reduction of its current consumption. Thus, the feedforward topology is a suitable solution to mitigate both the ADC power consumption and noise. The ADC for quantization uses a single-bit quantizer because any complex element matching circuit does not require by the DAC and the ADC circuit is inherently linear. Moreover, owing to the configuration of only two DACs and one comparator without a calibration circuit, the total power consumption and the overall silicon area of the DAC and digital circuit are much lower than the multibit quantizer [24]. On the other hand, the noise specification for quantization requires the oversampling ratio and the ΔΣ ADC order to be defined. To minimize the amplifier's power consumption, the ΔΣ ADC's thermal noise must be widely mitigated.

Audio applications have a relatively small bandwidth (B from 20-Hz to 20-kHz). As a result, ΔΣ ADC is particularly suited for this bandwidth. The ΔΣ ADC solution can achieve a large oversampling ratio $M = \frac{f_S}{(2B)}$ with a sampling frequency f_S of 3.072-MHz. Moreover, it can achieve high SNR values with a small area and simple hardware architecture by reducing noise and trading accuracy with speed and power consumption. If the ΔΣ ADC has an oversampling ratio M and order of L with N-bit quantizer, then the SNR can be written as [25]

$$SNR = \frac{3}{2}\frac{2^{2N}(2L+1)}{\pi^{2L}}M^{2L+1}, \tag{1}$$

where M, N, and L values can be chosen to achieve the target high SNR value. The ΔΣ ADC is simpler if it has an order of two with N = 1 [26]. However, in this case, M values should be high, which requires the integrators opamps with high slew-rate and high gain bandwidth. Therefore, the ΔΣ ADC is affected by high power consumption. Although, if the ΔΣ ADC has the fourth-order filtering with N = 1, then the requirements for each integrator will be more relaxed. The non-dominant quantization noise can be set by 10-dB under the overall ΔΣ ADC noise. The fourth-order integrator topology is chosen for the order of the ΔΣ ADC, as well as the oversampling M of 77 is set. The ADC has a 3.072-MHz sampling frequency and a 20-kHz signal bandwidth. The ADC coefficients are a_i for the integrator coefficient, k_i for the feedforward coefficient, and V_{oi} for the output of the integrator, with i = 1 ... 4, as shown in Fig. 3 [27]. They are derived from the ΔΣ ADC presented in [28]. In the objective of achieving high SNR with good loop stability, a behavioral simulation is used to optimize these coefficients.

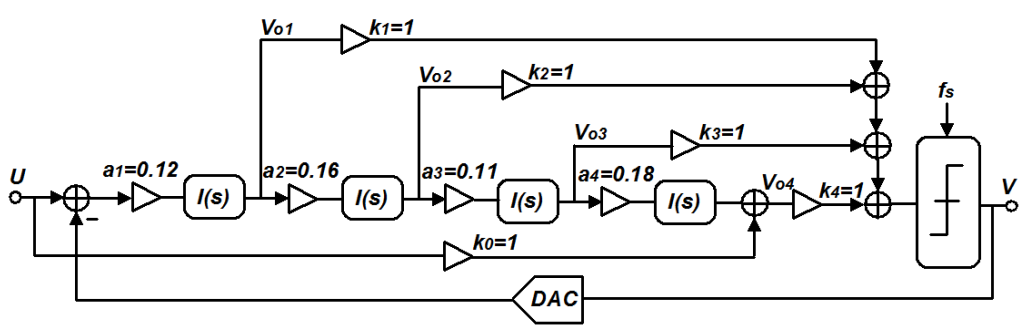
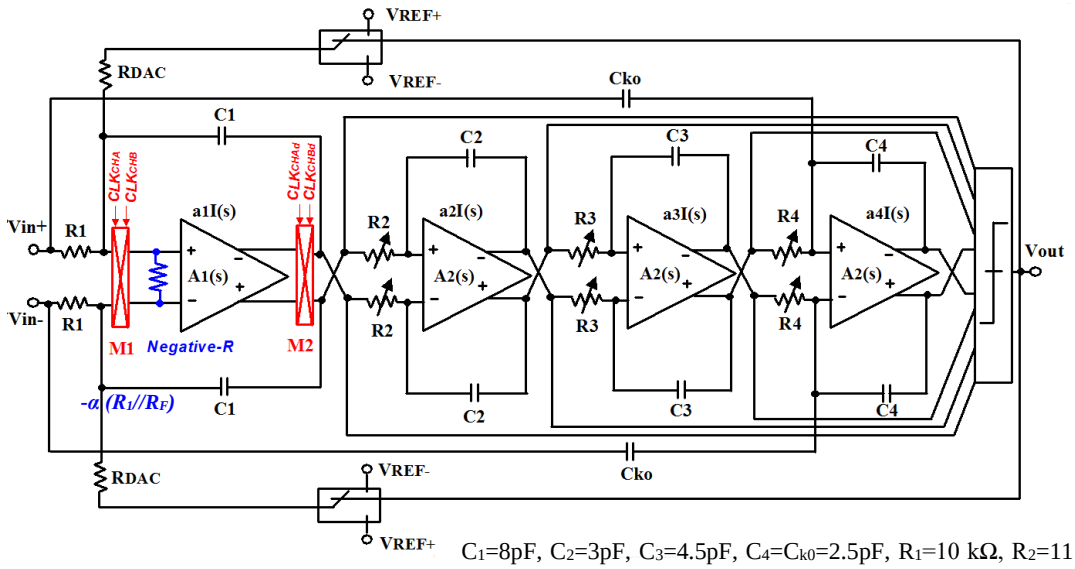


Figure 3: Circuit diagram of the CT ΔΣ ADC with the integrator coefficient ai, the feedforward coefficient for ki, and the output of the integrator Voi.

In this design, the DAC placed in the feedback is based on a non-return-to-zero (NRZ) pulse. Compared with the architecture of a return-to-zero (RZ) pulse and a half-delayed return-to-zero (HRZ) pulse, clock jitter does not affect the sensitivity of the NRZ pulse [29]. The input pulse is constant over the complete clock cycle. Therefore, the NRZ DAC pulse relaxes the first integrator slew rate. Moreover, the first integrator has low power consumption. Fig. 4 describes the complete circuit of the ΔΣ ADC. Each integrator is based on a closed-loop active-RC filter architecture. This architecture allows increasing the linearity and parasitic insensitivity of the integrator. The virtual ground of the active-RC filter maintains the amplifier input range requirement is relaxed. Therefore, when working at a low voltage level, the closed-loop active-RC filter is appropriate.

The SNR of the ΔΣ ADC is affected by the excess loop delay. From simulations, the excess loop delay must be limited to a maximum of 15% of the clock period to have a high SNR exceeding 90-dB. Therefore, the simulated loop delay time is around 54-ns. As a result, the single-bit quantizer easily satisfies this excess loop delay under the 65-nm CMOS process. To design a low-voltage ΔΣ ADC, the amplifier's gain-bandwidth and finite gain have important roles. The low supply voltage limits the amplifier gain while the amplifier power consumption is determined by its gain bandwidth. From simulation results, the CT input-feedforward topology is well suitable for the finite gain amplifier. Moreover, it is well suitable for the amplifier gain-bandwidth requirements. The designed amplifier must then have a DC-gain greater than 40-dB. It must have also a product gain-bandwidth greater than the sampling frequency to reach an SNR greater than 90-dB. The first integrator is the ΔΣ ADC key responsibility. Because of the input stage's non-idealities, the loop filter does not shape. It therefore directly affects the ΔΣ ADC system's performance. In addition, the first integrator specifies the linearity and the total noise of the ΔΣ ADC. Designing an amplifier with a high DC gain of about 80-dB and a high unity gain-bandwidth of about 8-MHz is the expected simulation of the first integrator to achieve a high SNR.



C_1=8pF, C_2=3pF, C_3=4.5pF, C_4=C_{k0}=2.5pF, R_1=10 kΩ, R_2=11 kΩ, R_3=28 kΩ, R_4=26 kΩ, R_{DAC}=4 kΩ.

Figure 4: Circuit of the proposed CT ΔΣ ADC.

3.1. Amplifier circuit of the first integrator

The amplifier of the first integrator is based on two stages architecture, as described in Fig. 5 [30]. The two stages architecture are respectively a folded cascode and a common source amplifier. The hybrid-cascode compensation approach is used to achieve precise and simple relationships of poles and zero in the objective to increase the amplifier's frequency response [31]. Amplifier (M15, M17), (M16, M18), (M19,

M21), and (M20, M22) transistor pairs are split [32]. Two current mirrors are used in the amplifier. The first mirror is composed of transistor set (M15, M17, M19, M21) and the second mirror is composed of transistor set (M16, M18, M20, M22). The proposed idea consists of creating a positive feedback loop between the two outputs V_{out+} and V_{out-} of the amplifier to increase the amplifier DC gain with the same UGBW value [30]. In this context, the terminal V_{out+} is assigned to the transistor drain M16 and the terminal V_{out-} is assigned to the transistor drain M15.

At the output V_{out+}, the small-signal analysis of the current mirror is performed. The equivalent output resistance R_{CS} can be expressed as

$$R_{CS} = \frac{1}{X + Y - Z}, \tag{2}$$

with $X = g_{m21}/(1 + g_{m21}R_{19})$, $Y = 1/(g_{m16}r_{ds16}R_{18} + r_{ds16} + R_{18})$ and $Z = g_{m16}/(1 + g_{m16}R_{18})$. The g_{m16} and g_{m21} are the transconductances of transistors M16 and M21; R_{18} and R_{19} are the resistance of the channel transistors M18 and M19 working in the triode region. Thus, the amplifier DC-gain can be written as

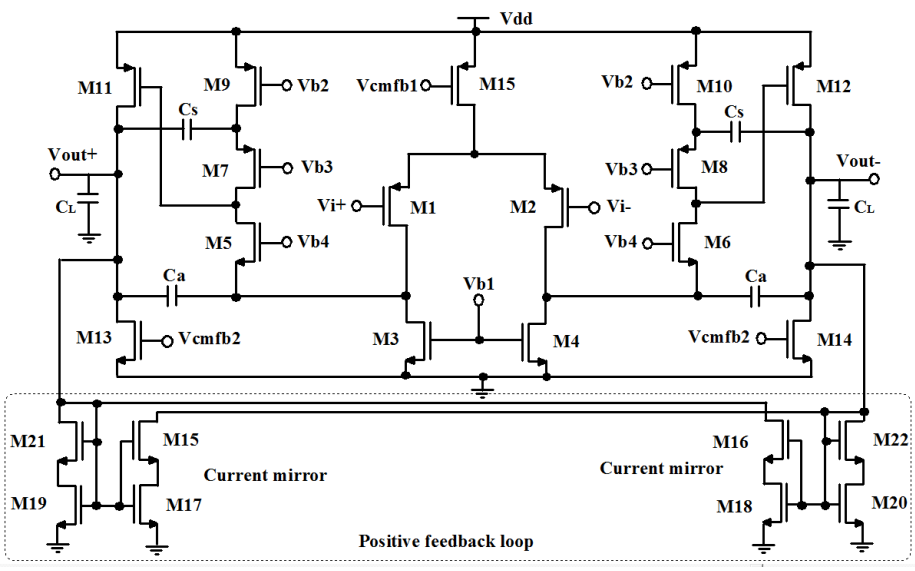


Figure 5: Proposed positive feedback two-stage amplifier for the first integrator.

$$A_d = g_{m1a}R_{out1}g_{m11a}R_{out2}, \tag{3}$$

$$R_{out1} = g_{m7a}r_{ds7a}r_{ds9a} \| [g_{m5a}r_{ds5a}(r_{ds1a} \| r_{ds3a})], \tag{4}$$

$$R_{out2} = \frac{1}{g_{ds11a} + g_{ds13a} + G_{CS}}, \tag{5}$$

where g_m denotes the transconductance of transistors, R_{out1} denotes the first stage equivalent output resistance and R_{out2} denotes the second stage output resistance, r_{ds} depicts the drain-source resistor, $G_{CS} = 1/R_{CS}$, and $g_{ds} = 1/r_{ds}$. If the denominator of Eq. (5) is chosen near-zero with $g_{ds11} + g_{ds13} + G_{CS} > 0$, then the differential voltage gain A_d can be drastically increased. After the common-mode gain analysis is done, the output resistance R'_{CS} analysis of the current mirror is performed, which can be written as

$$R'_{CS} = \frac{1}{X + Y + Z}, \tag{6}$$

The equivalent output resistance R'_{out2} of the second stage can be defined as

$$R'_{out2} = \frac{1}{g_{ds11a} + g_{ds13a} + G'_{CS}}, \tag{7}$$

where $G'_{CS} = 1/R'_{CS}$. From Eq. (5) and Eq. (7), it is clear that R'_{out2} is fewer thanR_{out2}. This component is therefore very successful in reducing the A_{CM} common-mode gain, which can be defined as

$$A_{CM} = \frac{g_{m1a}R_{out1}}{1 + 2g_{m1a}r_{ds15a}} g_{m11a}R'_{out2}. \tag{8}$$

The signal on the output nodes is impacted by a slight change in the power supply voltage. Therefore, a simulation of the power-supply rejection ratio (PSRR) is performed to measure this degradation. The PSRR analysis is also used to simulate the amplifier capacity to reject its input power supply ripples at different frequencies. The equation of the PSRR can be defined as

$$PSRR = \frac{-A_d}{\left(\frac{g_{m15a}}{2} + g_{m9a}\right) R_{out1} g_{m11a} R'_{out2}}. \tag{9}$$

From Eq. (9), if the differential-mode A_d increase and the second stage output resistance R'_{out2} decrease, then the PSRR of the amplifier increase.

A small shift in the g_m transconductance of the negative resistance generating components directly affect the opamp DC gain [33]. In addition, there would be a significant difference in the DC gain of the opamp. However, the use of a tail resistor is a fascinating approach to alleviating this problem. For further clarification, if ($\Delta g_m/g_m$) denotes a slight offset of the g_m component without the tail resistor, then the new offset value of the same g_m component with the tail resistor can be written as

$$\frac{\Delta g_{m,new}}{g_m} = \frac{\left(\frac{(g_m + \Delta g_m)}{1 + (g_m + \Delta g_m)R}\right) - \left(\frac{g_m}{1 + g_m R}\right)}{\left(\frac{g_m}{1 + g_m R}\right)} = \frac{1}{1 + (g_m + \Delta g_m)R} \times \frac{\Delta g_m}{g_m}. \tag{10}$$

It is evident from Eq. (10) that the tail resistor allows decreasing the offset of the g_m component by a factor of $1/[1 + (g_m + \Delta g_m)R]$. In addition, a negative resistance is generated at the output terminal of the second stage amplifier due to the proposed split-length transistor. The series of transistors (M17, M18, M19, M20) is located in the triode zone. Therefore, the equivalent channel resistance of the transistors creates an integrated tail resistor. As a result, the proposed split-length transistor technique decreases the sensitivity to process variation.

Regarding the second to the fourth integrators, the noise-shaping effect allows suppressing their non-idealities. As a result, the requirements of the amplifiers are relaxed. The core of the second to the fourth active-RC integrator is based on a two-stage amplifier with a common-mode feedback (CMFB) circuit as shown in Fig. 6 [34]. Compensation capacitors (C_C) guarantee the stabilization of the two-stage OTA. The key feature of this topology is the simultaneous separation of the specifications of gain and output swing [35]. To guarantee these specifications, the level of the CMFB output must be fixed to half of the supply voltage.

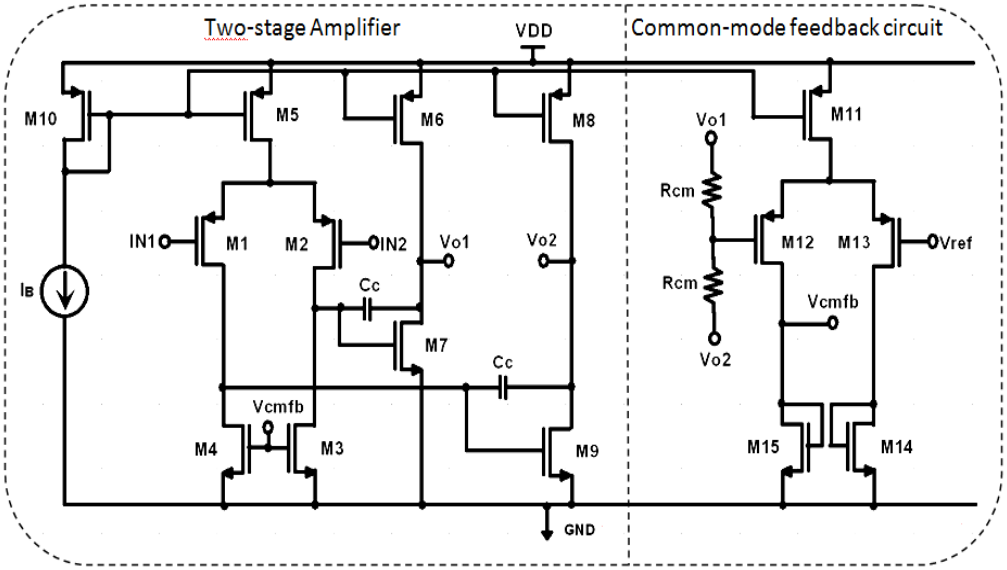


Figure 6: Amplifier circuit with the CMFB for the second to the fourth integrator.

3.2. Quantizer circuit

The ΔΣ ADC feedforward coefficients are based on two structures namely the area-efficient structure and the power-efficient structure [36]. The comparator integrates both the feedforward coefficients summation and the feedforward paths combination. The comparator with its inputs is shown in Fig. 7. In the design, the outputs of the integrators are connected to the comparator inputs. Input comparator transistors (M1A, M2A, M3A, M4A) have the same width W and the same length L, but the number of fingers is different. The comparator is cadenced by the clock *CLK1*. The comparator is reset if *CLK1* is at GND. Therefore, the two nodes of the quantizer *X* and *Y* are connected to the GND, while the two outputs V_{co+} and V_{co-} of the comparator are driven to the V_{DD}. On the other hand, if *CLK1* is at V_{DD}, then there is the activation of the comparator. In this operation mode, transistors M1, M2, M3, and M4 work under linear region because of the low threshold voltage as well as the small outputs of the integrators. Therefore, the current through nodes *X* and *Y* can be written as

$$I_X = \sum_{i=1}^{4} I_i = \mu_n C_{OX} \sum_{i=1}^{4} \frac{W_i}{L}\left(V_{oi+} - V_{TH} - \frac{V_X}{2}\right) V_X,$$
$$I_Y = \sum_{i=1}^{4} I_{i+4} = \mu_n C_{OX} \sum_{i=1}^{4} \frac{W_i}{L}\left(V_{oi-} - V_{TH} - \frac{V_Y}{2}\right) V_Y, \quad (11)$$

where W_i denotes the width of transistor Mi and V_{TH} denotes the transistor threshold voltage. Nodes *X* and *Y* generate a current difference of

$$I_X - I_Y = \frac{\mu_n C_{OX} V_X}{L} \sum_{i=1}^{4} W_i V_{oi}, \quad (12)$$

where V_{oi} denotes the i_{th} integrator differential output, $V_{oi} = V_{oi+} - V_{oi-}$. At first, the comparator detects the current difference, and then its outputs V_{co+} and V_{co-} are amplified to high levels. Feedforward coefficients k_1, k_2, k_3 and k_4 can be realized according to the transistor-channel-width ratio as $W_1 = W_2 = W_3 = W_4 = k_1 = k_2 = k_3 = k_4 = 1$. We have realized a simulation of the comparator with input transistors acting in the linear

region. If the input signal has a -3-dBFS, then a level voltage of 0.07-V controls almost 99 % of the output signal of the integrator. As a result, the outputs of the integrator exceed 0.23-V, and they have a common-mode voltage of 0.3-V. The comparator input transistors work in the linear region because they have a 0.16-V threshold voltage.

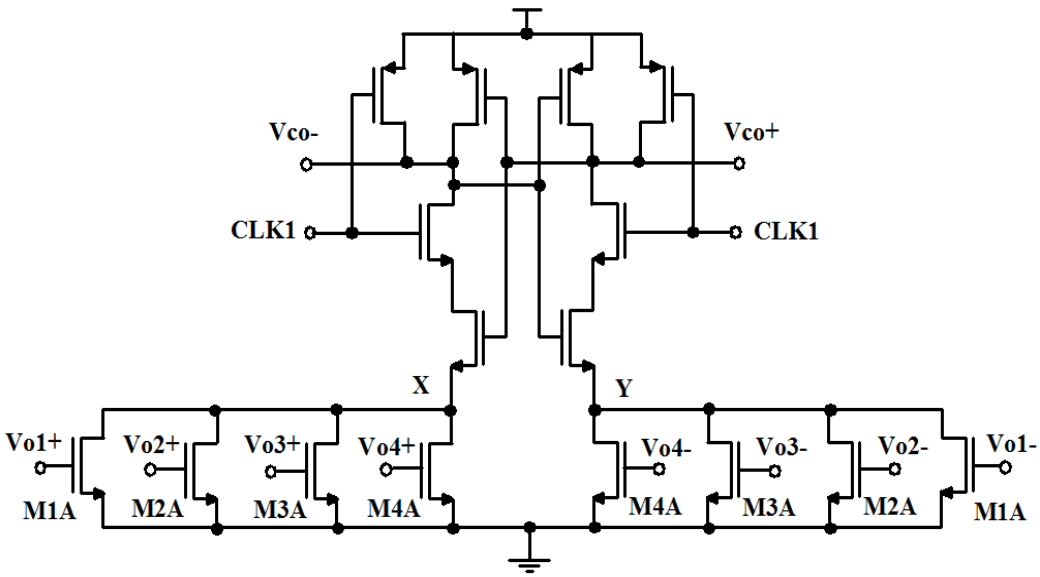


Figure 7: Circuit of the comparator with eight-input.

If the integrator output swings and the threshold voltage vary, then the input comparator transistors work out of the linear region. As a result, coefficient errors are generated by the comparator. Owing to the summation of the feedforward signals at the quantizer input, the noise-shaping effect ensures the suppression of the error in the feedforward coefficients k_1, k_2, k_3, and k_4. Therefore, the common-mode rejection ratio (CMRR) exceeds 120-dB. The deriving of the signal transfer function (STF) can be written according to the first input feedforward coefficient k_0 as

$$STF = \frac{V}{U} = \frac{k_0 + L(s)}{1 + L(s)}, \tag{13}$$

where $L(s)$ denotes the loop filter composed by the four-integrator coefficients a_1, a_2, a_3, and a_4, and by the four-feedforward coefficients k_1, k_2, k_3, and k_4. U and V depict respectively the ΔΣ ADC input and output. The function of the loop filter $L(s)$ based on the noise transfer function (NTF) can be written as [37]

$$L(s) = \frac{1}{NTF(s)} - 1. \tag{14}$$

Substituting Eq. (14) into Eq. (13), the STF can be written as

$$STF = \frac{V}{U} = NTF(s)[k_0 - 1] + 1. \tag{15}$$

From Eq. (15), the noise transfer function allows us to shape all deviation caused by the feedforward coefficient k_0 and hence to increase the CMRR of the comparator. To have a safe quantizer, the fourth integrator is implemented by the large input feedforward signal according to the capacitor ratio of C_{ko} to C_4. Therefore, one pair of transistors depict a feedforward coefficient with low-current consumption and low area. Furthermore, transistors M1, M2, M3, and M4 have a gate-source of maximum 80-fF.

3.3. RC time-constant tuning circuit

Integrated resistors and capacitors are affected by the process and temperature variations. Therefore, a large time-constant shift affects the CT ΔΣ ADC performance. The resistance and the capacitance variation are respectively ±20% and ±10% under the 65-nm CMOS process. To solve this problem, integrated resistances and capacitances must be tuning. If the resistances and the capacitances are tuned, then its absolute variation is controlled by about ±10%. The performance of the amplifier is stable when the integrated resistance and capacitance have a small variation. The solution adopted in this design is to use a technique of a four-bit digital signal tuning circuit as shown in Fig. 8. Moreover, the tunable resistors are controlled manually. The tuning circuit has a tuning range of [R, R+15*] and a tuning unit of R*. Due to distortions introduced by the nonlinearity of the switches, only the second, the third, and the fourth integrator use the technique of the tune resistors. Moreover, the suppression of non-idealities in these three integrators is realized. For a -3-dBFS input, we have studied and simulated the SNR performance of the ΔΣ ADC according to the RC variation on the system-level to estimate the ΔΣ ADC performance degradation. The simulation of the two worst cases is done by setting the first integrator coefficient a1 with respectively +30% and -30% variation. Moreover, the same percentage variation is assumed for coefficients a_2, a_3, and a_4. From simulation results, the designed tunable resistance guarantees a maximum of 10% variation of coefficients a_2, a_3, and a_4. As a result, the stability of the ΔΣ ADC is guaranteed with a few SNR degradations less than 4-dB.

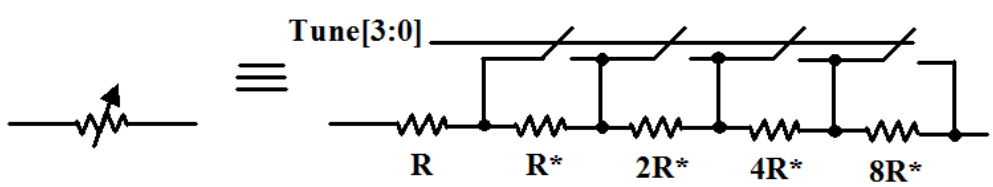


Figure 8: Equivalent circuit of the tunable resistor.

4. First integrator chopper negative-R technique

The input integrator is the most important stage of the CT ΔΣ ADC. The loop filter does not form the first integrator's non-idealities. The CT ΔΣ ADC's performance is however directly affected. At the ADC input, several elements produce noise sources. The noisiest components are the amplifier of the first integrator, the R_{DAC} resistors, and the input resistor R_1. The ADC input-referred noise can be expressed as [38, 39]

$$\bar{v}_{in}^2 = 2.\left(\bar{v}_{n,R_1}^2 + \bar{v}_{n,R_{DAC}}^2 \frac{R_1^2}{R_{DAC}^2}\right) + \bar{i}_{in,OTA}^2 R_1^2 + \bar{v}_{n,OTA}^2 \left(1 + \frac{R_1}{R_{DAC}}\right)^2, \tag{16}$$

where R_1 and R_{DAC} represent ADC 's dominant sources of noise to reduce its power consumption. If R_1 increases, the linearity of the active-RC filter increases to [40]. R_1 is set to 10-kΩ for the ADC and R_{DAC} is set to 4-kΩ. The thermal noise contribution limits the SNR to approximately 102-dB, which is well below the input signal peak value. The first integrator has an integrated capacitance C_1 of 8-pF.

We suggest using the well-known chopper stabilization method to mitigate the preamplifier's input-equivalent noise. The chopper stabilization circuit inserted around the preamplifier is shown in Fig. 9 [41, 42]. Two amplifiers compose the preamplifier. The first one depicts the main amplifier, $A_{main}(s)$, and the second one depicts the auxiliary amplifier, $A_{aux}(s)$. In low-frequency paths, $A_{aux}(s)$ cancel the non-idealities of $A_{main}(s)$. Firstly, $A_{aux}(s)$ measure the input signal of $A_{main}(s)$. The main amplifier virtual ground of value $V_X = V_{XP} - V_{XN}$ is then derived by the auxiliary amplifier toward zero. A compensation voltage of value $V_Y = V_{YP} - V_{YN}$ is therefore created by the auxiliary amplifier to the main amplifier. The virtual ground V_X can be defined as

$$V_X = \frac{V_{OUT}}{\left[A_{main}(s).\left(1 + A_{aux}(s)\right)\right]}, \tag{17}$$

The auxiliary amplifier enables the main amplifier noise component to be attenuated as

$$\overline{v}^2_{n,main_in} = \frac{\overline{v}^2_{n,main0_in}}{\left|A_{aux_int}(s)\right|^2}, \tag{18}$$

where $\overline{v}^2_{n,main_in}$ and $\overline{v}^2_{n,main0_in}$denote respectively the main amplifier's input noise with and without the auxiliary amplifier. The active RC-integrator signal transfer function (STF) is defined by $A_{aux_int}(s)$, which can be written as

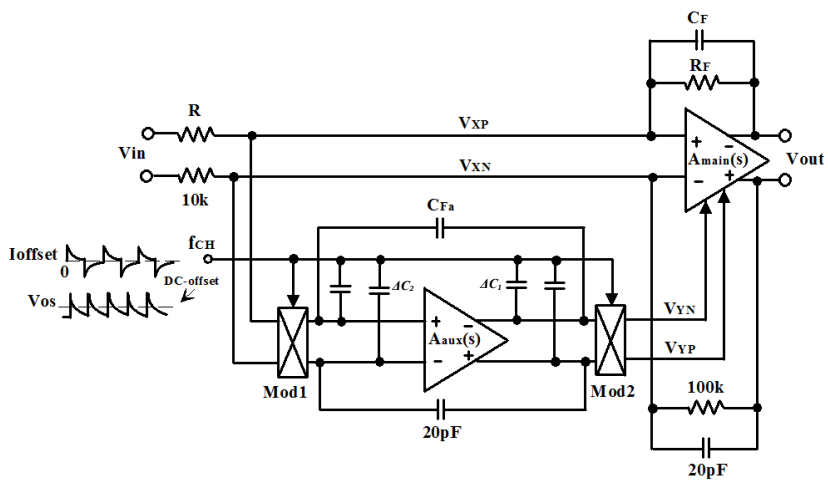


Figure 9: Chopper stabilization preamplifier.

$$A_{aux_int}(s) = \frac{A_{aux}(s)}{\left[1 + sR_1C_{Fa}\left(1 + A_{aux}(s)\right)\right]}. \tag{19}$$

The mismatch of the demodulated current spikes and the signal path creates an offset V_{os}. The capacitance mismatch due to the clock feed generates an AC current spike. The first modulator Mod1 rectifies the resulting AC current. Therefore, it generates a DC spike current at its input. The average current I_{offset} value of the measured DC spike can be written as

$$I_{offset} = 2.(\Delta C_1 - \Delta C_2)V_{clk}f_{CH}, \tag{20}$$

where ΔC_1 and ΔC_2 denote the parasitic capacitance of the chopper mismatch, V_{clk} is the magnitude of the clock signal and f_{CH} is the chopping frequency. This noise is flowing through the series impedance of the input signal source and the chopper stage. Therefore, it is represented by a voltage spike source placed in the amplifier input. The residual offset source V_{os} can be written as

$$V_{os} = 2R(\Delta C_1 - \Delta C_2)V_{clk}f_{CH}, \tag{21}$$

where R is the input resistance. The residual V_{os} offset represents the average DC spike value. In addition, a V_{os} spike voltage signal is generated at the input of modulator Mod1, producing a low-frequency

interference. To suppress this interference, we propose to create a proper delay Δt between the two chopping signals m1(t) and m2(t). Fig. 10 depicts the proposed delay-time chopper stabilization technique [43].

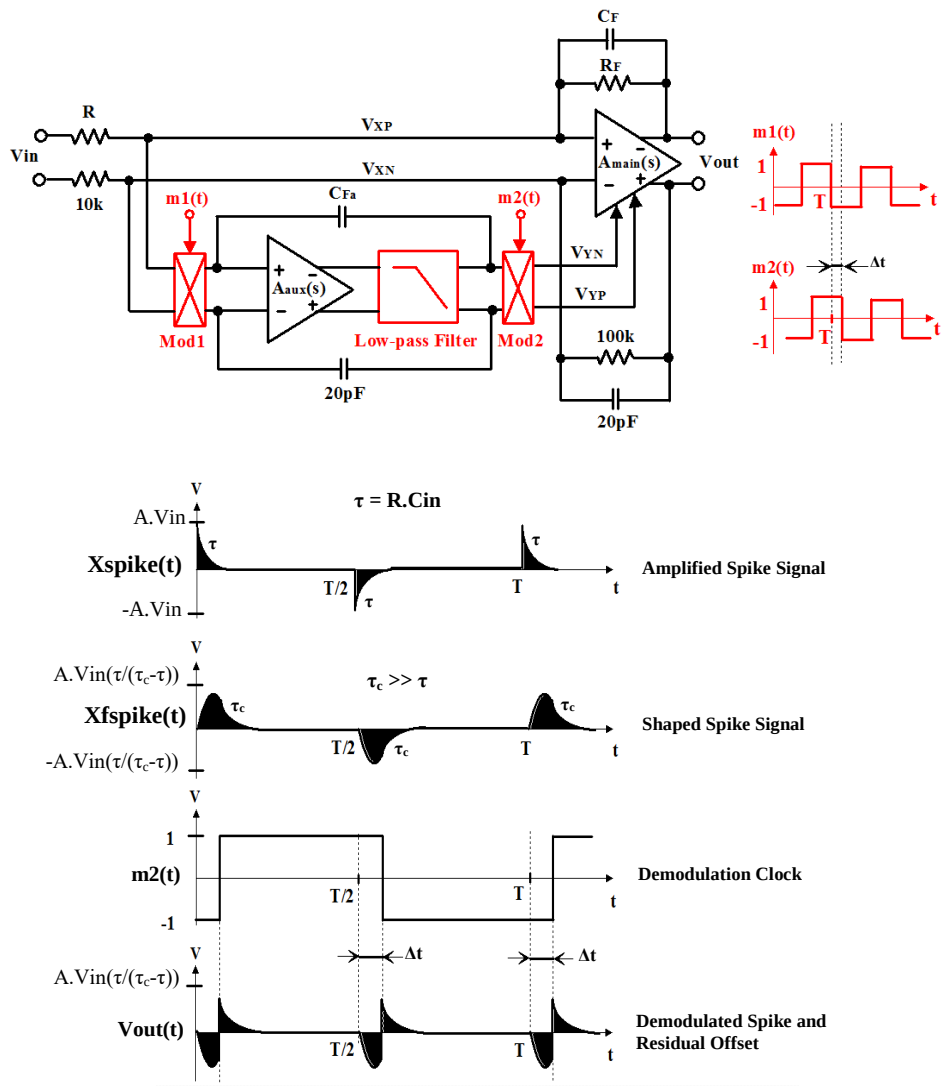


Figure 10: Delay-time chopper stabilization preamplifier.

The auxiliary amplifier $A_{aux}(s)$ is placed between the two modulators Mod1 and Mod2. In parallel, a delay Δt is introduced between the chopping signals m1(t) and m2(t). The spike signal generates by the two modulators is itself chopped owing to the addition of the delay Δt. The DC value of the output signal $V_{out}(t)$ is, thus, reduced. If an optimal delay value Δt_{opt} occurs, then the residual DC offset of the auxiliary amplifier $A_{aux}(s)$ is canceled. The optimal delay Δt_{opt} can be written as

$$\Delta t_{opt} = \log(2) \times \tau, \tag{22}$$

where$\tau = R \times C_{in}$. The resistor R is the amplifier input resistance and the capacitor C_{in} is the amplifier input capacitance.

The main drawback of this approach is the time τ itself. It is much dependent on both the input resistance R and input capacitance C_{in} of the amplifier. The spike pulse generated by the first modulator Mod1 attack the input of the preamplifier. The preamplifier, then, amplify this resulting spike pulse. Finally,

the amplified spike pulse is multiplied with the signal m2(t). Apart from chopping frequency higher-order harmonics, the resulting output signal V_Y contains a DC component. This DC component depicts the residual offset of the preamplifier caused by the chopping artifacts. A proposed technique to shape this DC spike is added to the chopper stabilization circuit. To solve this problem, a first-order low-pass filter is placed between the auxiliary amplifier $A_{aux}(s)$ and modulator Mod2. It has a time constant of τ_c. The square wave signal m1(t) has a period T with $T >> \tau_c >> \tau$. The created time τ_c primarily determines the time response of the shape of the filtered spike. The output offset of the preamplifier is linearly dependent on the time τ. Therefore, the optimal value of Δt_{opt} is determined in the worst-case preamplifier resistance. In this case, it is most useful to reduce the preamplifier offset. Approximately $\Delta t_{opt}/\tau_c$=0.8 has been selected for our proposed implementation. The cut-off frequency of the low-pass filter is fixed to 300 kHz. An f_{CH} of 120-kHz is the nominal chopping frequency.

Only $1/f$ noise is removed by the delayed chopper stabilization. The thermal noise of the auxiliary amplifier $A_{aux}(s)$ does not reduce. Therefore, the delayed chopper stabilization does not reduce the total noise level of the preamplifier. Likewise, to maintain its high gain at f_{CH}, a wide bandwidth of auxiliary amplifier $A_{aux}(s)$ is required. To decrease both the $1/f$ noise and thermal noise, we propose to add a negative-R technique to the proposed chopper stabilization circuit as shown in Fig. 11 [43]. This technique is proposed to remove the non-ideality of the preamplifier at V_X. It compensates for both I_R and I_{RF} error current produced at V_X by R and R_F respectively. Thus, the value of the proposed negative-R is properly determined to match the value of the two resistors R and R_F in parallel ($R//R_F$). Therefore, the V_X error is mitigated by the proposed chopper negative-R technique. For the chopper stabilization technique without the negative-R circuit, the preamplifier noise is studied. The overall preamplifier's noise transfer function (NTF) can be expressed as [43]

$$\frac{\overline{v}_{n,in}^2}{\overline{v}_{n,opamps}^2} = \left(1 + \frac{R_1}{R_F}\right)^2 [1 + s(R_1//R_F)C_F]^2, \tag{23}$$

where $\overline{v}_{n,in}^2$, and $\overline{v}_{n,opamps}^2$ are respectively the input-referred noise and the noise of the amplifiers. The $\overline{v}_{n,opamps}^2$ noise is determined at the input of the preamplifier. The NTF of the proposed chopper negative-R stabilization technique can be written as [43]

$$\frac{\overline{v}_{n,in}^2}{\overline{v}_{n,opamps}^2} = \left(1 + \frac{R_1}{R_F}\right)^2 [1 + s(R_1//R_F)C_F]^2 \left(\frac{\alpha - 1}{\alpha}\right)^2, \tag{24}$$

where the two parallel resistors $R \parallel R_F$ depict the negative-R circuit with an important matching coefficient α. If α is closer to 2, the noise opamps decrease ideally by a value of $\alpha = 1$. The negative-R circuit, in this case, contributes a noise level of $2.(R/R_N).4kTR_N$ to the $R_N = -\propto (R \parallel R_F)$. Therefore, the equivalent input-referred noise of the proposed negative-R preamplifier can be written as [43]

$$\overline{v}_{n,in}^2 = 2 \times \left[4kTR_1 + 4kTR_F\left(\frac{R_1}{R_F}\right)^2\right] + |H(s)|^2 \times \overline{v}_{n,opamps}^2, \tag{25}$$

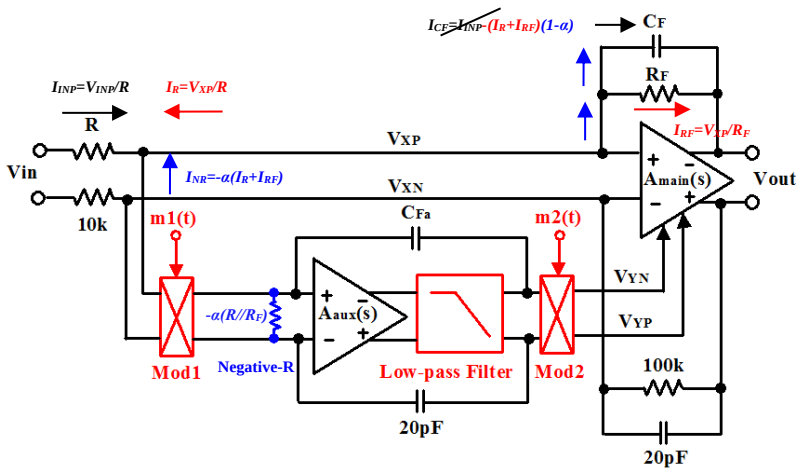


Figure 11: Chopper negative-R stabilization preamplifier.

where $|H(s)|^2$ is the noise transfer function of the negative-R with the opamps of Eq. (24). Thus, the chopper negative-R circuit enables mismatch and offset of the opamps to be attenuated.

The Negative-R transistor-level circuit is shown in Fig. 12. It is designed in a bipolar source degeneration topology. It only consumes 12-µW. In this circuit, the degenerated resistor and current source in this topology allow the precision of matching the circuit within 10% to be improved. In addition, a robust transconductance gm of the transistors of the negative-R circuit is preserved over the process variation with temperature and power supply [41].

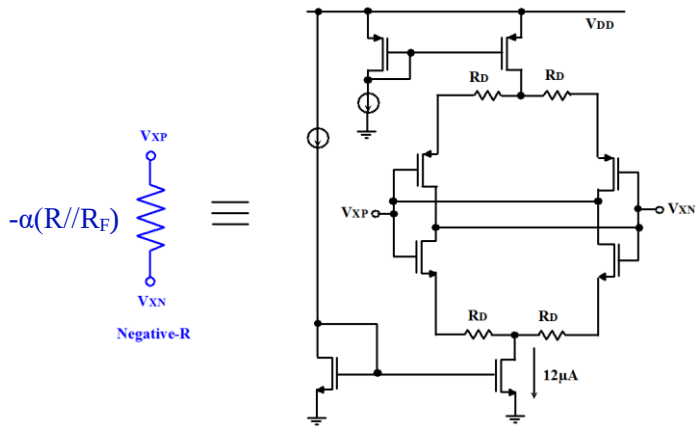


Figure 12: Negative-R circuit.

5. Experimental results

We have experimentally characterized a fabricated prototype of the proposed IoT circuit. It is based on an M&NEMS microphone and a CT ΔΣ ADC. The CT ΔΣ ADC circuit is designed in a CMOS 65-nm process with a 1.2-V supply voltage and a 0.1-mm^2 silicon area. Due to their high linearity, integrated resistors and capacitors are implemented with high-resistivity poly-resistors components and metal-insulator-metal (MIM) components respectively. Figure 13 depicts the die microphotograph of the proposed IoT circuit.

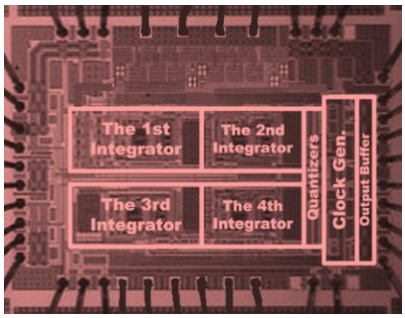


Figure 13: CMOS ΔΣ ADC microphotograph in a 65 nm process and a 0.1 mm^2 silicon die area.

We propose modifying the first integrator architecture to enhance the SNR, SNDR, and DR of the CT ΔΣ ADC developed in [27]. To reduce both the offset and $1/f$ noise, a positive feedback two-stage amplifier and a chopper negative-R technique are added to the first integrator. To measure the fabricated M&NEMS resistive microphone, we use the simultaneous comparison technique. To carry out the test of the chip, several measurement devices are used. A calibrated microphone, which acts as a reference microphone, will therefore be included in the test setup. It is located close to the measured M&NEMS microphone to evaluate its output responses. Moreover, we use an anechoic chamber for performing the complete measurement setup to isolate undesirable external phenomena. The M&NEMS microphone and the reference microphone are placed at a distance of one meter in front of the loudspeaker in the anechoic chamber. For measurement, the loudspeaker produces a sound that is used as a reference point at a frequency of 1-kHz. An EQ curve is used to achieve an equivalent response from the loudspeakers at all frequencies. The AP 2700 audio analyzer is coupled to both the M&NEMS microphone output and the B&K Type 2250 Analyzer output. An SRS-CG635 clock generator produces a precise clock with a range of less than 1-ps. We have also introduced an FPGA decimator filter for easier measurement results. The output of the filter attacks the sound analyzer AP 2700 with a serial audio interface.

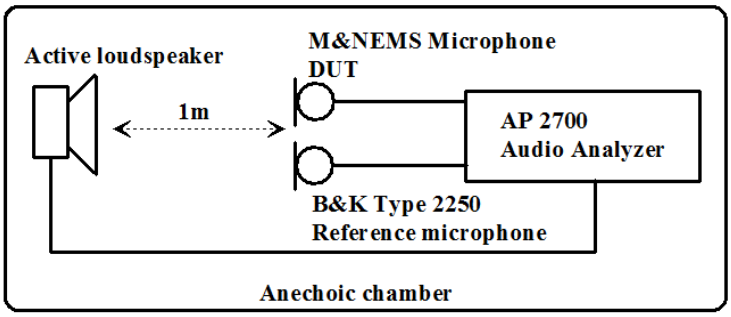


Figure 14: Measurement setup of the M&NEMS microphone system.

The loudspeaker's sound pressure is set at 94-dB. It has a sound frequency of 1-kHz. The instrument B&K analyzer allows detecting the intensity level of the generated sound. The sound level of 94-dB leads to a 1-Pa acoustic sound pressure level. The EQ curve allows correcting the frequency response to achieve a constant level. The frequency level of the neighbor reference microphone is then set at 1-kHz. The measurement result of the M&NEMS microphone in the 20-kHz frequency bandwidth to the reference frequency is presented in Fig. 15. The 94-dB sound pressure level corresponds to the 0-dB normalized response. It is obvious from Fig. 15 that the M&NEMS microphone has an approximately 20-kHz flat analog output response. In the second step, we perform the CT ΔΣ ADC measurements to define the peak SNR, peak SNDR, and it's DR.

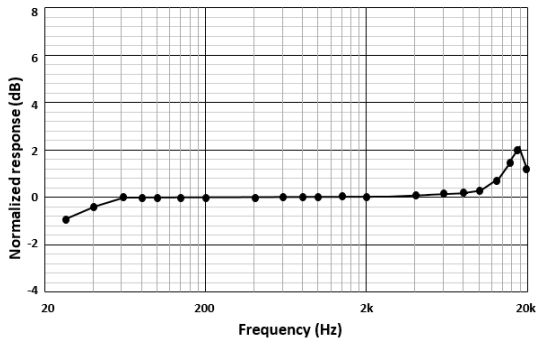


Figure 15: M&NEMS microphone response versus frequency with a 94-dB sound source level and a 20-kHz bandwidth.

We have measured SNR and SNDR of the CT ΔΣ ADC versus the input signal. The measurement results are shown in Fig. 16. The measured peak SNR is 102.8-dB with an input magnitude of -1.4-dBFS. The measured peak SNDR is 101.3-dB with an input magnitude of -3.4-dBFS. Furthermore, the measured DR of the CT ΔΣ ADC is 108-dB at 25° C.

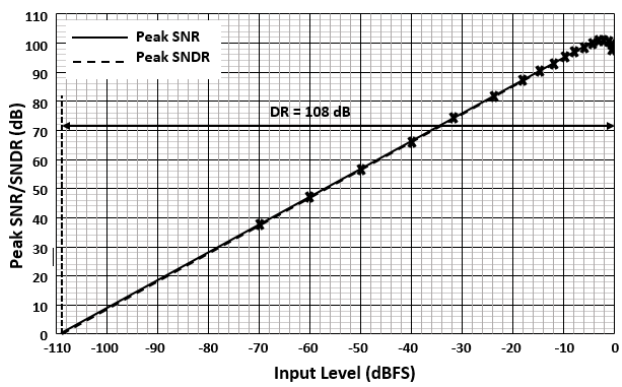


Figure 16: Measurement results of SNR and SNDR.

On the other hand, the CT ΔΣ ADC is attacked by an input signal of the magnitude of -3.4-dBFS and a frequency of 1-kHz. The measurement result of the CT ΔΣ ADC output spectrum is depicted in Fig. 17. From the measurement result, it is clear that the CT ΔΣ ADC is stable in the 20-kHz bandwidth. Moreover, the CT ΔΣ ADC reaches a good harmonic distortion (HD). The CT ΔΣ ADC has an overall measured power consumption of about 0.96 mW. The analog part consumes nearly 0.8 mW and the digital part consumes nearly 0.16 mW.

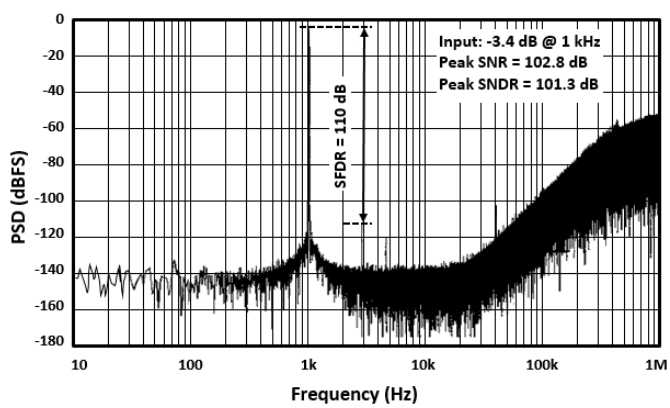


Figure 17: Measurement of the FFT response with a -3.4-dB and 1-kHz input.

We also carried out some measurements of the CT ΔΣ ADC performance at various temperatures to determine the influence of the temperature on the fabricated circuit. Measurement results of the SNR and SNDR versus temperature are presented in Fig. 18. The temperature ranges from 0° C to 90° C. From measurement results, the SNR and the SNDR are reduced by only 2-dB if the temperature varies from 0° C to 90° C. Therefore, the variation of the temperature does not affect the performance of ADC.

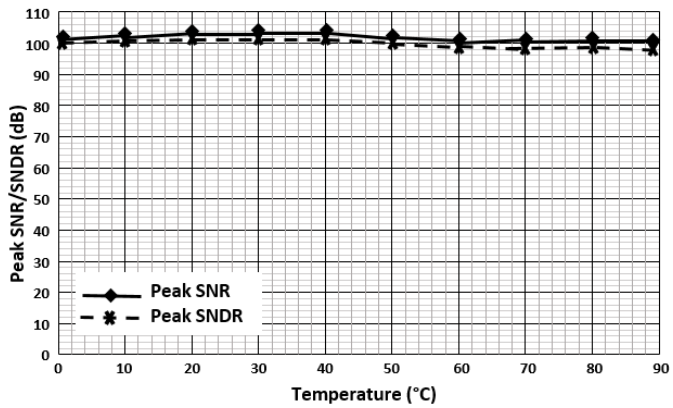


Figure 18: SNR and SNDR of the ADC versus temperature.

Table 1 summarizes the proposed CT ΔΣ ADC measurement results and the comparison with the state-of-the-art. The main advantage of the proposed M&NEMS microphone is that measurement results are done for the complete system composed of the CT ΔΣ ADC and the M&NEMS sensor. However, compared ADCs in the state-of-the-art are measured without the MEMS sensor. Measurement results of the SNR, SNDR, and DR of all other ADCs are near or just over 100-dB [44, 45, 29, 46-48]. On the other hand, our proposed CT ΔΣ ADC reaches a value greater than 100-dB for the same performance. Another important parameter is used to compare the output of the ADC and determine its performance. This parameter is the Schreier figure-of-merit (FOMs), which can be written as [49]

$$FOM_s = DR + 10\log\left(\frac{BW}{Power}\right). \tag{26}$$

From measurement results, the proposed CT ΔΣ ADC reaches a FOM of 181.2-dB. As a result, the proposed ADC reveals a competitive performance compared to the ADCs of state-of-the-art.

The CMOS interface chip is combined with a fabricated MEMS microphone to verify the performance improvement in the system. The closed-loop test setup uses a shaker table, a data acquisition board, and LABVIEW and MATLAB programs for signal processing. Since the interface electronics uses a high oversampling sigma-delta modulation technique, the PWM output bit stream has to be processed to obtain a useful signal. This is realized by transferring the digital output to a computer by means of a data acquisition board, and processing the signal. The entire system has been operated in closed-loop and the functionality of the system has been verified through extensive tests. The total power consumption is 0.96 mW. Moreover, a noise density of 7 nV/√Hz is achieved within the frequency range from 10 Hz to 10 kHz confirming the theoretical value.

Table 1: The proposed CT ΔΣ ADC compared to the State-of-the-Art.

Parameters	[44]	[45]	[29]	[46]	[47]	[48]	This work
Technology, nm	180	28	65	160	180	40	65
Power, mW	0.28	1.13	0.8	1.12	0.28	0.01	0.96
Supply, V	1.8	3.3	1	1.8	1.8	1.2	1.2
BW, Hz	24k	24k	25k	20k	24k	5k	20k
Peak SNDR, dB	98.2	98.5	95.2	103	98.5	93.5	101.3
Peak SNR, dB	102	101	100	106	99.3	94.3	102.8
FOMs, dB	182	174	178	181	183	187	181.2
DR, dB	103	101	103	109	104	96.5	108
Area, mm^2	1	0.02	0.25	0.16	1	0.05	0.1

6. Conclusions

This paper presents a proposed audio IoT system. A silicon nanowire and a 4th-order single-bit CT ΔΣ ADC are the M&NEMS accelerometer sensor and the CMOS readout interface, respectively. Various low-noise and low-power techniques are proposed to reduce the power consumption and noise of the CT ΔΣ ADC and maintain good performance. A continuous-time loop filter to relax the amplifiers' settling times replaces the discrete-time loop filter switches of the ADC. The proposed chopper negative-R technique is inserted around the first integrator because it is the noisiest ADC block. This technique allows mitigating the offset and $1/f$ noise. The first integrator is based on a positive feedback DC-gain enhancement two-stage amplifier, while the second to the fourth integrators; is based on a simple fully differential amplifier. The quantizer is embedded in the feedforward coefficients to minimize power consumption and improve performance. The proposed CT ΔΣ ADC is designed in a 65-nm CMOS process with a core area of 0.1-mm^2. The supply voltage and the power consumption are respectively 1.2-V and 0.96-mW. The complete audio IoT system is fabricated and measurement results are performed to extract its performances. Over a signal bandwidth of 20-kHz, the CT ΔΣ ADC measurement results reach a peak SNR of 102.8-dB, a peak SNDR of 101.3-dB, and a DR of 108-dB. As a result, the proposed CT ΔΣ ADC becomes one of the best audio ADCs from the result of measurements.

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