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Abstract—**Piezoelectric energy harvesting (PEH) interfaces have been widely investigated during the last decades in order to maximize the harvested power. Among the energy extraction circuits proposed in the literature, some of the most effective ones consist of extracting the electric charges from the piezoelectric elements in a synchronous way with the vibrations and within a very short portion of the vibration period (SECE, SECPE, FTSECE, etc.). For these strategies, most previous studies take the electrical efficiency (i.e., the electrical losses between the energy extracted from the piezoelectric element and the energy which is finally transferred in a storage element) into account in an ad-hoc and case-by-case manner. In this brief, we propose a unified analysis that applies to model the electrical efficiency of these SECE-based strategies taking into account losses introduced by the electrical interface. We identify the main loss mechanisms by demonstrating that the electrical efficiency mainly varies with two parameters: the quality factor of the electrical interface and the voltage inversion ratio of the considered strategy. Measurements on the FTSECE strategy show that our model predicts the stored power with a good accuracy and allows a better optimization of the harvesting interface (up to 5.4 times more stored power at off-resonance frequencies, and 30% larger harvesting bandwidth).**

I. Introduction

Electrical interfaces for piezoelectric energy harvesters come as a variety of strategies that have been attracting research interest for many years [1]. Each electrical strategy proposed in the literature can be associated with a particular power limit, a power bandwidth, and a frequency response [2,3]. While classical analyses allow to predict the *stored power* P_{stored} (i.e. the power which is eventually transferred on a storage element) for some strategies such as the standard bridge rectifier [4] or the parallel synchronized switch harvesting on inductor (SSHI) technique [5], these analyses only allow to predict the *extracted power* P_{ext} (i.e. the power which is extracted from the piezoelectric element without taking into account the unavoidable losses in the interface circuit used to transfer the electrical charges to a storage element) for the synchronized electric charge extraction (SECE) interface, or other SECE-based interfaces such as the short-circuit SECE (SCSECE) or the synchronous electric charge partial extraction (SECPE) [6, 7]. Some researchers recently proposed accurate analyses of the stored power with particular implementations of the SECE [8,9], but these analyses are topology-dependent and are hardly generalizable to all SECE-based interfaces and their various implementations [1]. Thus, in the current literature, there lacks a comprehensive and unified approach of the stored power in SECE-based interfaces.

In this brief, we propose to refine the classical analysis by adding the most significant electrical losses in those strategies' analysis, leading to a compact expression of the stored power

P_{stored} depending on an electrical efficiency η_{elec} (defined in Fig.1), valid for most SECE-based strategies in the literature. Finally, the proposed approach is applied and validated on a recently developed strategy, the frequency-tuning (FTSECE) [10].

II. Constant displacement extraction strategies

In this study, we focus on CDE strategies. These strategies consist of extracting the energy from the piezoelectric material within a very short duration (compared to the period of the mechanical vibration). This results in a negligible variation of the mechanical displacement x between the start and the end of the energy extraction phase, which is why we choose to call them CDE. Well-known interfaces for CDE strategies are the SECE interface [11] and its tunable versions: SECPE [6], SCSECE [7], FTSECE [10], phase-shifted SECE (PSSECE) [12], N-discharge SECE (NSECE) [13], synchronous inversion and charge extraction (SICE) [14], tunable SECE [15], unipolar SECE (USECE) [16] ... As shown in Fig.2, the energy is quickly extracted from the harvester when the piezoelectric voltage is equal to v_{tr} (corresponding to an angular phase-shift ϕ_S with the voltage extremum). The voltage varies during the energy extraction from v_{tr} to βv_{tr} (β being the voltage inversion ratio), meaning that a transitory energy storage (such as an inductor) is required to transmit the energy to a storage element (e.g., a capacitor).
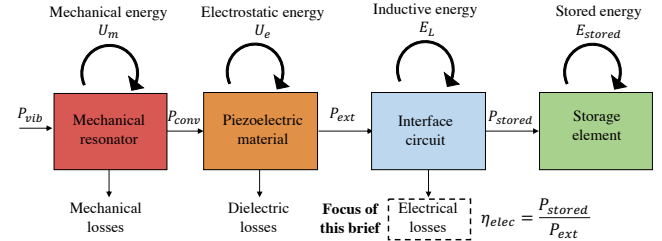
Fig. 1. Power path of a piezoelectric energy harvesting system with a CDE strategy and definition of the electrical efficiency. Note that for ceramic-based PEH, the dielectric losses are usually considered negligible [1].

Table. 1. Some SECE-based interfaces in the literature. Note that the efficiency of all SECE-based interfaces does not depend (in first approximation) on the electrical load.

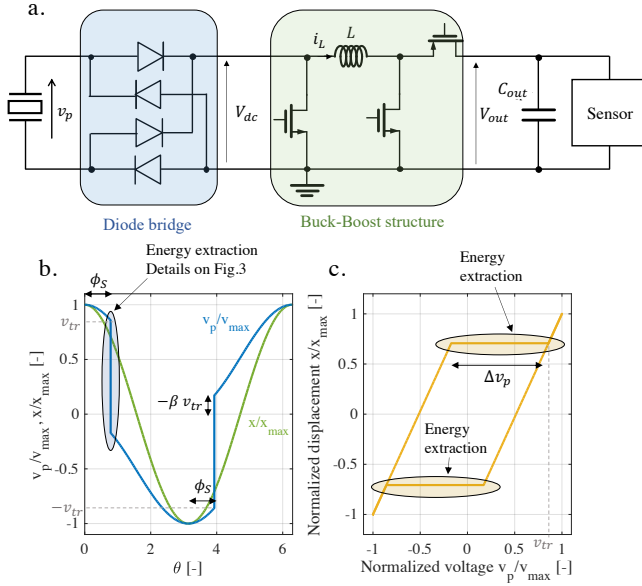| Interface acronym	Energy extraction angle ϕ_S	Voltage inversion ratio β	Optim. of the power at resonance	Optim. of the BW	Ref.
SECE	0°	0	No	No	[8]
SECPE	0°	[−1,1]	Yes	No	[6]
Tunable SECE	0°	[−1,1]	Yes	No	[15]
SCSECE	[−90°, 90°]	0	Yes	Yes	[7]
FTSECE	[−90°, 90°]	[−1,1]	Yes	Yes	[10]
NSECE	0°	0	Yes	No	[13]
SICE	0°	[−1,1]	Yes	No	[14]
USECE	0°	0	No	No	[16]

Fig. 2. Examples of a. system implementation, b. normalized transient waveforms and c. normalized energy cycle of a CDE strategy. β represents the voltage inversion ratio, ϕ_S the energy extraction angle, and v_{tr} the value of the piezoelectric voltage when the energy extraction begins.

Thus, in CDE strategies, the harvesting process consists of a two-step energy conversion: a first step where the energy is transferred from the harvester to the inductor, and a second step where the energy is stored from the inductor to the storage element. Unlike other techniques, such as a standard bridge rectifier [4] or the parallel SSHI [5], where it is possible to determine the stored power analytically, previous studies of CDE strategies usually consider the electrical efficiency in an ad-hoc and case-by-case manner [8, 9].

III. FROM THE EXTRACTED TO THE STORED POWER

A. Extracted power derivation of CDE strategies

Assuming that the dielectric losses are negligible (Fig.1), it has been proven in [1] that there exists a limit power P_{lim} that can be harvested for a harvester of mass M with linear damping (of mechanical quality factor Q_m) actuated by a sinusoidal vibration of constant amplitude γ. This expression is (1) where ω_0 is the natural short-circuit angular frequency.

$$P_{lim} = \frac{M\,\gamma^2 Q_m}{8\,\omega_0} \qquad (1)$$

In the case of CDE, the extracted power can be calculated from equation (2) where k_m^2 is the expedient electromechanical coupling and $\Omega = \omega/\omega_0$ the normalized vibration frequency.

$$P_{ext} = P_{lim}\frac{4k_m^2\varepsilon_D\Omega/Q_m}{(1-\Omega^2+k_m^2\varepsilon_K)^2+(\Omega/Q_m+k_m^2\varepsilon_D)^2} \qquad (2)$$

ε_D and ε_K represent the electrically-induced damping and stiffness. Their expressions depend on the CDE strategy and are given for most strategies in [1].

B. Stored power derivation

We propose to model an electrical efficiency η_{elec} (defined in Fig.1) that takes into account part of the losses in the electrical interface. Fig.3 depicts the piezoelectric voltage v_p and the inductor current i_L during the energy extraction of any CDE strategy (it could be a zoom on the energy extraction sequence for the strategy shown in Fig.2.b.). CDE interfaces can be characterized by their voltage inversion ratio $\beta \in [\beta_{min}, 1]$, as shown in Fig.2 and Fig.3 (with β being the ratio of the piezoelectric voltage right after the charge inversion over the piezoelectric voltage right before the inversion). $\beta_{min} \approx -e^{-\frac{\pi}{2Q_e}}$ gives the minimum possible inversion considering the quality factor $Q_e = R_{tr}^{-1}\sqrt{L/C_p}$ of the interface circuit [17], with R_{tr} being the total equivalent resistance of the resonant loop (modeling all the linearized losses in the components that can be found in the current path: diodes, wires, transistors and inductor) and C_p is the piezoelectric material capacitance.

From Fig.3, we observe that the energy flow is divided into two successive events: i) a transfer phase (yellow area) where the energy flows from the piezoelectric material to the inductor and ii) a charging phase (red area) where a portion of the energy is stored from the inductor to the storage capacitor.

We will assume that the major part of electrical losses is in the transfer phase of Fig.3. Indeed, the losses in the storage phase mainly depend on the active components used in the power path and on the voltage across the storage element. Hence, the contribution of the storage phase to the overall losses can be significantly reduced with appropriate components and sizing (low-Vt diodes or transistors having large channel widths for instance) and if the ratio between the output voltage and the diode threshold voltage used in the power path is sufficiently large [9]. This means that the impact of the load on the electrical efficiency is assumed to be relatively small, which is a common assumption for SECE-based interfaces [1] that has been experimentally verified in Fig. 7.
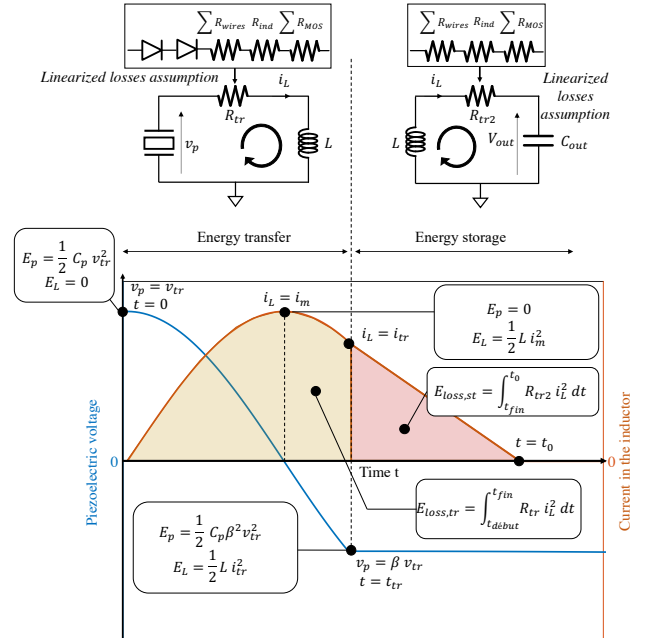

Fig. 3. Current and voltage waveforms of a CDE interface during the energy extraction. The mechanical displacement variation is considered negligible between the start and the end of the energy extraction phase.
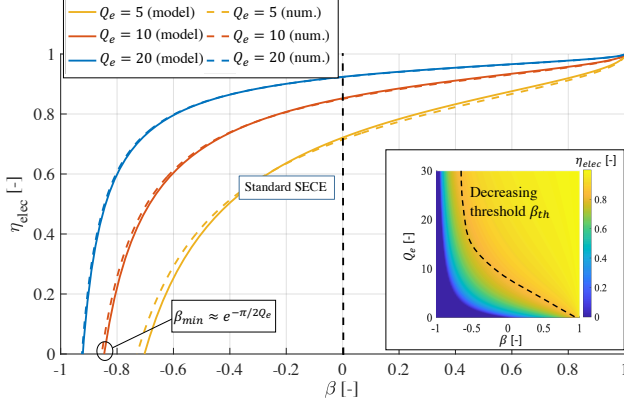
Fig. 4. Comparison of numerical and analytical values of η_{elec} as a function of β for three different electrical quality factors Q_e.

IV. DERIVATION OF THE EFFICIENCY FOR CDE INTERFACES

From Fig.3, the extracted energy with a CDE can be expressed by (3) as a function of the voltage inversion ratio.

$$E_{ext} = \frac{1}{2} C_p v_{tr}^2 (1 - \beta^2) \tag{3}$$

The peak of current through the inductor is reached when all the energy has been transferred from the piezoelectric generator to the inductor. Thus, when the current is maximum, the energy stored in the inductor is equal to the energy initially stored in the piezoelectric material before the charge extraction pondered by the electrical losses (taken into account thanks to $\eta_{elec}|_{\beta=0}$). This consideration is expressed analytically by (4) where i_m is the peak current through the inductor L.

$$L\, i_m^2 = C_p v_{tr}^2 \eta_{elec}|_{\beta=0} \tag{4}$$

The losses in the electrical interface during the energy transfer to the inductor can be established as (5) considering that the losses are relatively low ($Q_e > 1$).

$$E_{loss,tr} = \int_0^{t_{tr}} i_m^2 \sin^2 \left(\frac{t}{\sqrt{LC_p}} \right) R_{tr}\, dt \tag{5}$$

Solving the integral (5) with $t_{tr} \approx \arccos(\beta)\sqrt{LC_p}$, the losses during the energy transfer $E_{loss,tr}$ can then be expressed by equation (6).

$$E_{loss,tr} = \frac{E_{ext}\, \eta_{elec}|_{\beta=0}}{Q_e(1-\beta^2)} \left(\arccos(\beta) - \beta\sqrt{1-\beta^2} \right) \tag{6}$$

From (6) and considering the case when $\beta = 0$, we can find the expression of $\eta_{elec}|_{\beta=0}$.

$$\eta_{elec}|_{\beta=0} = \frac{E_{ext} - E_{loss,tr}|_{\beta=0}}{E_{ext}} = \frac{2Q_e}{2Q_e + \pi} \tag{7}$$

Combining (7) with (6), we eventually find the expression of the electrical efficiency for CDE interfaces as a function of the voltage inversion ratio β:

$$\eta_{elec}|_{CDE} = 1 - 2\frac{\arccos(\beta) - \beta\sqrt{1-\beta^2}}{(1-\beta^2)(\pi + 2\,Q_e)} \tag{8}$$

Equation (8) shows that a higher Q_e as well as a higher β (i.e., less collected / re-invested electrical charges) lead to higher electrical efficiencies. In the other hand, a smaller β leads to a higher electrical damping which might translate in a greater extracted power (for lowly coupled / highly damped harvesters or when the vibration frequency is far from the resonant frequency) [10]. Hence, to maximize the stored power, there can exist a trade-off between maximizing the extracted power (with low β values) and minimizing the electrical losses (with high β values).

Comparisons between equation (8) and numerical results obtained on an electrical simulator for various electrical quality factors demonstrate the good accuracy (absolute error < 0.05) of the proposed analytical derivation, as shown in Fig.4. For instance, the standard SECE ($\beta = 0$) exhibits an electrical efficiency of 0.72, 0.85 and 0.92 for electrical quality factors of 5, 10 and 20, respectively. Interestingly, we can observe that the electrical efficiency decreases quasi-linearly when β is large, but starts to drop exponentially below a decreasing threshold β_{th} (shown in Fig.4). This shows that the electrical efficiency of CDE remains relatively high as long as $\beta \geq \beta_{th}$ (no electrical charges re-injected in the piezoelectric material) but drops quickly when $\beta < \beta_{th}$ (too many charges are re-injected leading to important electrical losses). This confirms some tendencies that have been observed experimentally in the literature but have never been analytically modeled [6, 10].

V. EXPERIMENTAL VALIDATION OF THE PROPOSED ELECTRICAL EFFICIENCY FOR CDE STRATEGIES

In order to verify the proposed electrical efficiency model, we fixed a PMN-PT-based PEH on an electromagnetic shaker driven by a power amplifier at an acceleration amplitude of $0.4 m.s^{-2}$, as illustrated by Fig.5. The PEH electrodes have been connected to the PCB circuit shown in Fig.6. This PCB circuit includes an inductive switch made of two NMOS transistors BSP130 and two BAS116H diodes in series with a custom-made 1H inductor. As illustrated in Fig.6.a, every semi period of vibration, this switch is closed at a particular energy extraction angle ϕ_s ($\theta = \phi_s + k\pi$, $k \in \mathbb{N}_1$), and the energy is transferred from the PEH to the inductor. The switch is opened when the inversion ratio reaches a pre-defined value β, and the energy remaining in the inductor is then transferred in a 2mF capacitor through a bridge rectifier made with four BAS116H diodes. The voltage V_{out} across the capacitor has been adjusted thanks to a programmable decade resistor (MEATEST M642) used to emulate the sensor power consumption. Hence, thanks to the control signal of the inductive switch, the waveforms shown in Fig.2.b can be implemented for any values of (ϕ_s, β). The experimental setup has been automated thanks to a dSpace control and acquisition board, in order to extract the power for various combinations of inversion ratio β, energy extraction

angle ϕ_s, output voltage V_{out}, and vibration frequency f (30 values of $\beta \in [-0.6, +0.6]$, 30 values of $\phi_S \in [-90°, +90]$, 5 values of $V_{out} \in [+2V, +15V]$ and 50 values of $f \in [20Hz, 40Hz]$). We realized more than 200000 acquisitions on the automated testbench shown in Fig.5. For each acquisition, the extracted power as well as the stored power have been measured, which allowed us to compute the electrical efficiencies shown in Fig.7.

We can observe that the experiments are in good agreement with the theoretical model given by (8) and validate the efficiency dependency on the inversion ratio. The main contributor to the electrical efficiency variations seems to be the voltage inversion ratio, the other parameters sharing statistically a relatively small impact on its value. We attribute the main variations of the efficiency to the nonlinearities of the electrical interface (nonlinear losses in the inductor, diodes, and transistors) which lead to variations of the electrical quality factor depending on the extracted energy level.
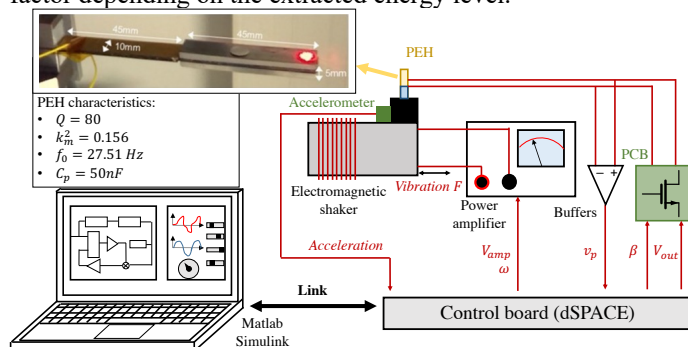

Fig. 5. Piezoelectric energy harvester and automated experimental setup used to verify the proposed electrical efficiency model.
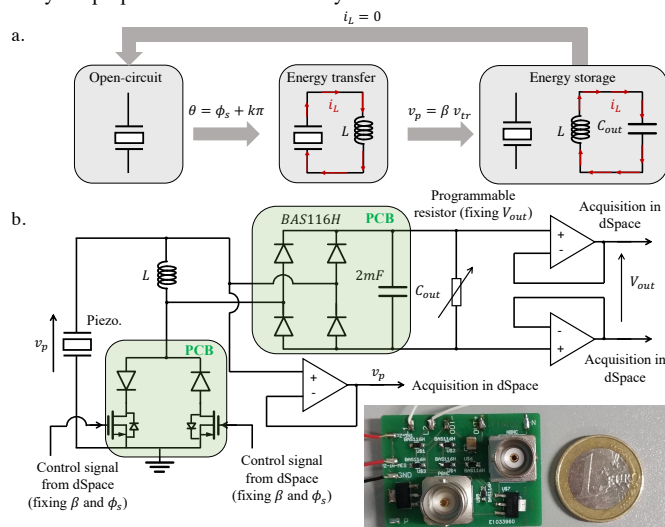

Fig. 6. a. Simplified three-steps operation of the circuit and b. PCB used to implement the FTSECE. High-voltage High-impedance buffers are used to send the signals from the PCB/PEH to dSpace. Note that the waveforms associated with the circuit for a given β and ϕ_s are shown in Fig.2.b. and Fig.3.

Figure 7 confirms the assumption that the losses during the energy storage remain negligible compared to the losses in the energy transfer, as long as β is small ($\beta \leq 0.2$). When few charges are extracted (i.e., when β gets close to 1), the losses during the energy transfer become excessively small, leading to a growing difference between the experiments and (8). Nevertheless, our model is accurate enough to predict the

behavior of any CDE strategy along with the inversion coefficient for any voltage inversion ratio, angle of the energy extraction, vibration frequency, and output voltage.
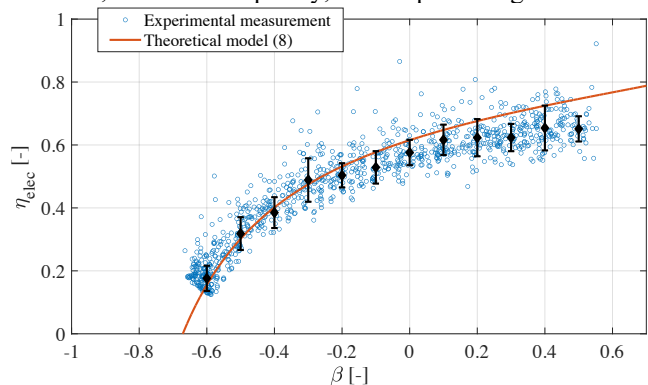

Fig. 7. Theoretical and experimental measurements (with averages and 1-sigma error bars) of the electrical efficiency on a generalized CDE strategy as a function of the voltage inversion coefficient β. During the whole experiment, the electrical quality factor $Q_e = 4.3$.

VI. APPLICATION TO OPTIMIZE FTSECE TUNING PARAMETERS

An example of strategy whose analysis can be refined thanks to the electrical efficiency is the Frequency Tunable Synchronous Electrical Charge Extraction (FTSECE). This strategy (experimentally validated in [10]) is a CDE with two tuning parameters: the voltage inversion ratio β and the phase shift ϕ_s between energy extraction events and extrema of voltage. A fine tuning of β and ϕ_s for each vibration frequency allows to increase the harvester's bandwidth as well as to optimize the extracted and stored powers. The circuit implementing this strategy controlled by a dSpace board is shown in Fig. 6 and exhibits a measured electrical quality factor $Q_e = 4.3$.

$$\begin{cases} \varepsilon_D = \dfrac{4}{\pi}\dfrac{1-\beta}{1+\beta}\cos^2(\phi_S) \\ \varepsilon_K = 1 + \dfrac{2}{\pi}\dfrac{1-\beta}{1+\beta}\sin(2\phi_S) \end{cases} \quad (9)$$

As described in [10], the extracted power with the FTSECE can be obtained from (1) and (2) with the electrical damping and stiffness expressions given by (9). The optimal value of the extracted power (with a fine tuning for every vibration frequency of β and ϕ_s and for the PEH parameters shown in Fig.5) is shown in yellow in Fig.8.a. We also obtain the stored power thanks to the extracted power expression pondered by (8). The optimal value of this stored power is obtained by maximizing $(\eta_{elec}P_{ext})$ with a fine tuning of β and ϕ_S and is shown in blue in Fig.8.a. Note that in each case, the optimal values of β and ϕ_S depend on the PEH characteristics (k_m^2 and Q), as detailed in [10].

Figure 8.a demonstrates that the inclusion of the electrical efficiency in the analysis is consistent with the measured power (red diamonds) and allows for an accurate model of the stored power with the FTSECE (as an example of CDE strategy). Fig.9 proves that choosing the β that directly maximizes the stored power (shown in red in Fig.8.a) allows for a better optimization of the FTSECE than optimizing the extracted power while not considering the electrical efficiency during the choice of the β.

Indeed, directly optimizing the stored power allows to increase the stored power by up to 5.4 times (for a vibration frequency of 32Hz) compared to a standard optimization of the extracted power. Furthermore, the proposed optimization enlarges the harvesting bandwidth (frequency bandwidth where the stored power is greater than 0.5 P_{lim}) by 30%.

Our model allows a first analytical estimation of the electrical efficiency for a given strategy, while providing physical insights on the losses' origins. Such model facilitates the electromechanical optimization of piezoelectric energy harvesters while taking into account the electrical losses, without relying on heavy computations and circuit simulations. The proposed model also enables the realistic comparison of various electrical strategies (i.e. SECE-based strategies with SSHI) without requiring long circuit simulations consisting of multiple parametric sweeps.
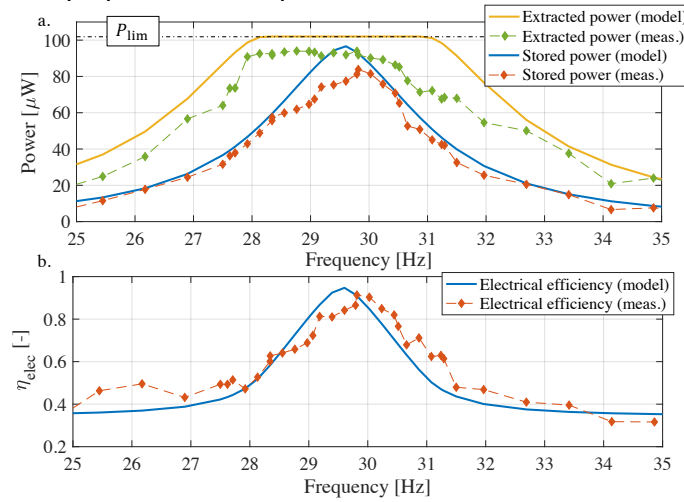

Fig. 8. a. Theoretical and experimental measurements of the extracted power and stored power obtained with the FTSECE and b. electrical efficiency.
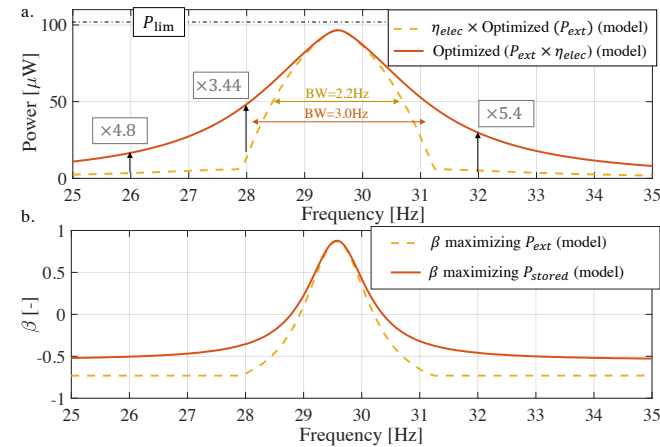

Fig. 9. Stored power obtained with the FTSECE strategy with an optimization of the extracted power and an optimization of the stored power.

VII. CONCLUSION

In this brief, we present an analytical expression of the electrical efficiency in order to take into account the losses in CDE strategies and estimate the stored power. This analysis completes the existing modeling and predictions already conducted to analytically express the extracted power from the piezoelectric harvester, and give physical insights about the main loss mechanisms in energy harvesting interfaces. As

proved experimentally with the FTSECE strategy, our approach enables a more realistic estimation of the stored power while not sacrificing the generality of the analytical approach. Furthermore, our approach enables a joint optimization of the harvester and its associated electrical interface (i.e., the FTSECE) by choosing the electrical parameters that maximize the stored power and not only the extracted power. This optimization allows us to enlarge the harvesting bandwidth by 30%, and to increase the off-resonance stored power by up to 5.4 times.

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