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Yazan Barazi, Frédéric Richardeau, Frédéric Richardeau, Jean-Michel Reynes. VDS and VGS Depolarization Effect on SiC MOSFET Short-Circuit Withstand Capability Considering Partial Safe Failure-Mode. *Energies*, 2021, Invited Paper - Special Issue Safety Design and Management of Power Devices including Gate-Drivers, 10.3390/en14237960 . hal-03456511

HAL Id: hal-03456511

<https://hal.science/hal-03456511>

Submitted on 30 Nov 2021

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Article

V_{DS} and V_{GS} Depolarization Effect on SiC MOSFET Short-Circuit Withstand Capability Considering Partial Safe Failure-Mode

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Abstract: This paper presents a detailed analysis of 1200 V Silicon Carbide (SiC) power MOSFET exhibiting different short-circuit failure mechanisms and improvement in reliability by V_{DS} and V_{GS} depolarization. The device robustness has undergone an incremental pulse under different density decreasing; either drain-source voltage or gate-driver voltage. Unlike silicon device, the SiC MOSFET failure mechanism firstly displays specific gradual gate-cracks mechanism and progressive gate-damage accumulations greater than $4 \mu\text{s}/9 \text{ J}\cdot\text{cm}^{-2}$. Secondly, a classical drain-source thermal runaway appears, as for silicon devices, in a time greater than $9 \mu\text{s}$. Correlations with short-circuit energy measurements and temperature simulations are investigated. It is shown that the first mechanism is an incremental soft gate-failure-mode which can be easily used to detect and protect the device by a direct feedback on the gate-driver. Furthermore, it is highlighted that this new mechanism can be sufficiently consolidated to avoid the second drain-source mechanism which is a hard-failure-mode. For this purpose, it is proposed to sufficiently depolarize the on-state gate-drive voltage to reduce the chip heating-rate and thus to decouple the failure modes. The device is much more robust with a short-circuit withstand time higher than $10 \mu\text{s}$, as in silicon, no risk of thermal runaway and with an acceptable penalty on R_{DS-ON} .

Keywords: SiC MOSFET; failure analysis; gate damage; fail-to-open; fail-to-short

Citation: Barazi, Y.; Richardeau, F.; Jouha, W.; Reynes, J.-M. V_{DS} and V_{GS} Depolarization Effect on SiC MOSFET Short-Circuit Withstand Capability Considering Partial Safe Failure-Mode. *Energies* **2021**, *14*, 7960. <https://doi.org/10.3390/en14237960>

Academic Editors: Adolfo Dannier and Andrea Mariscotti

Received: 20 September 2021
Accepted: 23 November 2021
Published: 29 November 2021

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1. Introduction

The 4H-Silicon Carbide (4H-SiC) material has much better physical characteristics than silicon (Si). With a threefold higher band-gap energy, a tenfold higher breakdown field, and an extremely low intrinsic free carrier concentration, 4H-SiC is a leading material for high-voltage power devices. Due to the difficulties of deep and wide P+ doping implantation, bipolar devices such as BJT (Bipolar Junction Transistor) and IGBT (Insulated Gate Bipolar Transistor) are not as easy to process as for silicon. A unipolar SiC device such as MOSFET (Metal Oxide Silicon Field Effect Transistor) is preferred. However, non-native oxide based SiO_2 -SiC structures still suffer from imperfections at the SiC interface leading to reduced mobility in the channel with gate-threshold voltage drift. However, SiC MOSFETs offer several advantages compared to silicon device (low on-state and switching losses, higher switching frequencies, and higher temperature stability), which makes them an alternative solution of IGBT or silicon Super-Junction MOSFETs, up to 30% to 50% losses reduction can be achieved depending on switching frequency and voltage rating [1]. SiC MOSFETs are taking over different markets, where they are found in different applications, especially on-board chargers or power trains in automotive for medium power and railways for high power. However, in extreme operation, short-circuit (SC) robustness is a key application requirement for semiconductor power devices. The short-circuit (SC) withstanding time (T_{SCWT}) of standard and commercial SiC MOSFETs is much lower than that of silicon

devices [2]: from 10 μs , which is now practically the IGBT standard, to a few μs for recent commercial MOSFET device. This difference is due to the continuous reduction of the chip area and thus the increase of the current density in the extreme short-circuit operation. Indeed, manufacturers optimize SiC MOSFET from the point of view of reducing switching times and energies by reducing input–cross–output structural capacitors (C_{iees} , C_{rss} , C_{oss}) of the chip, with the same apparent drain-source on-state resistance (R_{DSON}). This implies faster gate-driver protection, which must also remain robust against switching oscillations at turn-on. In order to compensate the low short-circuit robustness of SiC MOSFET, specific designs have been analyzed to find the best trade-off between T_{SCWT} and $R_{\text{DSON}} \cdot \text{cm}^2$ (normalized on-state drain-source resistance). A first approach consists in optimizing the gate geometry while remaining in usual planar structure. In [3], authors show that a thinning of the gate from 55 nm under $V_{\text{GS}} = 20 \text{ V}$ to 27 nm under $V_{\text{GS}} = 10 \text{ V}$ allows to increase T_{SCWT} by 47% at the cost of only a 12% increase in T_{SCWT} . In contrast, in [4], the authors show that a thickening of the gate from 50 nm to 85 nm allows the T_{SCWT} to be increased by 50% but at the cost of a more penalizing increase of 30% in $R_{\text{DSON}} \cdot \text{cm}^2$. Source region (N+) around the gate is also an interesting parameter. In [5], authors show that adjusting the doping downwards is the most efficient parameter to both increase the T_{SCWT} from 4 μs to 10 μs with a +20% penalty on $R_{\text{DSON}} \cdot \text{cm}^2$. Another approach is to redesign the gate shape. In [6], authors show that an adapted trench gate structure allows the maximum field amplitude and temperature level to be reduced to the same short circuit time as a planar gate. The time for which failure will be visible on such a device will therefore be higher, resulting in a more robust component. In [7], trench structure can also be completed by a so-called super-junction structure which amplifies the above properties with an increase of 10% to 50% of the T_{SCWT} at the cost of a very acceptable increase of the $R_{\text{DSON}} \cdot \text{cm}^2$. All these approaches are interesting in principle, to reach the best trade-off between T_{SCWT} and $R_{\text{DSON}} \cdot \text{cm}^2$, but they require a more expensive design and manufacturing effort than a standard design. So, in this paper, authors propose solutions to improve robustness based on standard and commercial components. In addition, a particular effort is made to finely analyze the device's degradation modes and specifically those that preserve the application's operating safety by avoiding a drain-source short-circuited state.

The SC performances and failure mechanisms of standard and commercial SiC MOSFET and Si IGBT have been discussed in different studies [8–10]. The SiC MOSFET mainly presents two failure mechanisms, under SC operations, both known as drain-source fail-to-open-circuit (FTO, or soft failure mode) and drain-source fail-to-short-circuit (FTS, or hard failure mode) [9,11,12]. Clearly, these signatures depend on the power density applied and then the temperature rise within the device. The FTS mode is derived from thermal runaway by the parasitic BJT p-well region triggering the loss of the turn-off and the failure of the chip. On the other hand, the specific FTO mode; which is by far the preferred mode; results at $V_{\text{GS}}^{\text{FAILED}} < V_{\text{GSTH}}$ leading to transistor shutting off, an intrinsic fault self-containment capability with enabling the system safe operation without complex or costly auxiliary components. This failure mode can be due mainly to the progressive ILD (Internal Layer Dielectric) cracks, fusion, and diffusion of the Al top metal, leading to the partial shorting of the gate and source terminals. This is related to extreme thermo-mechanical stresses and heat in SC between the polysilicon gate and the Al source.

In this context, a direct approach to make commercial SiC MOSFET more robust and safer is to reduce the power density applied to the chip, either by the drain voltage depolarization or by the gate voltage depolarization. In [13], authors present an analysis of the main parameters V_{DS} bias, V_{GS} bias, and R_{G} (external gate resistance) on short-circuit electrical stresses with an estimation of the transient chip temperature based on a TCAD model. Parameter V_{DS} bias is the most important one to reduce the temperature, but the authors do not present any estimate or measurement of the corresponding T_{SCWT} and no consequence on the failure modes. In [14], authors propose a fairly comprehensive exploration of the reduction of V_{GS} and V_{DS} from 800 V to 400 V in planar and trench

structures. At 800 V V_{DS} bias, authors show that the FTS mode cannot be avoided and that a V_{GS} depolarization from 15 V bias to 12 V bias increases T_{SCWT} by 40%. At 600 V V_{DS} bias, T_{SCWT} increases by 53% and the FTS mode can be neutralized to leave the FTO mode visible, provided that the channel turn-off is reinforced with a V_{GS} bias of -10 V instead of -5 V. Finally, authors also show that at 400 V V_{DS} bias, both structures exhibit a FTO mode with a 250% higher T_{SCW} . However, although interesting, this article does not detail the degradation mechanisms of the gate.

This paper aims to present different failure mechanisms of a recent, second generation, ST-Microelectronics™ device 1200 V, 75 mΩ, 33 A @ $T_{case} = 25$ °C planar-gate type device, in an automotive-grade 3-lead TO247 case [15], under incremental-pulse short-circuit behavior. The DC testing voltage was at nominal and reduced 600 V operation instead of standard 800 V used in extreme short-circuit assessment. The impact of gate-source decreased from 18 V to 10 V is also analyzed on the T_{SCWT} and $R_{DS(on)}$ trade-off.

In contrast to the state-of-the-art literature, we will pay particular attention to the mechanisms and failure modes specific to the SiC MOSFET under reduced or depolarized voltage conditions, in particular the properties that preserve the electrical safety of the device and the absence of drain-source short-circuit.

The paper structure is divided by two main approaches: the drain-source voltage V_{DS} depolarization and gate-driver voltage V_{Drv} depolarization. Each section will discuss both the drain-source voltage and the gate-driver voltage depolarization. The first section is focused on the short-circuit electrical behavior under incremental pulse width, whereas the second section is focused on the electrical effect after the first failure. The paper points out the effect of progressive gate-damage accumulation, by discussing observations over thermal and energy dissipation. It will show that this specific SiC MOSFET mechanism can be easily detected to self-protect the device with a feedback on the gate-driver. Moreover, the authors studied the depolarize on-state gate-drive voltage sufficiently to reduce the chip heating-rate and thus increasing the robustness of the short-circuit withstand time above 10 μs, as in silicon, without the risk of thermal runaway [16].

2. Short-Circuit Stress Analysis

2.1. Applied Stress and Power Test Bench

In order to electrically identify and characterize the device short-circuit withstand time, short-circuit energy, and failure mechanism, the device was placed under extreme short-circuit mode; which is known as Hard Switch Fault HSF [16]. The DUT (Device Under Test) was placed on the low side of a phase-leg power test bench presented in Figure 1. On the high side of the power test bench, a connection was made between the drain and source electrode of the upper device of the leg by using a copper line in order to simulate the HSF short-circuit behavior. The power test bench presented in Figure 1 was supported by a fast high current electronic breaker and safety fuses, to limit the final damage of the device from a possible physical explosion. The power test bench also consisted of an adapted gate driver with on-state and off-state adjustable voltage, controlled by an FPGA (field programmable gate arrays) and a touch screen, in order to ease the short-circuit test manipulation.

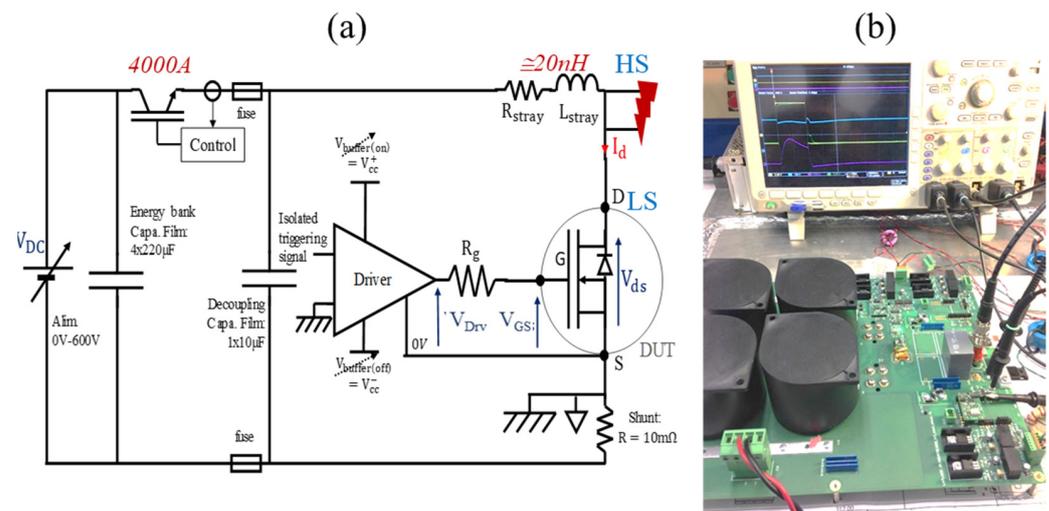


Figure 1. (a) Schematic view of the power test bench used for short-circuit test. (b) V1-2018 Laplace Laboratory test-bench: Max 600 V, 400 A, 100 μ s, 125 $^{\circ}$ C.

One should note, there is a straightforward relationship between the power density in short-circuit operation and the maximum temperature (1) [17]. This relationship can help to easily identify different features about the DUT. This relation assumes a homogeneous surface density on the top of the chip which is well suited to the case of the SiC MOSFET. Indeed, its epitaxy is thin and highly doped compared to silicon device, with a strong gradient of narrow field, very close to the chip surface. Moreover, ref. [9] presents that both failure modes depend on the temperature increase and the growth rate within the device. In order to avoid a fast critical FTS failure, the temperature increase within the device should be controlled or limited. One can use Equation (1) to decrease the junction temperature by decreasing the power density. The power density can be decreased either by decreasing the drain voltage V_{DS} , or by decreasing the density of saturation current by depolarizing the gate-drive voltage V_{Drv} . This paper presents both methods. The first approach was decreasing the drain voltage by using 600 V DC bus voltage instead of the nominal 800 V used in application. The second approach was to further decrease the power density by V_{GS} depolarization.

$$\Delta T_{jmax}(t) = \frac{2 \times V_{DS} \times J_{sat}}{\sqrt{\rho c_p \lambda \pi}} \sqrt{t} \quad (1)$$

where r is the density of SiC, c_p is the specific heat of SiC and l is the thermal conductivity of SiC. V_{DS} is the drain-source voltage. J_{sat} is the saturation channel current. t is the transient time, proportional to short-circuit time in our case.

2.2. DC Voltage Depolarization Method

2.2.1. Failure Mode Sequences for a Given Device

Sequence 0:

The applied test is a successive incremental short-circuit pulse with an initial pulse of 0.5 μ s and a step of 0.25 μ s, until the device reaches its physical destruction. Different DUTs have been tested. For this study, seven components have been tested. The test is under a nominal V_{Drv} (−5 V/18 V) driving with a gate resistor $R_G = 47 \Omega$ and a reduced $V_{Bus} = 600$ V. The DUT was designed for 1.2 kV compared to $V_{Standard} = 2/3 \times 1200$ kV = 800 V, which is the specified range of the maximum transient bus voltage typically in reverse operation of automotive power train. The R_G gate resistor is deliberately chosen to be high in order to avoid turn-off power surges and voltage spikes instead of using a dedicated soft turn-off circuit. Moreover, in this study this gate resistor is used to ease local measurement of dynamic, temporal gate leakage $I_{GS}(t)$. Most of the figures are oscilloscope views

illustrating V_{Drv} , V_{GS} , V_{DS} , I_D , and I_G . The gate current I_G is given by the difference between V_{Drv} and V_{GS} divided by the gate resistor.

Figure 2a presents preliminary oscilloscope view at $t_{Pulse} = 1 \mu s$ of the device number #3. This figure is introduced in order to get familiarized with a single pulse waveform. Figure 2b illustrates the incremental short-circuit test. The gate current illustrated is a cropped view of the whole signal, the positive and negative current peaks are not illustrated; only to enhance and amplify the current leakage signal if illustrated. Each component is led to its final destruction. During the test run, different failure modes and degradations have been noticed.

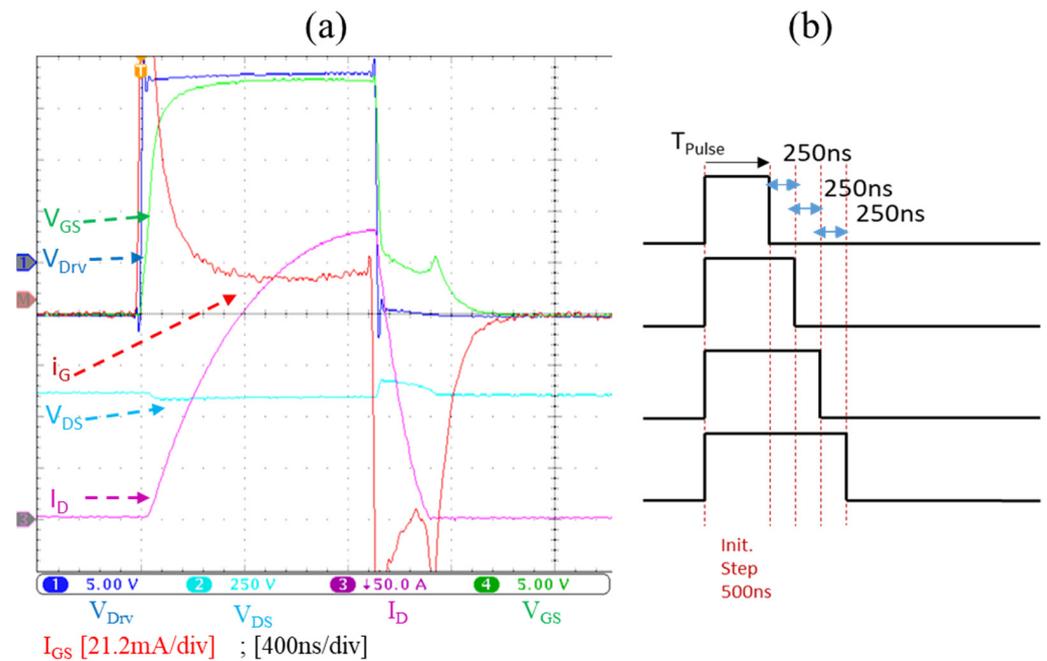


Figure 2. (a) Oscilloscope waveforms at $1 \mu s$ of the DUT #3 under HSF, @ $V_{DS} = 600 V$, $R_G = 47 \Omega$, $V_{Drv} = -5 V/18 V$. (b) Applied control SC signal test.

Sequence 1:

After several incremental pulses, the first degradation that has been noticed is that V_{GS} starts to slightly decrease (point I. in Figure 3); (green waveform, Figure 3 at $3.5 \mu s$ for DUT #3). This behavior is conditioned by electric field stress in the oxide combined with high temperature in the gate-oxide caused by extreme power density applied, in the channel and the JFET regions [18]. This behavior is known by the gate current-leakage, (point II. In Figure 3). The physical origin of the gate leakage-current is still under study by the authors, but it is strongly assumed to be related to indirect tunneling effect at medium electric field and high temperature (Schottky emission). In Figure 3, the V_{GS} drop is directly translated to an ohmic drop which is a high gate leakage current through the external gate resistor 47Ω , as illustrated in the red waveform (I_G). This non-permanent and transient gate leakage current is a great marker in order to detect the presence of a short-circuit, as also suggested in [19,20].

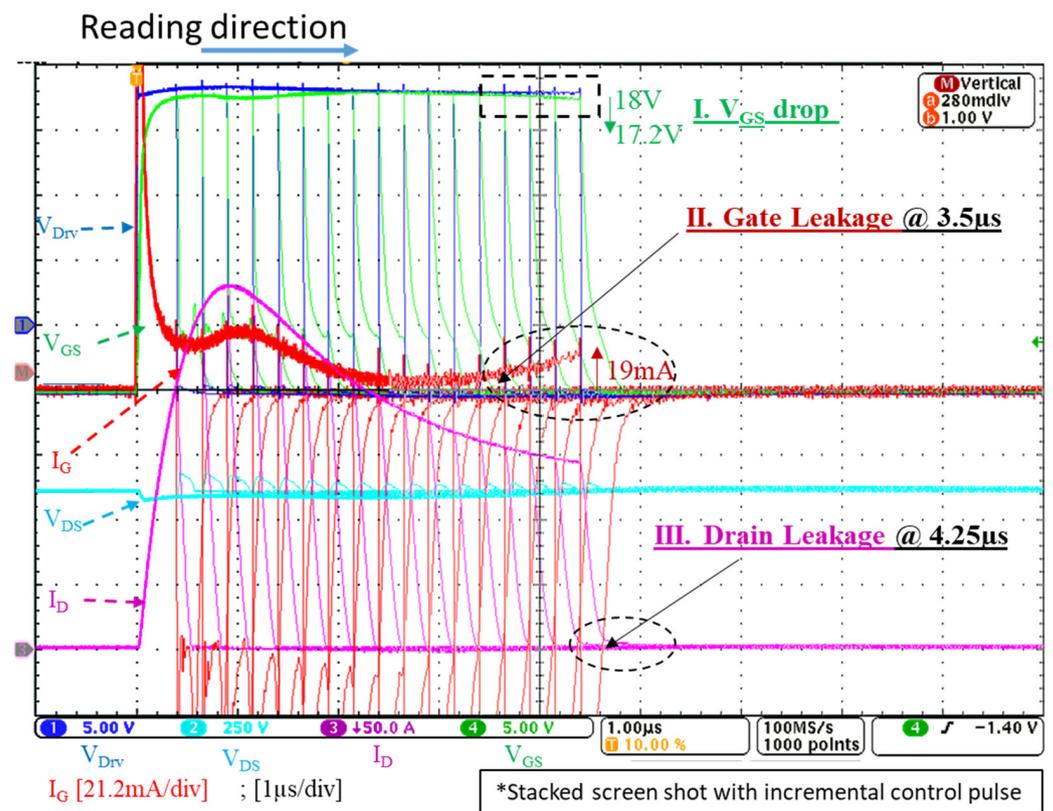


Figure 3. Stacked incremental pulse duration oscilloscope waveforms from 0.5 μ s to 4.5 μ s with a step of 250 ns. @ $V_{DS} = 600$ V, $R_G = 47 \Omega$, $V_{Drv} = -5$ V/18 V, DUT #3.

Sequence 2:

Afterwards, the pulse duration increases, therefore an increase in the temperature, eventually leads to a significant drain current leakage increase (point III. In Figure 3); known as the current tail [21]. This drain leakage is visible in Figure 3 at 4.25 μ s.

As the pulse length gets longer, V_{GS} drop becomes significant, which helps reduce the dissipated power and brings the device to a less thermal stable point. This can result in a delayed thermal runaway. Moreover, the high temperature during SC events exerts thermo-mechanical stresses to the oxide due to a significant misalignment between thermal expansion coefficients α_{AL} and α_{SiO_2} (ratio ≈ 40) [22]. In this case, with lower V_{DS} , the DUT goes into a partial and delayed gate damage as shown in Figure 4, which is an irreversible phenomenon, (point IV. & V. in Figure 4).

The delayed crack [22] as presented in Figure 4 is probably due to a mechanical time constant plus the penetration duration or the diffusion of the metal in the cracks.

As presented in Figure 4 when the pulse duration reaches 5.25 μ s, the gate-source voltage shows a depolarization from -5 V to -4 V (point V. in Figure 4), after 5 μ s delay, which is translated by an increase in the gate current leakage. Furthermore, The DUT presents an appearance of a first failure mode, known as a soft gate damage.

The gate failure seems to be a reaction of a transient electro-thermal-mechanical process. In order to study this first failure mode in depth, a cell-level 1D thermo-metallurgical simulation is presented in the fourth section. This failure behavior can be the outcome of the increase of the temperature resulting into aluminum melting and stress on SiO_2 which exceeds its mechanical stress [23].

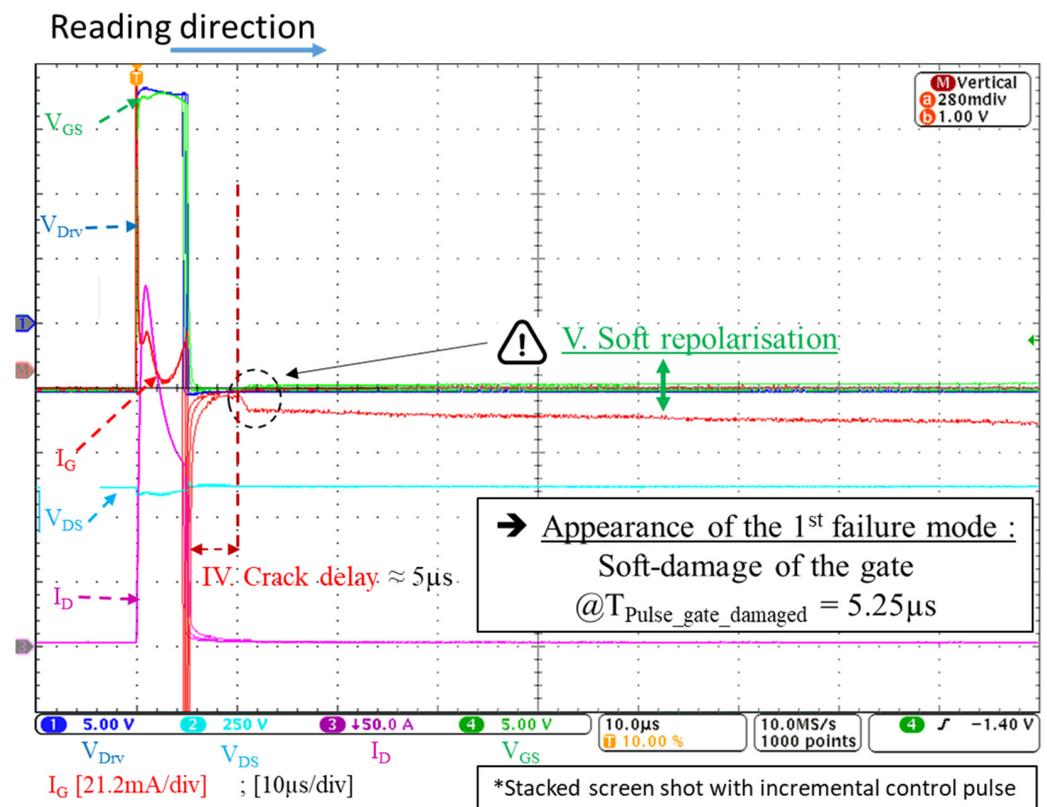


Figure 4. Continuity of the stacked incremental pulse duration oscilloscope waveforms from 4.75 μs to 5.25 μs with a step of 250 ns. @ $V_{DS} = 600\text{ V}$, $R_G = 47\ \Omega$, $V_{Drv} = -5\text{ V}/18\text{ V}$, DUT #3.

Sequence 3:

After the appearance of the first partial gate damage, the next pulse; which is 250 ns longer than the previous one (5.25 μs); clearly indicates the confirmation of a permanent partial gate damage (point V. in Figure 5). The waveforms show that V_{GS} is softly depolarized from 18 V to 15 V and from -5 V to -4 V . Moreover, I_{DMax} is significantly reduced (point VII. in Figure 5), as well as the power density. These reductions allow the device to support few more short-circuit pulses, and allowing the temperature and the power density within the device to be furthermore increased. On the other hand, the gate current leakage is increased, and will remain very high for future pulses.

However, such a high level of permanent gate-current leakage or gate-voltage collapse can be easily detected by the driver. This property can be used to locally self-turn-off the device to prevent it from getting too close to its critical failure mode, FTS [19,24].

Sequence 4:

Afterwards, the device was exposed to longer and longer pulses duration, Figure 5. In the process the device showed more and more drain leakage (point VII. in Figure 5), again with an increase on the temperature and the power density, which brought the device to a second gate damage (point VI. in Figure 5). This resulted in a reduction of the drain leakage tail (point VIII. in Figure 5), and further depolarization of V_{GS} (point VI. in Figure 5). This pushed the device to a further extreme operational point, and continued until the device reached a final critical failure, FTS @7.5 μs (point IX. In Figure 5).

These different post cracks were a clear marker of a permanent physical degradation of the device. Different studies show the presence of the gate damage failure mode [25,26], and the successive degradations [27]. However, some authors have shown that it is also possible to partially restore the gate-integrity by a dedicated original gate-bias procedure, in off-line operation, provided that the gate is not totally cracked [28].

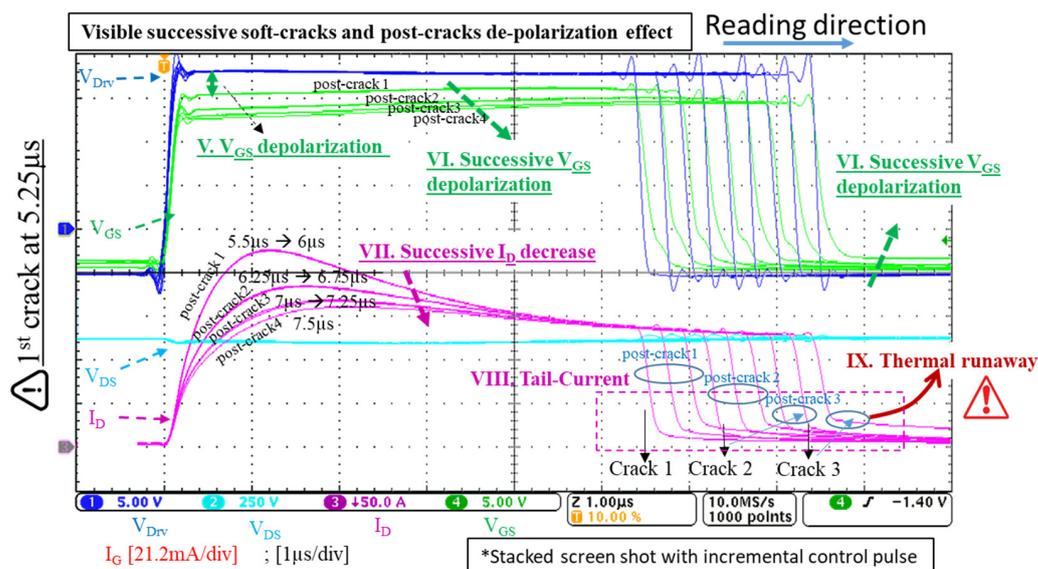


Figure 5. Continuity of the stacked incremental pulse duration oscilloscope waveforms from 5.5 μ s to 7.5 μ s with a step of 250 ns. @ $V_{DS} = 600$ V, $R_G = 47 \Omega$, $V_{Drv} = -5$ V/18 V, DUT #3, 1st SC test. (NB: gate damage at 5.25 μ s).

2.2.2. DC Voltage Depolarization Method under Several Devices

The sequences in the section above and the study of different devices helped to illustrate the timeline presented in Figure 6. The timeline presents, the appearance of gate and drain leakage as well as the gate damage failure and the final failure FTS respectively.

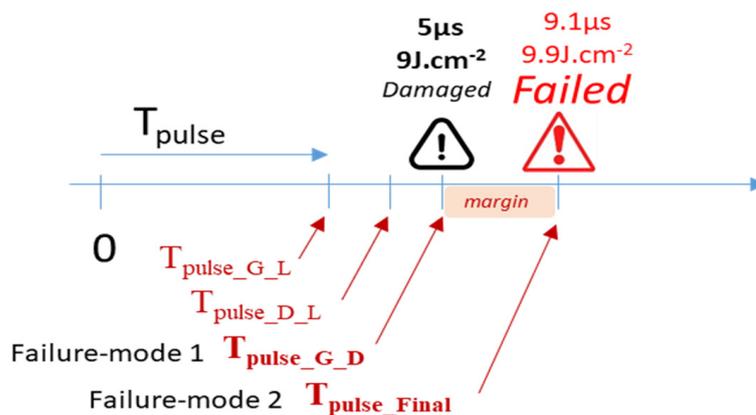


Figure 6. Timeline illustration exhibiting the main pulses: G_L, gate_leakage; D_L, drain_leakage; G_D, gate-damage; FTS, pulse_final.

The incremental pulse duration test is applied on different devices separately. After the gate-damage, each device shows its unique crack behavior and depolarization amplitude; regarding the decrease of the drain current I_D and the amplitude depolarization of V_{GS} . Moreover, the number of post-cracks differs from a device to another, where it can be one crack or up to four cracks, as illustrated in Figures 5 and 7.

For a large scope of study, different tests have been applied on different devices:

- Different SC initial pulse duration:

Oscilloscope waveforms of a different device are presented in Figure 7. The applied test on this device was only different by its initial pulse. This initial pulse duration time was 3 μ s instead of 0.5 μ s. The purpose of this applied test was to see the effect of the gate-damage time by reducing the early stress on the device. One should note that the degradation of the device was not noticed when a pulse longer than the average gate-

damage pulse (5 μs) was applied to a non-stressed device. Figure 7 presents the behavior of the DUT #4 after gate damage which occurs at 5 μs . Similar behavior has been noticed for those devices with a different initial pulse. As the one can see; after the presence of gate damage (point V.); the presence of point VI., VII., VIII., and IX. are visible with different amplitude.

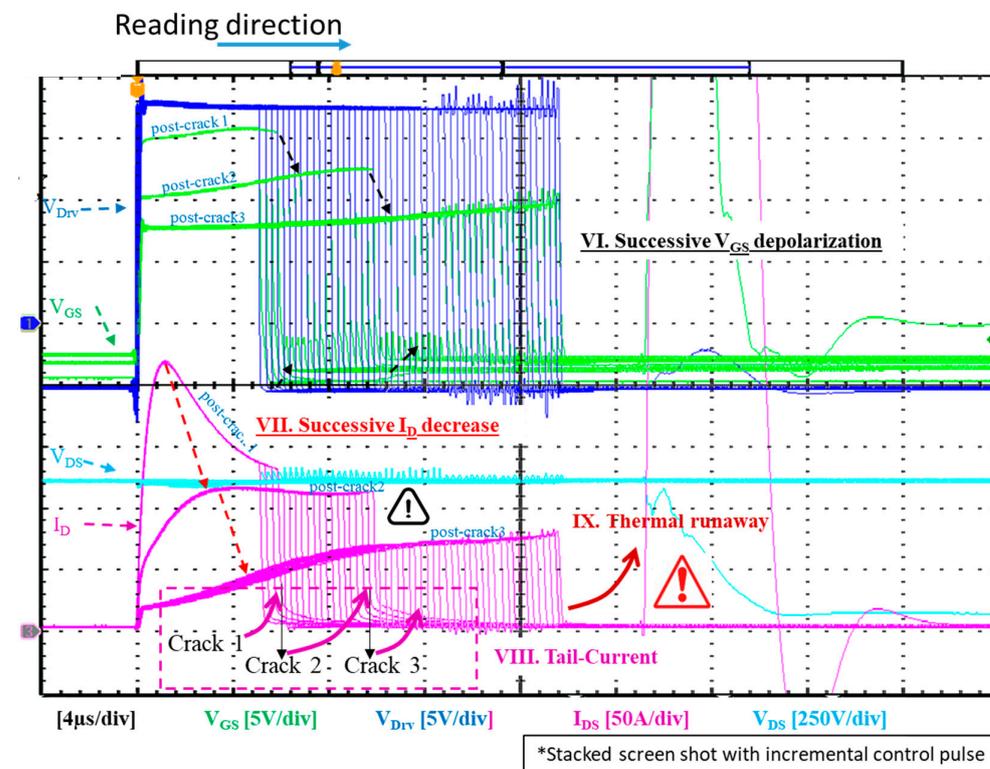


Figure 7. Stacked incremental pulse duration oscilloscope waveforms from 5.25 μs to 17.75 μs with a step of 250 ns. @ $V_{DS} = 600\text{ V}$, $R_G = 47\ \Omega$, $V_{Drv} = -5\text{ V}/18\text{ V}$, DUT #4, 2nd SC test. (NB: gate damage at 5 μs).

- Long SC pulse:

In the case where the pulse width equaled 110% of the gate-damage pulse or longer, the device went directly to a critical failure mode, FTS. The device had no time to consolidate the gate-damage behavior, therefore there were no visible cracks and no SC cycling capability. It could be due to the absence of the non-visible cracks, or fatigue, and no partial degradation before reaching certain energy amount.

Different key parameters of several devices are presented in Table 1. The appearance of the gate damage was reproducible around 4.75 μs and 5.25 μs , contrary to the FTS failure mode. Moreover, the case temperature has no clear influence on the gate-damage failure time.

Table 1. Different key parameters of several devices.

DUT	#2 @ 25 °C	#3 @ 25 °C	#4 @ 25 °C	#6 @ 25 °C	#16 @ 125 °C	#19 @ 125 °C
Test	1st Test	1st Test	2nd Test	1st Test	1st Test	1st Test
V_{GS_th} [V]	3.85	3.31	3.27	2.89	3.06	2.99
$T_{Pulse_G_L}$ [μs]	3.5	3.5	3.5	3	3.75	3.5
$T_{Pulse_D_L}$ [μs]	4.25	4.25	3.75	3.75	4.75	4.25
$T_{Pulse_G_D}$ [μs]	4.75	5.25	5	4.75	4.75	5

Table 1. Cont.

DUT	#2 @ 25 °C	#3 @ 25 °C	#4 @ 25 °C	#6 @ 25 °C	#16 @ 125 °C	#19 @ 125 °C
$T_{\text{Pulse_Final}}$ [μs]	8.75	7.5	17.75	6.5	NA	5
$I_{\text{D_Max}}$ [A]	260	285	285	320	245	270
E_{Final} [mJ]	NA	606	592	581	NA	504
$E_{\text{Final}} \cdot \text{cm}^{-2}$ [$\text{J} \cdot \text{cm}^{-2}$]	NA	10.1	9.87	9.68	NA	8.40
Crack Delay [μs]	2.4 μs	5.5 μs	5 μs	4 μs	>4.25 μs	6.25 μs
Pulses Nb. before Damage	18	20	9	18	18	19
Failure Type	GD + FTS	GD + FTS	GD + FTS	GD + FTS	GD + FTS	GD followed FTS

2.3. Gate Voltage Depolarization Method

This section is dedicated to the second depolarization method. This method is based on the direct decrease of V_{Drv} voltage. Figure 8 shows the results of short circuit tests carried out on the DUT #8 under ($V_{\text{DS}} = 600 \text{ V}$, $V_{\text{Drv}} = 10 \text{ V}$) using a direct depolarization of V_{GS} ; bringing the maximum short-circuit current from 250 A; observed for DUT #4; to less than 115 A; for DUT #8 (i.e., 50% reduction with a more softened form).

An increase in the T_{sc} with a theoretical ratio close to four ($\times 4$) is to be expected, according to Relation (1) and considering an invariant failure temperature threshold between the two bias modes of the gate voltage, (quadratic effect between T_{sc} and power density).

Indeed, it can be observed that direct depolarization of V_{GS} method showed promising results exhibiting a T_{SC} equal to 16 μs ; compared to 5 μs for DUT #4. This confirmed the previous analysis while being slightly less advantageous. However, the method allowed exceeding 10 μs (standard for IGBT device), with the appearance of FTO mode under a V_{DS} close to the nominal value.

Figure 8. presents the first failure mode (gate damage or partial FTO), which occurred around 11 μs , and the full FTO failure, which appeared at 16 μs (point X. in Figure 8). The impact of a direct V_{GS} depolarization on $R_{\text{DS-ON}}$ is illustrated in Section 3.2.

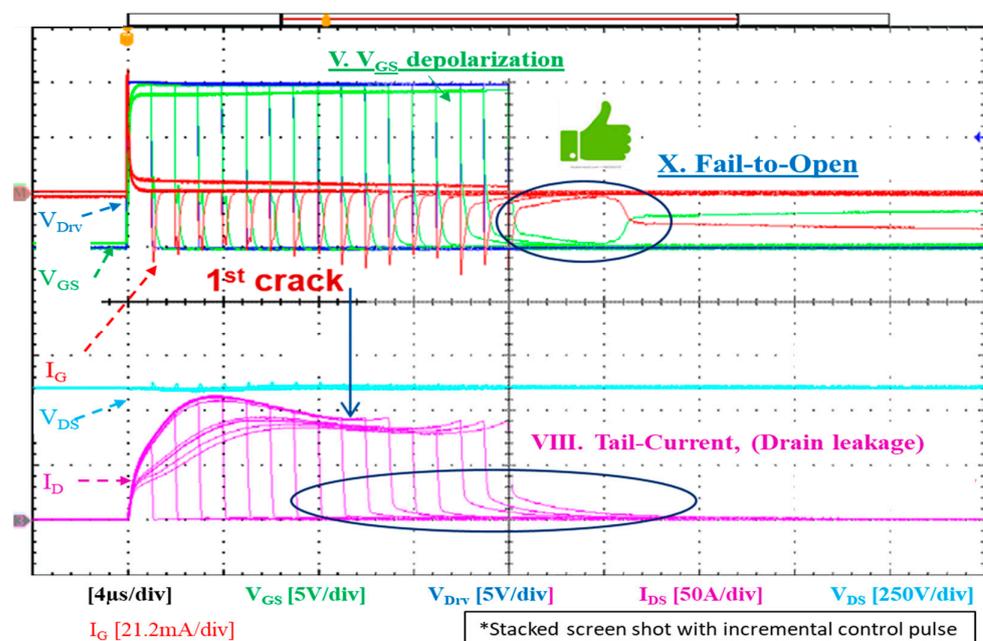


Figure 8. Stacked incremental pulse duration oscilloscope waveforms from 1 μs to 16 μs with a step of 1 μs . @ $V_{\text{DS}} = 600 \text{ V}$, $R_{\text{G}} = 47 \Omega$, $V_{\text{Drv}} = -5 \text{ V}/10 \text{ V}$, DUT #8.

3. Electrical and Structural Analysis

3.1. Energy Study under Short-Circuit

The gate damage and the degradation that followed on the device can be seen and interpreted from the energy dissipated in the device. The degradations were translated by several post-cracks. The energy dissipated (E_{Dis}) inside the DUT was calculated from the V_{DS} and I_D waveforms captured during the SC phase by integrating $V_{DS} \times I_D$ over the duration of the SC pulse $T_{SC-Pulse}$ (2).

$$E_{Dis} = \int_0^{t_{SC-Pulse}} V_{DS} \times I_D dt \quad (2)$$

Figure 9a,b present the short-circuit energy of the DUT #3 and DUT #4 respectively. The figures perfectly exhibit the depolarization dips of the device and the presence of the successive gate damage including the amplitude of the cracks. The DUT #3 shows at the 1st appearance of the gate damage that the dissipated energy was reduced from 556 mJ to 534 mJ allowing the device to withstand more temperature increase. The same reduction could be noticed for the cracks that followed. Similarities to this behavior are also reproducible for different DUT, as presented in Figure 9c for the DUT #6.

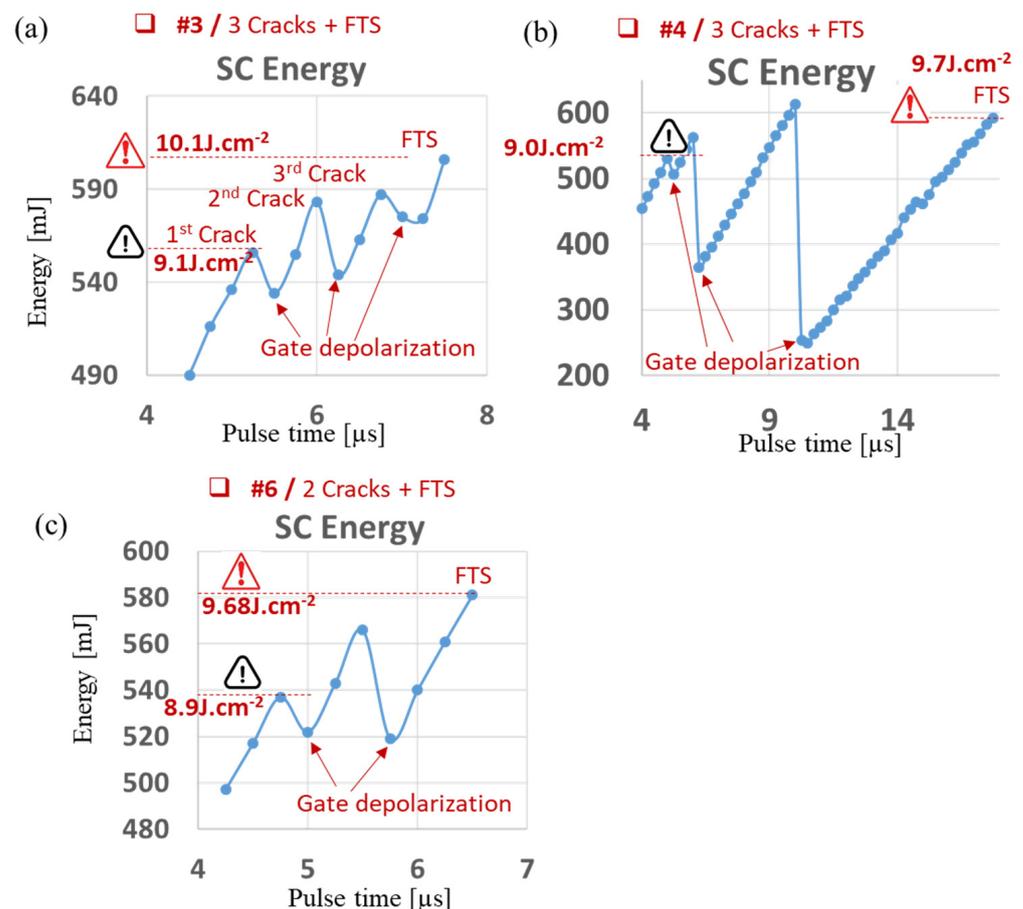


Figure 9. Energy dissipated for each incremental pulse test, exhibiting the failure energy behavior. (a) DUT #3, (b) DUT #4, (c) DUT #6, @ $V_{DS} = 600$ V, $R_G = 47 \Omega$, $V_{Drv} = -5$ V/18 V.

For all DUT tested the gate-damage occurred between 530 mJ and 550 mJ. On the other hand, the FTS occurred between 581 mJ and 606 mJ. The robustness margin was small between the soft gate-damage and the hard failure mode. This small margin was visible when 110% of the gate-damage pulse was applied on an unstressed device; exhibiting directly an FTS.

From Figure 10, one can estimate that improving the gate, i.e., by increasing the mechanical strength of the ILD using a material other than SiO₂, might slightly increase the apparent withstand time from 5.25 towards 5.75 μ s, emphasizing a critical failure “FTS” under a nominal V_{GS} bias. This improvement will hide the gate-depolarization phenomena therefore avoiding the safe failure mode. In contrast to the safe damage behavior at 5.25 μ s, the device still has switching capability (where V_{GS} is de-polarized, and the device only softly damaged and not destroyed).

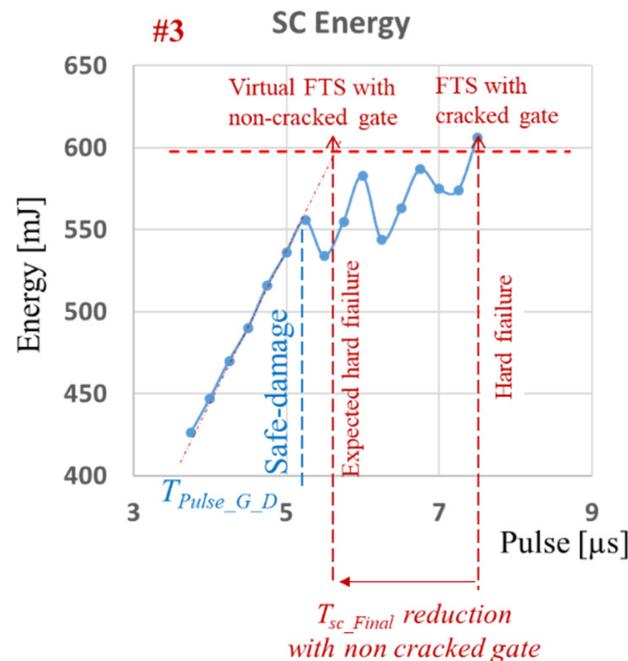


Figure 10. Estimated behavior from the energy extrapolation.

3.2. R_{DS-ON} Analysis

The occurrence of the first crack led to a depolarization of the gate voltage, which is reduced by few volts at most. Figure 11 shows that this depolarization affects the R_{DS-ON} increase by no more than 10%. In general cases where conduction and switching losses are equal, this penalty on the R_{DS-ON} will only impact the total losses by 5% which is very reasonable. However, this result has to be considered on a case-by-case scenario depending on the design of the component and the shape of its I_D (V_{DS}) characteristic.

If this first crack is detected by the driver and the fault is inhibited, the same component can be reused without having to be replaced. However, the gate-driver supply must feed a permanent current overload of several tens of mA. An excess of power to be transferred to the gate which can reach +1 W in the driver power supply. This over-supply is significant and should be taken into account at the design stage. Furthermore, this over-supply can also be used as a means of detecting the occurrence of a hard crack to manage the shutdown of the converter and then the replacement of the component at the appropriate time regarding the mission profile.

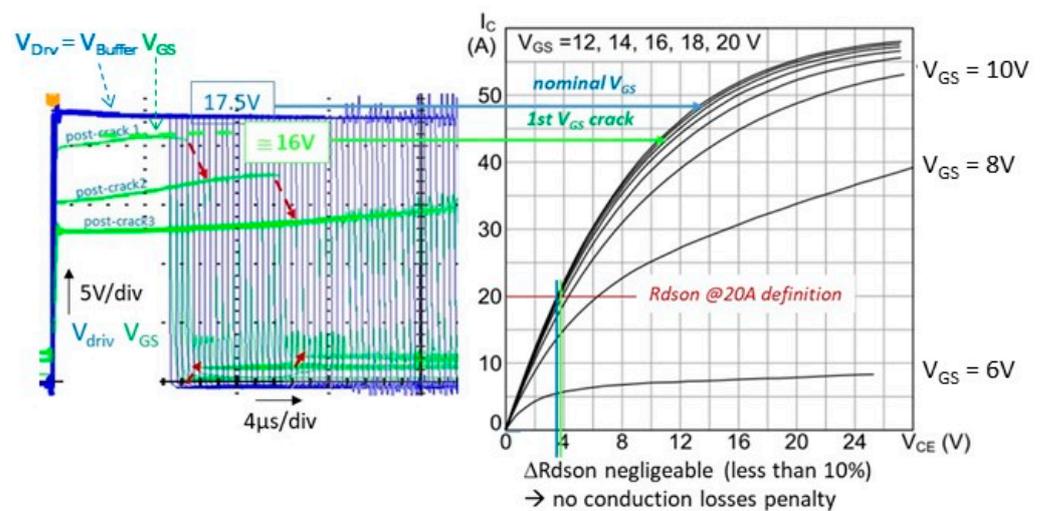


Figure 11. Gate-crack impact on R_{DS-ON} increase using V_{DS} depolarization.

The gate depolarization described in Section 2.2.1 obviously also involves an increase in R_{DS-ON} . However, this penalty is more acceptable for the SiC MOSFET because this component has a channel resistance that decreases at intermediate temperatures (up to 300 °C) compared to the other series resistance components R_{JFET} and R_{DRIFT} . This effect is related to Coulomb-like mobility through scattering of ionized impurities. As the channel resistance becomes of majority value in depolarization mode, this property gives an overall resistance that is more temperature stable than a silicon MOSFET. For the DUT studied in this paper, $R_{DS-ON}(V_{GS})$ is drawn in Figure 12 and points out an increase of 23%. In the general case, conduction and switching losses are equal, this penalty on the R_{DS-ON} will only impact the total losses by half (11.5%) which is acceptable.

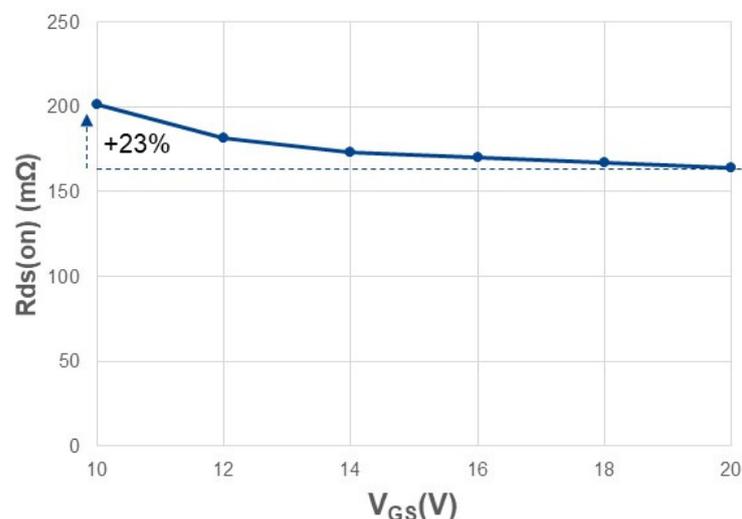


Figure 12. $R_{DSon}(V_{GS})$ under V_{Drv} depolarization @ $I_D = 20$ A, $T_{CASE} = 200$ °C from Data-Sheet device SCTW40N120G2VAG; <https://www.st.com> (accessed on 25 November 2021).

4. Thermal 1D Simulation Analysis

In order to support the gate-damage analysis, thermal modelling and simulation of the chip temperature were carried out, as detailed in [29]. The model takes into account the temperature dependence of the conductivity and the specific heat of SiC and aluminum, as well as the solid–liquid phase transition of the Al top layer. Using structural computer aided design tools (Comsol™ was used in this case), a cell-level 1D_x/Ex—electric field, J_x—current density model was carried-out. The software receives as input the current waveform

$I_{DS}(t)$ of the DUT #4 from the experimental bench at a constant voltage $V_{DS} = 600$ V and $V_{GS} = 18$ V/−5 V.

Figure 13 shows the temperature rise at $T_{pulse_G_D} = 5$ μ s of all the main layers of the chip during the short-circuit. After only 3 μ s, it is visible that the Al layer was above its melting point with a high thermal energy injected into its liquid phase. Moreover, according to [29], at the Al melting temperature, the thick oxide was probably already cracked because the mechanical stress exceeded its mechanical strength which is confirmed previously by the gate-crack electrical observation on Figure 6. The final and maximum temperature in the chip was evaluated by simulation at 1280 °C. This value remained lower than the polysilicon level fusion (1400 °C), SiO₂ level fusion (1700 °C) and nitride passivation layer Si₃N₄ (1900 °C). Then, all these material regions should not be severely damaged up to 5 μ s short-circuit operation.

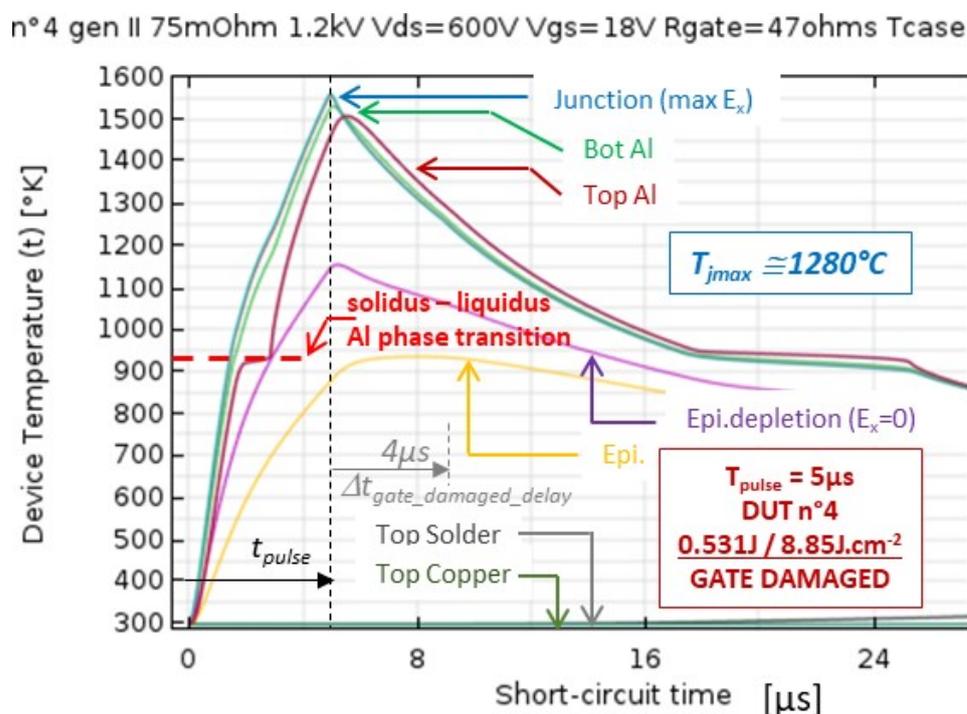


Figure 13. 1D chip temperature simulation in short-circuit operation for $V_{DS} = 600$ V, $V_{Drv} = -5$ V/18 V, $R_G = 47$ Ω , $T_{Pulse} = 5$ μ s, $T_{case} = 25$ °C.

In order to explain the physical origin of FTO failure mode; Figure 14 illustrates the electro-thermal simulation of DUT #8, a device that had undergone a gate depolarization method; $V_{Drv} = 10$ V. The simulation shows that the temperature on the top layer of the Al reached the start point of the metallurgical phase transition (solid-liquid) around 8 μ s, i.e., more than twice the delay time of DUT #4. The temperature of the top Al layer starts rising again and follows the thermal dynamics of the junction after about 8 μ s of stable phase.

The final and maximum temperature in the chip is simulated at 1242 °C, which is only 3% lower than in case DUT #4, while the short-circuit pulse times are in a ratio of 3.2 (5 μ s vs. 16 μ s). It seems therefore that this threshold temperature could be a salient indicator of the onset of the gate degradation mechanism.

After the end of the pulse, it is clearly seen that the temperature at the bottom Al layer became lower than the temperature at the top Al layer: the metal layer restituted thermal energy in a liquid state. When the temperature reached the phase transition zone, the heat sink reactivated and considerably reduced the thermal dynamics of the bottom Al layer and the junction. Afterwards, the accumulated energy was released during the following microsecond, leading to the solidification of the whole Al layer. Through a thermo-mechanical stress point of view, it is obvious that the estimated temperature of

the metal top was above 600 K, which led to the mechanical rupture of the ILD—SiO₂ to 1.4 GPa, by compression to the Al layer on the top of SiO₂ [29].

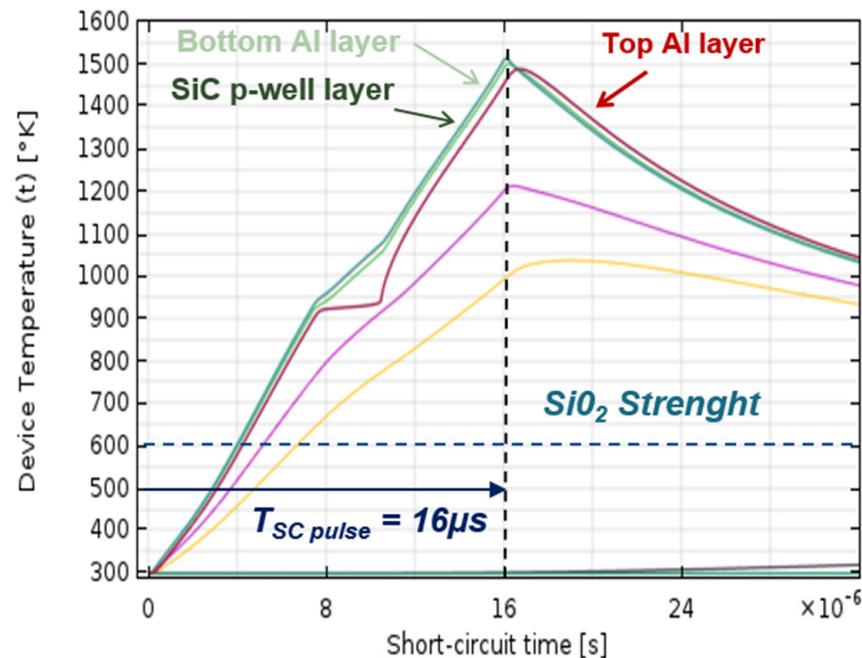


Figure 14. Estimated temperature of the main chip layers under Comsol for the DUT #8 at $V_{DS} = 600$ V, $V_{Drv} = -5$ V/10 V and $T_{case} = 25$ °C at $T_{SC} = 16$ μ s.

5. Discussion

In order to fully understand the effect of both depolarization methods (V_{GS} and V_{DS}) a comparative study is presented in Table 2, including results of the same rating device under nominal conditions at $V_{DS} = 800$ V [15]. As one can see, under nominal conditions the device withstands around $T_{SCWT} = 1.62$ μ s; with a critical FTS mode. On the other hand, using V_{DS} depolarization method, the device withstands around $T_{SCWT} = 4.9$ μ s, with a safe failure mode (gate damage). Finally, using V_{GS} depolarization method, the device withstands around $T_{SCWT} = 9.6$ μ s, which is close to what the IGBT standard T_{SCWT} (10 μ s), with the same safe failure mode and only a 23% R_{DSON} increase. Overall, we can note that the damage or failure temperature was decreased ⁽¹⁾ from one method to another; (respectively: 1320 °C, 1207 °C, 1056 °C); which allowed the device to withstand more the SC; (respectively: 1.62 μ s, 4.9 μ s, 9.6 μ s). It is also remarkable to note that the damage mode corresponding to the strong degradation of the gate ⁽²⁾ is well associated with comparable temperature values for V_{DS} and V_{GS} depolarization (respectively: 1207 °C and 1241 °C ⁽²⁾). The gate leakage on the other hand is not visible under V_{GS} depolarization, ⁽³⁾, Table 2).

The experimental observations on the gate voltage in short-circuit operation and the thermal simulations make it possible to establish relevant correlations: A threshold temperature between 1200 °C and 1300 °C seems to correspond to a limit of use of the component. This is an interesting result, although it is to be expected that the duration of the pulse (total and after the melt time) will have an influence on the level of gate-damage its repetitive short-circuit cycles capability, but this last point is a research prospect for single pulse test and repetitive pulses. However, even if this threshold is exceeded, the gate-damage mode remains soft and progressive: it can be easily detected and managed by monitoring the gate voltage at the buffer output or indirectly by oversupply. The depolarization of the gate voltage from 18 V to 10 V allows the short-circuit withstand time to reach the usual 10 μ s which is a standard for IGBT technology which is still the most common power device in medium and high power. This property can be inexpensive on losses, depending on the case, it also allows considerably the reduction of the level of electric field stress on the gate oxide and improves reliability on long term operation.

Table 2. Average key parameters between V_{DS} and V_{GS} depolarization compared to nominal operating conditions [15].

Conditions	[15]		V_{DS} Depolarization Method		V_{GS} Depolarization Method	
	Time [μ s]	T° [C]	Time [μ s]	T° [C]	Time [μ s]	T° [C]
	$V_{Bus} = 800$ V, $R_G = 4.7$ Ω , $V_{GS} = -5$ V/+18 V		$V_{Bus} = 600$ V, $R_G = 47$ Ω , $V_{GS} = -5$ V/+18 V		$V_{Bus} = 600$ V, $R_G = 47$ Ω , $V_{GS} = -5$ V/+10 V	
$T_{Pulse_G_L}$	-	-	3.25	917	N.V. ⁽³⁾	N.V. ⁽³⁾
$T_{Pulse_D_L}$	-	-	4.25	1082	8.8	977
$T_{Pulse_G_D}$	-	-	4.9	1207 ^{(1),(2)}	9.6	1056 ⁽¹⁾
T_{Pulse_Final}	1.62	1320 ⁽¹⁾	9	Destroyed	16	1241 ⁽²⁾
E_{G_D} [mJ]	-	-	-	540	-	-
E_{Final} [mJ]	-	-	-	600	-	-
Failure mode	FTS		GD + FTS		GD + FTO	

N.V: none value, ⁽¹⁾ first light gate-damage or failure temperature, ⁽²⁾ hard gate-damage temperature, ⁽³⁾ N.V: none value.

6. Conclusions

Unlike silicon power MOSFETs, SiC devices showed different failure mechanism at reduced drain—source voltage 600 V compared to nominal 800 V for a 1.2 kV rating with nominal gate drive voltage. At 600 V the power density was decreased showing a succession of gate degradations as a non-catastrophic failure-mode. For the 75 mOhms studied device the gate damage occurs between 530 mJ and 550 mJ around 5 μ s which is perfectly reproducible. The gate damage produces a soft or hard depolarization on V_{GS} which keeps the thermal runaway further away. After the first crack, the device was operational with a small penalty on R_{DS-ON} . At the end, the device could withstand further longer short-circuit with successive cracks and gate depolarization which further reduced the power density to be dissipated. This SiC device also showed further robustness on short-circuit withstand time using a gate-drive voltage depolarization. This method also showed a first failure mode gate damage, and a final failure as a complete fail-to-open mode giving $V_{GS} < V_{GSTH}$.

These results complement and clarify many previous results obtained by the authors or their collaborators in SiC planar gate-MOSFET technology. This technology is the most widely used in SiC. The trench-gate structures are not considered in this paper because they are more complex to realize with more singular properties and with a more sensitive variation of the threshold gate voltage according to the gate polarization. It would require a more specific study in line with the perspective works of the authors.

Author Contributions: Conceptualization, Y.B., F.R. and W.J.; methodology, Y.B., F.R. and W.J.; software, Y.B.; validation, Y.B., F.R. and W.J.; supervision, F.R. and J.-M.R. All authors have read and agreed to the published version of the manuscript.

Funding: This work was made possible in large part by direct or indirect funding from the French National Research Agency (ANR). A large part of the results was obtained within the framework of the internal SiCRET “Silicon Carbide Reliability Evaluation for Transport” project Ref: CDP-E-001-068-V0 led by the Saint-Exupéry Institute of Technological Research in Toulouse (IRT SE).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Acknowledgments: We would like to thank Safran Tech™ division from Safran™ company and the Power Electronics team, in particular its leader Stéphane Azzopardi, for their scientific and financial support in the development of this topic and of part of the results obtained (part. Section 2.2.2).

Conflicts of Interest: The authors declare no conflict of interest.

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