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Shambo Mukherjee, Jacques Millo, Baptiste Marechal, Séverine Denis, Gwenhaël Goavec-Mérou, et al.. Digital Doppler-cancellation servo for ultra-stable optical frequency dissemination over fiber. IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, 2022, 69 (2), pp.878. 10.1109/TUFFC.2021.3125066 . hal-03454914

HAL Id: hal-03454914

<https://hal.science/hal-03454914v1>

Submitted on 5 Nov 2024

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Digital Doppler-cancellation servo for ultra-stable optical frequency dissemination over fiber

Shambo Mukherjee, Jacques Millo, Baptiste Marechal, Séverine Denis, Gwenhaël Goavec-Mérout, Jean-Michel Friedt, Yann Kersalé, Clément Lacroûte

Abstract

Progress made in optical references, including ultra-stable Fabry-Perot cavities, optical frequency combs and optical atomic clocks, have driven the need for ultra-stable optical fiber networks. Telecom-wavelength ultra-pure optical signal transport has been demonstrated on distances ranging from the laboratory scale to the continental scale. In this manuscript, we present a Doppler-cancellation setup based on a digital phase-locked loop for ultra-stable optical signal dissemination over fiber. The optical phase stabilization setup is based on a usual heterodyne Michelson-interferometer setup, while the Software Defined Radio (SDR) implementation of the phase-locked loop is based on a compact commercial board embedding a field programmable gate array, analog-to-digital and digital-to-analog converters. Using three different configurations including an undersampling method, we demonstrate a 20 m long fiber link with residual fractional frequency instability as low as 10^{-18} at 1000 s, and an optical phase noise of -70 dBc/Hz at 1 Hz with a telecom frequency carrier.

I. INTRODUCTION

With the joint progress of ultra-stable Fabry-Perot (FP) cavities, optical frequency combs (OFCs) and atomic optical standards, the development of optical frequency references has reached both an unprecedented level of performances and an advanced degree of industrial integration. While laboratory FP cavities have reached the 10^{-17} level [1]–[5], many transportable prototypes have been developed [6]–[9] and several companies have developed FP-based ultra-stable lasers. OFCs have also become a wide-spread laboratory tool, and transportable models have been demonstrated [10]. Optical atomic clocks have shown the same level of progress, with both optical lattice and single-ion clocks reaching the 10^{-18} accuracy level and below [11]–[15].

This progress in ultra-stable optical references impacts many fields, including time and frequency metrology, precision spectroscopy, microwave photonics [16] and fundamental physics [17], [18]. Several proposals have argued for the development of ultra-stable optical fiber networks on the continental scale [19], [20]. Such networks are already being deployed within national and international frameworks. In practice, ultra-stable optical links have been implemented at several scales, from the laboratory or campus [21], [22] to inner- and inter-city links [23]–[25] and beyond, with long-haul fiber links [26]–[29].

Such ultra-stable fiber links are based on a heterodyne Michelson interferometer in which one of the arms is shortened to exhibit length fluctuations as small as possible. The second arm includes the required length to transfer the optical signal to the end-user. The resulting beatnote phase fluctuations are directly related to the length difference fluctuations between the reference arm and the optical fiber link. If the length of the reference arm is stable enough, phase fluctuations detected with a photodiode at the interferometer output corresponds to the link optical length fluctuations caused by vibrations and thermal perturbations. From this signal an active loop filter generates a compensation signal to cancel the link phase noise. This is the so-called Doppler-cancellation scheme [23], [30], [31], which can also work by post-processing the link phase fluctuations [32]. State-of-the-art long-haul optical fiber links reach a residual link fractional frequency stability in the 10^{-19} or below for integration times above 1000 s seconds, on distances of over 1000 km [27], [33]–[35].

In parallel to such advances, the recent years have seen the advent of digital-electronics in the fields of stabilized lasers, time-and-frequency metrology and atomic physics. With analog-to-digital and digital-to-analog converters (ADCs and DACs), field programmable gate arrays (FPGAs) and direct digital synthesis (DDSs) having reached levels of performance, integration and ease-of-use competitive with analog electronics including for radiofrequency (RF) applications, several laboratories and companies have started to move from analog to digital electronics control loops [36]–[39]. Such Software Defined Radio (SDR) setups bring the possibility to implement different schemes using the same hardware with the benefit of software long term stability and reconfigurability when implementing classical analog processing techniques, and enable the simple duplication of systems and electronic functions, the possibility to control many different channels in parallel with a high data rate and strong computing power, along with small components footprint. Beyond these advantages, discrete time digital signal processing brings a new paradigm illustrated here with sub-sampling and benefiting from high order Nyquist zones [40]. Digital implementation of the local oscillator as a numerically controlled oscillator (NCO), and mixing in the FPGA removes the classical analog challenges of local oscillator leakage through the mixer and I,Q imbalance when recovering the phase from a quadrature demodulation. This approach has led to numerous novel developments [41]–[47].

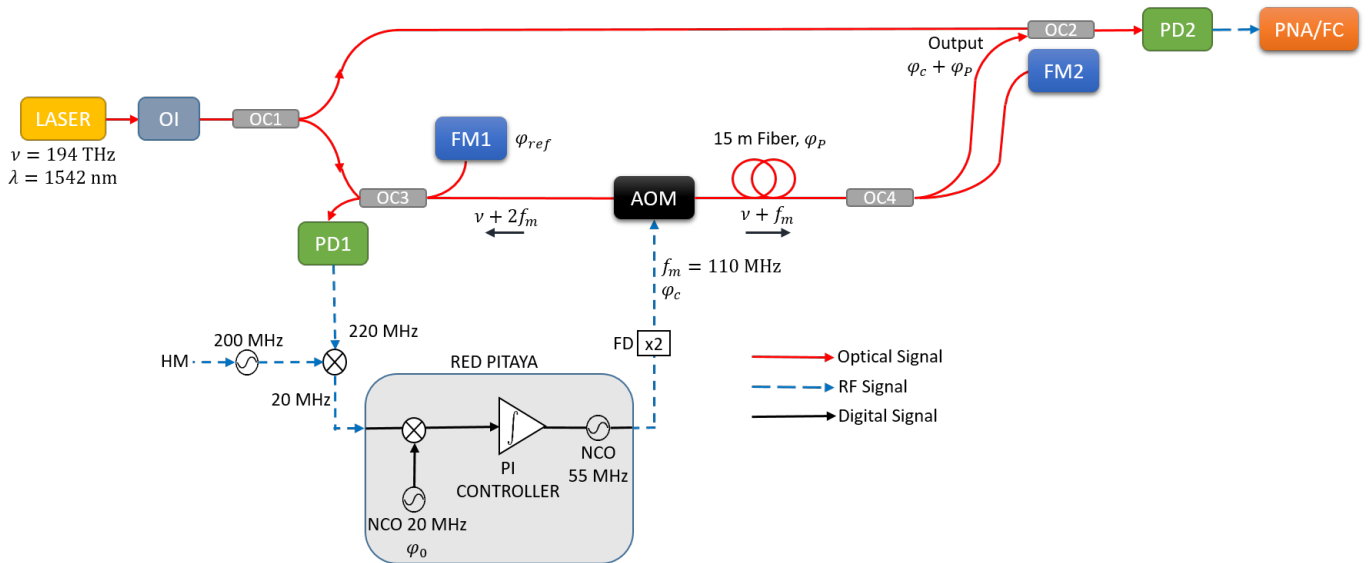


Fig. 1: Experimental scheme of the stabilized optical signal transfer through a 20 m long optical fiber link. The stabilization setup consists in a heterodyne Michelson interferometer (HMI) formed between optical coupler OC3 and the Faraday mirrors FM1 and FM2. Digital control of the optical phase measured at photodiode 1 (PD1) is performed through a digital phase-locked loop. Characterization of the link output phase noise is performed by comparison to the laser source through a Mach-Zehnder interferometer formed between optical couplers OC1 and OC2. Relevant frequencies and phases have been indicated. See text for details. HM: Hydrogen Maser, OI: Optical Isolator, OC: Optical Coupler, PD: Photodiode, AOM: Acousto Optic Modulator, PLL: Phase-Locked Loop, FM: Faraday Mirror, NCO: Numerically Controlled Oscillator.

Among these approaches, Tourigny-Plante *et al.* use the CORDIC arctan algorithm to digitally extract the signal phase [45]. The phase-locked loop (PLL) is implemented on the same board used in this manuscript, clocked by its internal quartz, using an open-source code available online [48]. The digital PLL is demonstrated on a Doppler-cancellation scheme similar to the one presented here and characterized in-loop. Another approach is presented by Cárdenas-Olaya *et al.*, using a tracking DDS scheme that is, to our knowledge, not openly documented [49]. The noise of the digital instrumentation has been carefully characterized [50] and demonstrated experimentally by two-way compensation of long-haul optical fiber links [51].

In this manuscript, we present a digitally controlled Doppler-cancellation setup developed to provide a stabilized fiber output to a compact FP cavity [52] on the laboratory scale. We have put the emphasis on simplicity using off-the-shelf optical components and a compact, digital electronics control loop. The digital control loop can be fully reproduced using the OSC-IMP environment, with all code being openly released under the CeCILL Licence [53]. As presented in the next Section, we rely on a simple demodulation scheme to access the signal phase noise, different from the arctan approach developed in [45] or the tracking DDS approach of [49]. While in-situ characterization of the Ref. [50] setup is implemented using two-way compensation [51], we present a more traditional Doppler-compensation setup with out-of-loop characterization. In addition to the standalone configuration of the digital board, presented also in [45], we characterize external referencing and undersampling using this board.

Section II presents the setup, including both the optical interferometers and the control electronics. Section III illustrates the results obtained in three different configurations, namely using a stand-alone digital board, an externally clocked digital board, and using undersampling. Section IV puts these results in perspective with the current state-of-the-art and applications of ultra-pure signal optical fiber transfer.

II. METHODS

The aim of the setup is to transfer an ultra-stable signal at the laboratory scale (few tens of meters) using an optical fiber while maintaining the spectral purity and frequency stability of the signal. To do so, the main challenge is to reduce the phase disturbances caused by the thermal sensitivity and mechanical vibrations sensitivity of the optical fiber through the path of the link and to compensate these phase fluctuations using a PLL.

A. Principle of the compensated link

The link, including the noise compensation, is based on a heterodyne Michelson interferometer (HMI) scheme (Fig. 1) in which the beam splitter is the fiber coupler OC3. The short arm of the Michelson interferometer that defines the phase reference φ_{ref} of the link is formed between OC3 and the Faraday mirror FM1. The long arm used to transfer the optical reference that

includes the 15 m of optical fiber is the path between OC3 and another Faraday mirror FM2 in which the phase is affected by environmental perturbations φ_P . This path includes an acousto-optical modulator (AOM) driven at $f_m \approx 110$ MHz that adds a controlled phase φ_c to this arm. The optical coupler OC4 extracts the signal at the end of the link, with phase $\varphi_u = \varphi_P + \varphi_c$. The beatnote signal on PD1 carries the phase of the link at $2f_m \simeq 220$ MHz and is demodulated by an RF reference signal at $f_0 = 220$ MHz¹. The error signal $\varepsilon = 2(\varphi_P + \varphi_c - \varphi_{ref}) - \varphi_0$ with φ_0 the contribution of this RF reference, vanishes when the loop filter is activated to compensate the noise of the link. Please note that the factor 2 comes from the double pass of the light in the two arms of the HMI. Thus the phase at the output of the link is $\varphi_u = \varphi_{ref} + \frac{1}{2}\varphi_0$. With this basic model we see that the noise compensation is ultimately limited by the phase fluctuations of the reference arm φ_{ref} and the RF reference φ_0 . A more detailed analysis of the link various noise contributions can be found in [54].

B. Optical setup

The experiment is fed by a free-running, commercial fibre laser (NKT Photonics Koheras Adjustik, with a typical phase noise of 80 dBrad²/Hz at 1 Hz) of wavelength $\lambda = 1542$ nm with about 14 mW optical output power. The 90/10 fiber beam splitter OC1 splits the laser into the two parts of the setup, with 10% going to the characterization part. The light is injected in the 15 m fiber through the 90/10 coupler OC3 using the 90%-port. At the end of the link the 90/10 coupler OC4 sends 90% to the output port and 10% to Faraday Mirror FM2. With this configuration 35% of the power injected in the link is transmitted to the end user (at the output point on Fig. 1) and the beatnote signal on PD1 is realized with 8.1% of the laser output power coming from the reference arm and 0.17% from the round trip. Should this be too low, this could be increased to 1.3% by using 50/50 couplers for OC3 and OC4, with an end user total transmission decreased to 11%.

Since the signal provided by the photodiode PD1 is processed by the PLL to phase lock the link (in-loop signal), it can not be used to evaluate the performances of the link. A dedicated part of the setup is implemented to characterize the signal transmitted by the link (Fig. 1). We use a heterodyne Mach-Zehnder interferometer (HMZI) formed between beamsplitters OC1 and OC2 to characterize the link output phase noise. One arm of the HMZI is formed by a short uncompensated fiber path between OC1 and OC2, while the second arm is formed by the ultra-stable link and its output fiber.

In practice, the evaluation of performances of the link requires to place the end close to the beginning. In order to passively reduce the effect of uncompensated fiber paths (OC1-OC2, OC1-OC3, OC3-FM1 and OC4-OC2, with a total length of 4.5 m), the entire setup except for the 15 m patch-cord is placed on a floated optical table and underneath a wooden box that provide passive acoustic isolation and thermal shielding from the room air conditioning residual temperature fluctuations.

Moreover, the uncompensated fiber path between OC4 and OC2 is partially corrected for by placing the FM2 close to OC2 and using the same length of fiber, so that thermal perturbation, fluctuating slowly, affect these two fibers similarly and the compensation matches the perturbations in the output fiber.

The ultra-stable link performance is analyzed by characterizing the 110 MHz beatnote signal on PD2 using either a phase noise analyzer (PNA, Rohde & Schwarz FSWP) or a frequency counter (FC, K+K FXE) to quantify both phase noise and fractional frequency stability.

C. Control electronics

Our control electronics is centered on a digital PLL implemented on an FPGA integrated on a system on a chip (SoC). The commercial board (RP, Red Pitaya STEMLab 125-14) includes an analog to digital converter (ADC, 14 bits, 125 MS/s/channel, two channels), a digital to analog converter (DAC, 14 bits, 125 MS/s/channel, two channels) as well as the SoC including an embedded processor (Xilinx Zynq 7010). Fig. 2 sketches the electronics setup used in the two first measurements of this work. Modifications for the last step will be described in section III-C. Compliance with the Nyquist–Shannon theorem during sampling by the ADC, in addition to the front-end filters, requires downconverting the 220 MHz of the HMI beatnote signal to 20 MHz, below the Nyquist frequency $f_N = 62.5$ MHz of the ADC thanks to a 200 MHz signal source that is derived from an active hydrogen MASER (HM) using a DDS synthesizer. The resulting signal is filtered and amplified to provide a 11.6 dBm signal to the input connector of the board taking care to add a 50 Ω load in parallel to the high-impedance ADC input (the jumper on the board is positioned to the ± 1 V full scale).

The functions to process the signal for digital PLL are the same than with analog electronic: demodulation with a phase reference, low-pass filtering, loop filter and modulation of a controlled oscillator (see Fig. 2). Data provided by the 14-bits ADC, processed by these functions and sent to the DAC are signed and fed with a constant data rate of 125 MS/s. A 16-bits amplitude and 40-bits phase accumulation register NCO is the phase reference of the phase-locked loop. The demodulation is implemented with a multiplication process with a 14 bits output followed by a finite impulse response (FIR) filter configured with 25 coefficients each encoded in 16 bits.

In this manner, the signal recorded from the ADC at baseband is frequency transposed by the multiplication with the complex NCO acting as an ideal mixer that avoids the classical imbalance and lack of quadrature issues found in hardware

¹Please note that in practice we use two different schemes, with cascaded analog and digital demodulation at 200 MHz and 20 MHz or direct digital demodulation of the 220 MHz beatnote.

implementations. The phase detector is a complex to real part converter since no gain was observed when using the more time and resource consuming arctan CORDIC implementation which would extend the linearity range to large phase offsets. In this short link investigation, no phase slip was observed once the lock is activated, and the setpoint remains in the locally linear behaviour of the complex to real phase detector. Using the CORDIC implementation might be necessary for implementing longer links, to ensure linearity and avoid cycle slips.

The FIR filter cutoff frequency is 4 MHz with more than 40 dB rejection for frequencies above 14 MHz. The FIR output is a 32 bits data stream. A dynamic shifter is then used to reduce the number of bits to 14 before the loop filter while adapting the range to the signal dynamics on the fly for the generation of the correction signal. The output is added to a constant value used to bias the frequency of the output DDS based on a second NCO. Then, data are sent to the channel 1 of the DAC. As the Nyquist-Shannon sampling theorem must also be satisfied for this converter, the NCO center frequency is set at 55 MHz and then the signal is frequency doubled, filtered and amplified to drive the AOM, which then corrects the optical fiber link phase fluctuations. Another DDS is implemented in the FPGA-chip based on a third NCO that outputs to channel 2 of the DAC. For most measurements presented below, this allows us to determine the digital phase reference contribution to the lock performance. The NCOs are implemented as 40 bits accumulators clocked at a rate of 125 MHz, leading to a $125 \cdot 10^6 / 2^{40} \simeq 0.11$ mHz resolution. The accumulator feeds a lookup table generating a sine wave encoded with 4096 values matching the 12-bit DAC resolution.

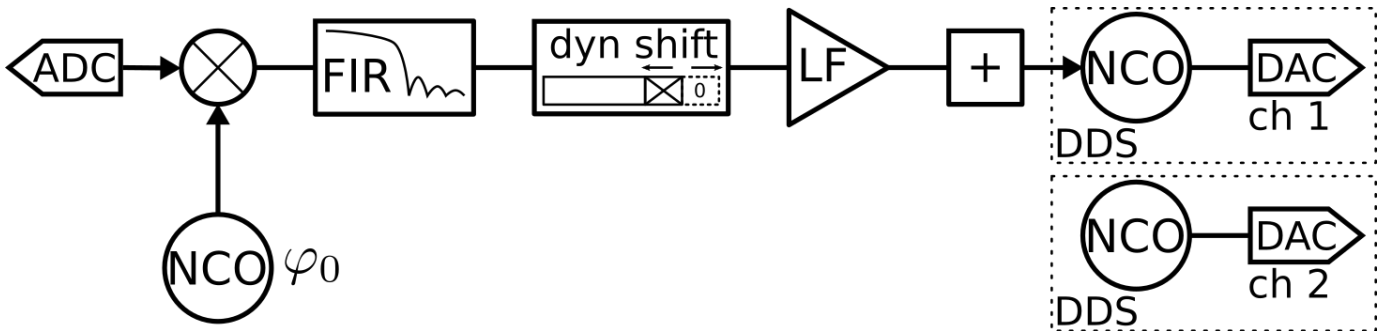


Fig. 2: Digital control scheme. The digital board offers two parallel channels. The two channels are similar and benefit from the digital implementation of duplicating functionality, emphasizing the flexibility of the SDR approach. We use the first one for locking. The second channel is used as a DDS for the experiments presented here. The design is based on separate blocks each representing a function. ADC: analog to digital converter. NCO: numerically controlled oscillator. FIR: finite impulse response filter. dyn shift: dynamic shifter (adds or removes least significant bit(s), set on-the-fly by user). LF: loop filter (proportional integrator function). See text for details.

Details and designs can be found here: https://github.com/oscimp/app/tree/master/redpitaya/double_iq_pid_vco

The embedded processor is used to run a GNU/Linux operating system (OS) dedicated to these applications (Buildroot). A digital signal processing framework dedicated to time & frequency metrology application has been developed and is available to the community at <https://github.com/oscimp/oscimpDigital> providing a consistent set of the real time signal processing blocks configuring the FPGA, the Linux drivers communicating with hardware, and the userspace libraries providing the flexibility of a user friendly interface for controlling the various processing blocks. This OS interfaces most of the basic functions described above, including network connectivity and file storage for long term logging as required for metrology application, and allows modifications of parameters by the users such as filter coefficients and DDS's frequencies. Among other features, a key one is the optimization of the resolution in agreement with the range of the error signal by using the dynamic shift register. This block selects 14 consecutive bits among the data 32 bits. The number of discarded lowest significant bits n is set by the user (where $18-n$ will be the number of discarded most significant bits). This reduction of the data size can be crucial since each single mathematical operation enlarges the number of bits required to losslessly encode the output.

Such an inflation of the number of bits in the data flow is not relevant because (i) it will rapidly surpass resources available in the FPGA, (ii) part of the lowest significant bits can often be neglected and (iii) the output DAC ultimately limits the resolution (14 bits for the RP).

This is also useful for adjusting the resolution when the input level range is changing. A high n will ensure that higher amplitude signals full dynamic is captured without overflows at the servo input, which is useful for monitoring the signal in open-loop (monitoring not shown in the circuit diagram), while a lower n guarantees a full resolution of the nearly vanishing error signal when the PLL is engaged.

As mentioned above, we use the characterization photodiode (PD2) to analyze the link output phase noise and fractional frequency stability carried by the 110 MHz beatnote. While the PNA input can directly analyze the 110 MHz signal phase-noise, the frequency counter input bandwidth is 60 MHz. When measuring fractional frequency stability, we thus mix the 110 MHz signal from PD2 with a 100 MHz signal from a synthesizer clocked by an HM in order to generate a 10 MHz signal.

III. RESULTS

We present the results obtained with our setup, including both phase noise and fractional frequency stability. We have investigated three configurations based on the Figs. 1 and 2 general scheme. In §III-A, we use a stand-alone board, and all the digital electronics controls are clocked by the board internal quartz oscillator. In §III-B, we use the same scheme but this time adding a highly stable external clock to the digital electronics board. In §III-C, the Fig. 1 scheme is slightly modified as we implement undersampling, again using an external clock.

A. Using the board internal quartz oscillator

In this section, we use the board internal quartz oscillator to clock the digital controls. The results obtained are shown in Fig. 3.

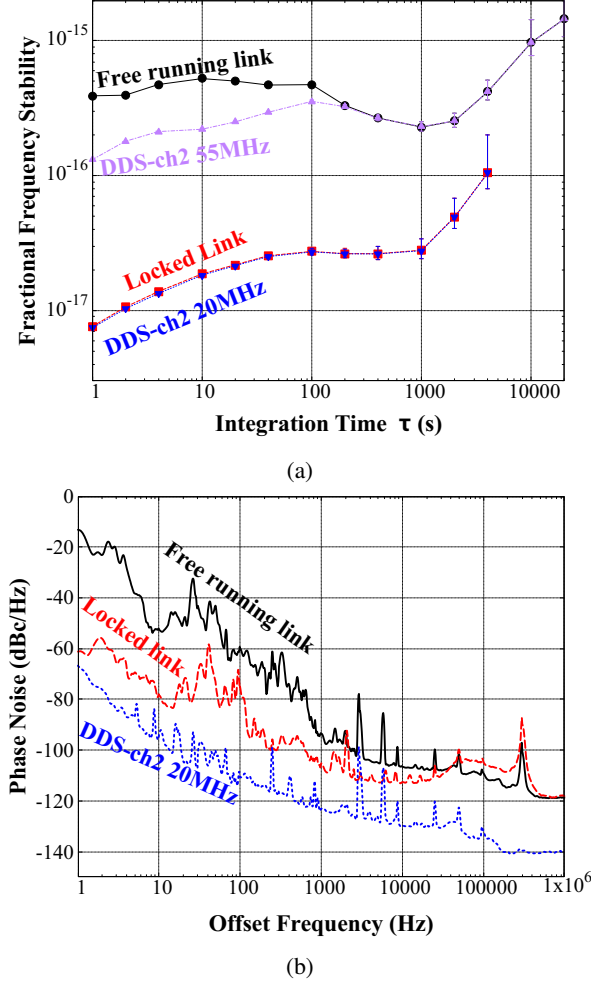


Fig. 3: Stand-alone digital configuration. (a) Fractional frequency stability of free running link (solid black circles), locked link (solid red squares), 55 MHz RP output (solid purple triangles), 20 MHz output (solid inverted blue triangles). (b) Phase Noise of free running link (black straight line), locked link (red dashed line), 20 MHz output (blue dotted line). All RP signals are normalized to the 194 THz carrier frequency.

Fig. 3 (a) shows the fractional frequency stability (FFS, estimated by the modified Allan deviation) of the free-running (black solid circles) and locked (red solid squares) PD2 signal. The locked link stability starts at around 8×10^{-18} at 1 s with an initial $\tau^{1/2}$ slope, followed by a 3×10^{-17} plateau until 1000 s and a linear frequency drift for longer integration times. The correction provides more than a factor of 10 instability reduction between 1 s and 1000 s, while the link instability is reduced by a factor 50 at 1 s.

In order to determine the contributions of the digital control board to the link performances, we have also monitored the NCO phase fluctuations with the DDS implemented on the channel 2 of the DAC set to 55 MHz for free-running measurements and to 20 MHz when the lock is engaged. In open-loop, the 55 MHz frequency noise will be multiplied by 2 at the board output. In closed-loop, the 20 MHz NCO frequency fluctuations are divided by 2 through the control loop at the user end (see

II-A). To analyze their contributions, we scale the 55 MHz and 20 MHz signals by multiplying their frequency fluctuations by 2 and 0.5, respectively, and normalize them by 194 THz for FFS plots.

The FFS of the 55 MHz signal shows that the DDS used to drive the AOM is limiting for integration times longer than 200 s when the link is free running. This phase fluctuation is cancelled when the loop is closed and we see that the FFS of a 20 MHz signal scaled to the link output frequency overlaps with the stabilized link FFS indicating that the phase reference of the PLL φ_0 is the limitation. The corresponding DDS FFS at 20 MHz is around 1.6×10^{-10} at 1 s, consistent with the measurement presented in [55].

Fig. 3 (b) shows the single-sideband phase noise spectrum of the free-running (black line) and locked (red dashed line) PD2 signal. The locked link instability is -60 dBc/Hz at 1 Hz, reaching a -110 dBc/Hz floor around 10 kHz. The lock bandwidth is ≈ 40 kHz.

Please note that the NCO contribution at the link output is of about -66 dBc/Hz at 1 Hz. If we scale this back to the digital board clock frequency, this corresponds to -31 dBc/Hz at 1 Hz at 125 MHz. This is in good agreement with the RP internal quartz phase noise presented in [55]. This implies that the NCO performance is entirely determined by the board internal quartz, justifying the use of an external clock for improved performance.

B. Using the board clocked by an external clock

To further investigate the fundamental limitation of the RP we provide an external low noise 125 MHz clock signal to the digital control board. This signal is generated by a DDS clocked by an active HM, and is coupled to the board through a balun to respect impedance matching. The contribution of the clock signal is now estimated at 10^{-19} or below. The results are shown in Fig. 4.

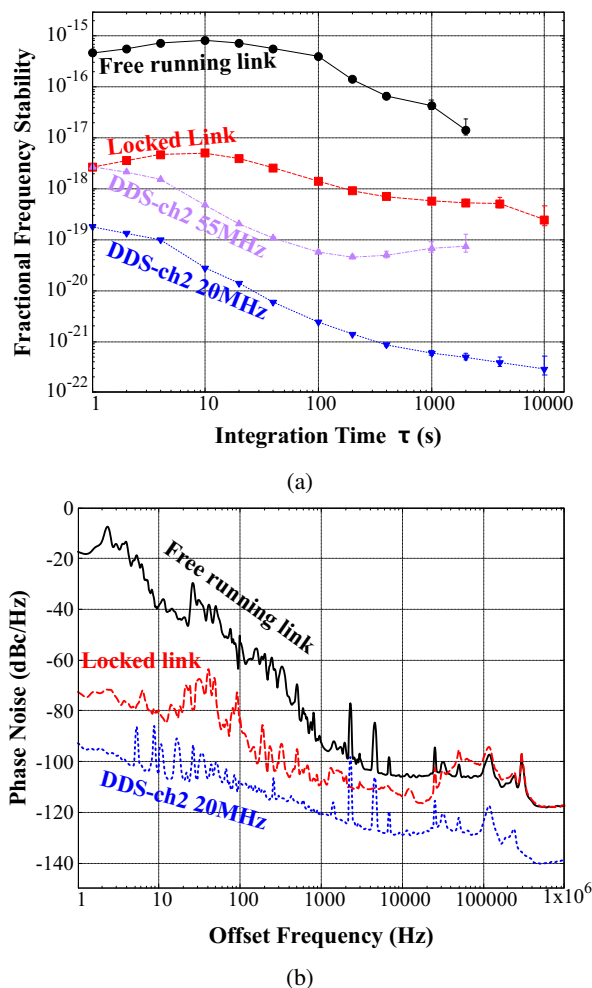


Fig. 4: External clock digital board configuration. (a) Fractional frequency stability of free running link (solid black circles), locked link (solid red squares), 55 MHz RP output (solid purple triangles), 20 MHz output (solid inverted blue triangles). (b) Phase Noise of free running link (black straight line), locked link (red dashed line), 20 MHz output (blue dotted line). All RP signals are normalized to the 194 THz carrier frequency.

Fig. 4 (a) shows the fractional frequency stability (estimated by the modified Allan deviation) of the free-running (black solid circles) and locked (red solid squares) PD2 signal when using an external clock. The locked link stability starts at around 2×10^{-18} at 1 s with a 8×10^{-18} bump at ten seconds, and then reaches a floor below 10^{-18} . The link instability is reduced by a factor 100 from 1 s to 400 s.

Fig. 4 (b) shows the single-sideband phase noise spectrum of the free-running (black line) and locked (red dashed line) PD2 signal when using an external clock. The locked link phase noise is below -70 dBc/Hz at 1 Hz, reaching a -110 dBc/Hz floor around 10 kHz. The lock bandwidth is ≈ 40 kHz, as in the previous section. The NCO contribution is again consistent with the external clock phase noise measured by [55].

C. Implementing undersampling with the Red Pitaya

In this section, we use undersampling in order to directly extract the phase noise from the 220 MHz output of the lock photodiode PD1. To do so, we have patched the commercial board by bypassing the anti-aliasing filters to directly send the signal to the sample and hold of the ADC (this would be unnecessary for boards such as the STEMlab 122-16 with direct RF sampling up to 550 MHz). The board unbalanced to balanced amplifier that acts as a low pass filter is replaced by a passive balun transformer, so as to benefit from the full 750 MHz bandwidth of the LTC2145 analog to digital converter frontend. This enables undersampling the signal, under the strong assumption of a pure and known beatnote frequency; this is mandatory for recovering the useful signal when it does not comply with the Nyquist–Shannon theorem.

We use this method to avoid the use of a mixer and synthesizer at the output of PD1. In addition to removing these potential noise and aging sources, the local oscillator phase is unknown at startup, whereas the ADC is readily frequency and phase synchronized over a network disseminating time and frequency information. Thus, undersampling allows for coherent acquisition on the large scale of a laboratory. As shown Fig. 5, we filter and amplify the photodiode signal and send it directly to the modified board. With an external clock at 125 MHz, we work in the second Nyquist band of the input ADC. As a result, the 220 MHz signal is read as a $2 \times 125 - 220 = 30$ MHz sine wave. We demodulate this aliased signal using a 30 MHz NCO. The rest of the setup is unchanged compared to previous sections.

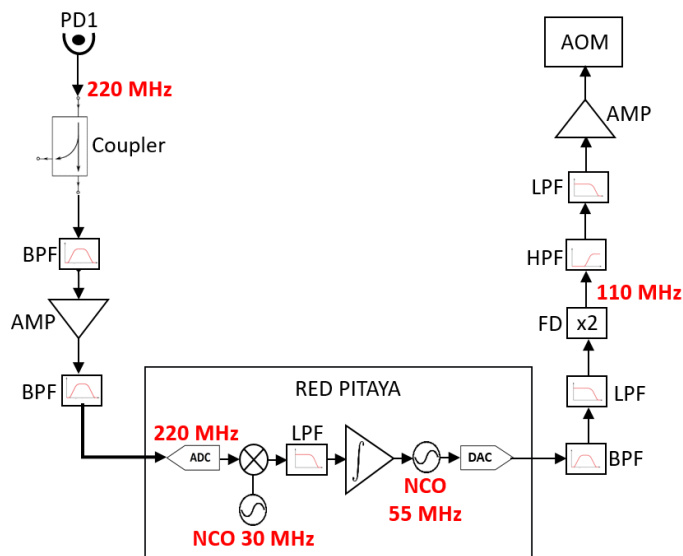


Fig. 5: Control electronics, undersampling servo loop setup. Fluctuations carried by the 220 MHz signal are directly sampled by a Red Pitaya to implement a PLL. Corrections are carried by the 110 MHz signal driving the AOM. See text for details. PD: Photodiode, LPF: Low Pass Filter, HPF: High Pass Filter, BPF: Band Pass Filter, AMP: Amplifier, FD: Frequency Doubler. The coupler is for monitoring purposes only.

The fractional frequency stability and the phase noise measurements are shown in Fig. 6 by the dashed curves.

Fig. 6 (a) shows the fractional frequency stability (estimated by the modified Allan deviation) of the free-running (black open circles) and locked (red open squares) PD2 signal for the undersampling scheme. The locked link stability starts at around 6×10^{-18} at 1 second with a 4×10^{-18} bump at ten seconds, and then reaches a floor below 10^{-18} . There is a 1/100 reduction of the link instability from 1 s to 200 s.

Fig. 6 (b) shows the single-sideband phase noise spectrum of the free-running (black dashed line) and locked (red dashed line) PD2 signal for the undersampling scheme. The locked link instability is -70 dBc/Hz at 1 Hz, reaching a -110 dBc/Hz floor around 10 kHz. The lock bandwidth in this configuration is around 70 kHz.

IV. DISCUSSION

The results obtained with a commercial board-based digital control for a Doppler-compensation scheme are very promising for a wide range of applications that require the local distribution of an optical frequency reference signal.

The measured locking bandwidth for all configurations is between 40 and 70 kHz. With our link length of about 20 m in total, the one-way optical delay τ_{link} is about 100 ns, which determines the best achievable, link-delay-limited bandwidth of $1/(8 \times \tau_{link}) \approx 1.25$ MHz (assuming a $\pi/4$ phase margin). The digital board main delay stems from the FIR, and is estimated to be at most 136 ns for our 25-coefficients filter. Lastly, the analog electronics and AOM contribution to the delay is of about 1 μ s. With this total 1.236 μ s delay, the maximum achievable bandwidth in our configuration is around 100 kHz.

Using a stand-alone board, the fractional stability performance is compatible with compact ultra-stable cavity setups, which have demonstrated fractional frequency stabilities in the range of 10^{-15} as well as ultrastable FP cavities with stabilities in the range of 10^{-16} and slightly below. It is however not suitable for the best current FP cavities or atomic clocks. For applications where the optical signal transmitted through the link would serve as a microwave photonics source, the measured phase noise is remarkably low. Assuming perfect division to 10 GHz, the measured phase noise contribution of the link would be -155 dBc/Hz at 1 Hz, with a -205 dBc/Hz floor.

Using an external clock pushes the setup performance towards state-of-the-art, and its residual fractional frequency instability is sufficient to transfer signals at the level of the best FP-based ultrastable lasers in the low 10^{-17} . When using an active HM as a reference, the digital board clock performance will actually be limited by its internal PLL residual noise [55]. According to [55], using instead a 10 MHz reference signal would degrade the SoC PLL residual noise by roughly a factor of 2. Given the typical performance of GPS-disciplined Rb standards, this would still guarantee a link fractional frequency stability well below 10^{-17} at 1 s and a negligible NCO contribution at longer integration times.

Our measured stabilized link performance is however not suitable for the transfer of the signal from state-of-the-art optical clocks, with instabilities starting at 10^{-16} or below and integrating as $\tau^{-1/2}$. The measured noise of our setup seems to show a floor near 1000 s which is close to the performance of these clocks. We however believe that the measured fractional frequency stability is limited by our HMI setup rather than the link, and that etalon effects due to the absence of a second AOM near the FM could explain the measured instability. This could be tested in the future to verify that the presented setup is compatible with today's best optical atomic clocks. As our setup is mostly targeted towards compact, less-demanding applications, we have not tried to improve the setup limit. It is clear that the digital board itself should not limit the setup performance even for state-of-the-art performance, as the NCO contribution is below 10^{-18} at all integration times and integrates down to the 10^{-22} range. Moreover, the ADC flicker phase noise is about -109 dBc/Hz at 1 Hz, with a floor at -146 dBc/Hz, even for a 220 MHz input frequency, as shown in [56]. This makes the ADC phase noise contribution well below the best phase noise reported here.

As shown in Fig. 6, the undersampling setup provides the same results as the regular externally clocked board, with a simpler setup.

The ch. 2 DDS output is also useful as an indication of the digital board performance. As described in section III-A, the in-loop and out-of-loop NCO contributions are scaled differently, by a factor of 0.5 and 2 respectively. Assuming they have identical FFS determined by the board clock FFS, their impact at the optical carrier frequency should differ by a ratio of $4 \times 55/20 = 11$. However, we observed that this ratio ranges between 15 and 20 at 1 s for our measurements, while for longer integration times, different behaviors are observed. This seems to imply that the assumption of FFS determined only by the digital board clock fails, and that additional frequency noise is added by the NCO. While this is not a limitation for the purpose presented here, this should be explained and is currently under investigation.

V. CONCLUSION

We have implemented a Doppler-cancellation scheme for optical fiber link phase stabilization that relies on a digital servo-loop. Using a commercial digital control board in three different configurations, including using an external clock and undersampling. Using an external clock, the stabilized link is compatible with current state-of-the-art optical references. Using undersampling simplifies the setup while maintaining this level of spectral purity.

While the fractional frequency stability reached with our measurements could be improved by improving the optical setup, we have determined that the digital electronic board intrinsic noise would limit the performance to the low 10^{-22} range at 10000 s. This shows that low-cost, small footprint devices can be integrated to the most demanding metrological setups. All digital designs are available at <https://github.com/oscimp/oscimpDigital> and can therefore be easily duplicated.

VI. ACKNOWLEDGEMENTS

This work has been supported by the EIPHI graduate school (contract ANR-17-EURE-0002), the labex FIRST-TF (ANR-10-LABX-48-01), the EquipeX OSCILLATOR-IMP (ANR-11-EQPX-0033), the Région Bourgogne Franche-Comté, and the Centre National d'Études Spatiales (CNES, R&T R-S19-LN-0001-019).

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The authors would like to thank Rodolphe Boudot and Marion Delehaye for their careful reading of the manuscript, as well as L  o Tranchart and Ivan Ryger for the FIR delay measurements.

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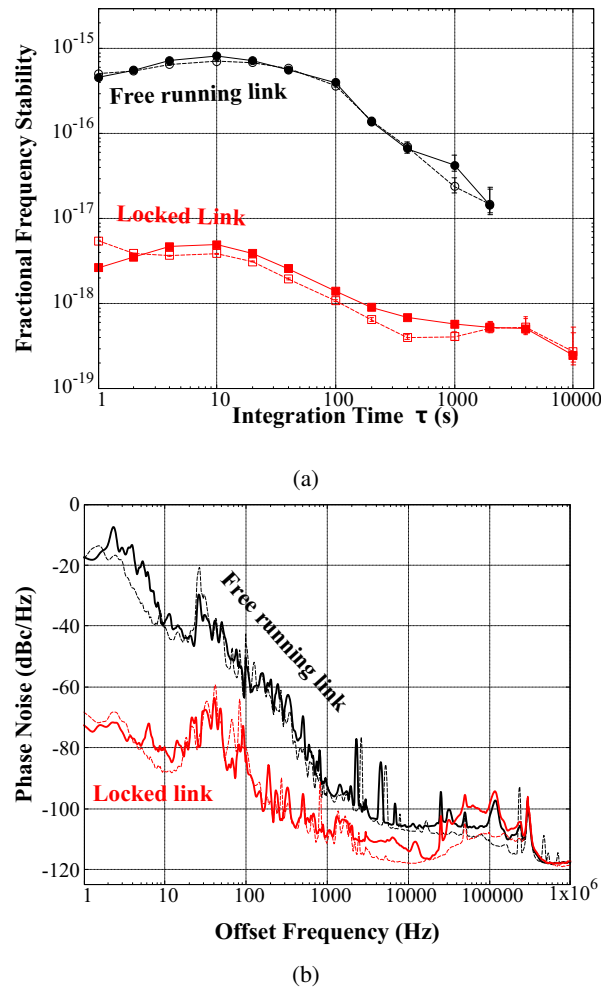


Fig. 6: (a) Comparison between the external clock (full symbols) and undersampling (with external clock) configurations, free running link with undersampled Red Pitaya (open black circles), locked link (open red squares). All RP signals are normalized to the 194 THz carrier frequency.

(b) Comparison between the Phase Noise of the link with undersampled Red Pitaya (red dashed, black dashed) and normal Red Pitaya (red straight, black straight).

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