

Glass Substrate Interposer for TSV-Integrated Surface Electrode Ion Trap

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ABSTRACT

Confined by a combination of RF and DC electrical field, trapped ions are well isolated to retain their quantum properties, and laser addressing is used to perform computation and readout [1]. As a promising candidate for quantum computation, ion traps have been developed from mechanically assembled Paul trap to lithography-defined surface electrode ion trap over past two decades. To further boost its computation capability, numerous ions (~100 ions, intermediate scale) should be trapped and entangled simultaneously, which requires the coherent control from thousands of co-planar RF and DC electrodes. This remains a challenge for conventional wire bonding due to the lack of complex signal-feedthrough capability. To resolve this issue, TSVs are integrated into surface electrode ion trap design. At the same time, interposer with redistribution (RDL) layer is introduced for TSV landing. As a result, the CPGA-RDL signal transmission via TSVs can be achieved with much higher flexibility and scalability than wire bonding.

Previously, both top ion trap (denoted as TSV die) and interposer die are fabricated on silicon substrate as shown in Fig. 1. However, it was found that the silicon substrate interposer has large parasitic capacitance which will significantly affect the RF performance of the whole device (Fig. 2 (a)). To solve this issue, glass is used to replace silicon as the interposer substrate. Firstly, glass is a dielectric material and has low loss tangent (~0.028 @ 50 MHz), which means the RF dissipation through glass can be greatly reduced (see Fig. 2 (b) and Ref. [2] for details). Secondly, glass substrate interposer employs simpler fabrication process, as compared to its silicon counterparts which require additional dielectric layer deposition and patterning. Besides, to further minimize the parasitic capacitance of glass substrate interposer, the geometry of RDL is optimized with smaller surface area, where only TSV landing pads and necessary routing circuits are maintained. The gaps between neighboring electrodes are also enlarged to minimize shorting, as shown in Fig. 3.

Standard wafer-level packaging techniques are used for both TSV die and interposer die fabrication. They are fabricated separately and selected known good dies are bonded after individual testing and characterization. The fabrication process of TSV die is illustrated in Ref. [3]. For glass substrate interposer, adhesion layer (Ti, 0.1 μm) and seed layer (Cu, 0.1 μm) are first deposited on glass surface. Mask-defined electroplating of 2 μm Cu is then carried out, followed by seed layer etch back to prevent inter-electrode shorting. A polyamide layer is deposited on top of Cu RDL to protect it from oxidizing. Finally, openings are made in this polyamide layer to accommodate under bump metallization (UBM), which consists of 3 μm Cu and 0.3 μm Au.

As mentioned, the parasitic capacitance of silicon interposer die is much larger than TSV die. This indicates that great RF power will be dissipated from interposer during ion trapping operation, since the two capacitors from interposer die and TSV die are in parallel. In this case, the overall ion trap performance (e.g., heating rate, lifetime, etc.) will be undermined, despite the retained low-loss property by the TSV die itself. However, with the introduction of glass substrate interposer, the RF loss from interposer can be reduced significantly, while the ion trapping functionality of TSV die can be maintained. After the fabrication of glass substrate interposer, C - V measurements and S-parameter tests will be performed and the obtained results will be compared against silicon substrate interposer and TSV die. After the final assembling of TSV die and glass interposer, a resonator test will be performed to verify the device's RF

performance prior to the ion trapping test. (We acknowledge the funding support from A*STAR Quantum Technology for Engineering (A1685b0005) for this work.)

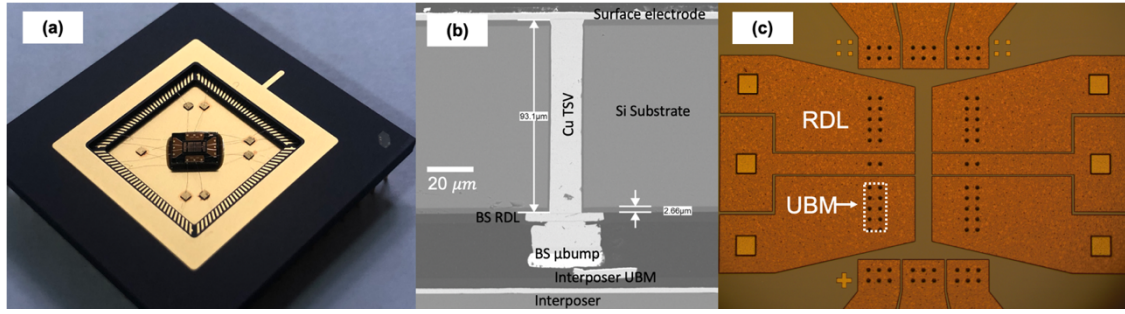


Fig. 1. (a) Bonded TSV die and silicon substrate interposer in a CPGA package; (b) The cross-sectional SEM image of bonded TSV die and silicon substrate interposer; (c) The optical graph of surface geometry of silicon substrate interposer.

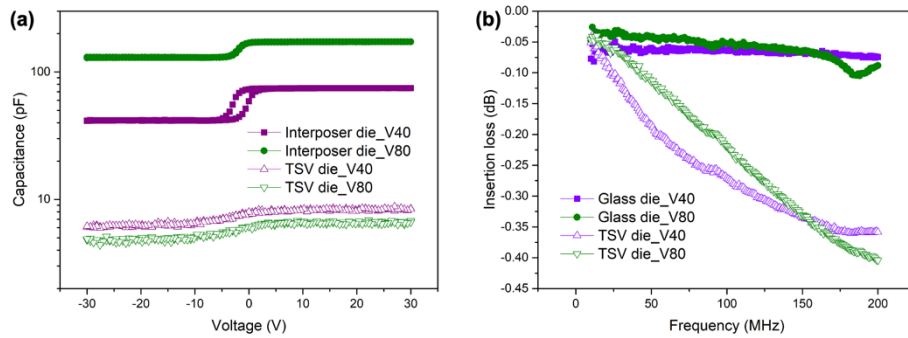


Fig. 2. (a) C - V measurement of TSV die and silicon substrate interposer (two size variations are included). Silicon substrate interposers exhibit 10 times larger capacitance than TSV dies; (b) Insertion loss (S21) of ion trap on glass substrate and TSV-integrated silicon substrate. Both show extremely low power dissipation [2], indicating glass substrate interposer can have competent RF performance.

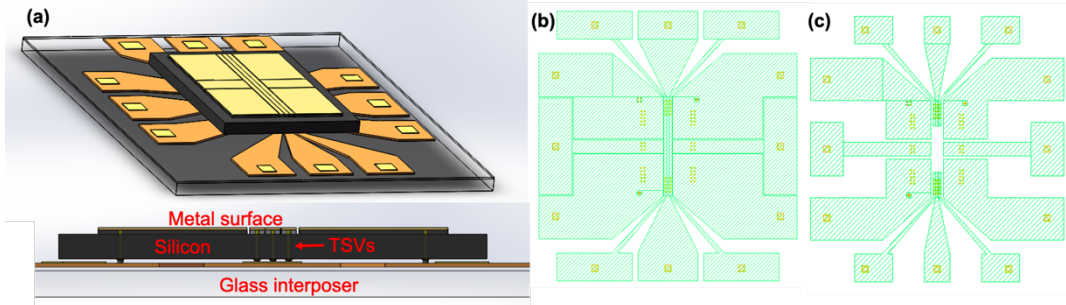


Fig. 3. (a) Schematics of bonded TSV die and glass substrate interposer; (b) Geometry of RDL layer of original silicon substrate interposer; (c) Optimized geometry of RDL layer of glass substrate interposer. The inter-electrode gaps are enlarged, while the surface area reduction is about 40%, as compared with original geometry.

References

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