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III-V MULTIJUNCTION SOLAR CELLS ON ULTRATHIN GE/SI VIRTUAL SUBSTRATES GROWN AT LOW TEMPERATURE BY RF-PECVD

Iván García^{1*}, Monalisa Ghosh², Víctor Orejuela¹,
Pere Roca i Cabarrocas², Ignacio Rey-Stolle¹

¹Instituto de Energía Solar, Universidad Politécnica de Madrid, 28040 Madrid, Spain

²LPICM-CNRS, Ecole Polytechnique, 91128, Palaiseau, France

ABSTRACT: The application of Ge/Si virtual substrates with an ultrathin Ge layer to the development of high efficiency III-V solar cells is analyzed. The potential to achieve high efficiencies in GaInP/GaInAs/Si triple-junction cells, which is affected by the optical absorption in the Ge layer, is theoretically demonstrated under realistic scenarios of Ge/Si substrate characteristics and III-V cell configurations. The first dual-junction GaInAs/Ge/Si III-V cells fabricated on these substrates demonstrate the concept with functional devices and show the route to high efficiency implementations by using appropriate Si substrates and optimized Ge deposition.

Keywords: germanium virtual substrate, low-temperature RF-PECVD, III-V multijunction solar cell

1 INTRODUCTION

Virtual substrates fabricated by direct deposition of Ge on Si have gained attention over the last years due to the high quality obtained, i.e., low threading dislocation densities (TDD) and surface roughness, offering a high potential as low-cost templates for the implementation of all kinds of GaAs-based electronic devices, including high efficiency multijunction solar cells. We have shown GaInP/GaInAs/Ge 3-junction cells (3JSC) on active (thick Ge) Ge/Si virtual substrates in previous conferences [1], [2]. The formation of cracks due to the mismatch in thermal expansion coefficients between the Si substrate and the rest of Ge and III-V layers poses an important challenge to this approach. Thinning the III-V structure has been demonstrated to prevent cracking at the expense of some efficiency loss [3].

In this work we are presenting a parallel approach consisting on using Ge/Si virtual substrates with an ultrathin Ge layer (20-140 nm) fabricated by low-temperature radio-frequency plasma-enhanced chemical vapor deposition (RF-PECVD), with a reported TDD below $5 \cdot 10^6 \text{cm}^{-2}$ [4]. This thin Ge layer bridges the lattice constant difference between Si and GaAs and thus would enable the deposition of high efficiency III-V solar cell structures on top without surpassing the critical thickness for crack formation. In this case, the Ge layer is too thin to function as a subcell, but the Si substrate can perform the role of bottom cell. This method is simpler and potentially lower cost than designs using GaP nucleation and GaAsP-based buffer layers [5], or wafer-bonding [6]. However, the thin Ge layer introduces a parasitic optical absorption that affects the efficiency potential. Therefore, the potential to obtain high efficiency triple-junction solar cells (3JSC) with a Si bottom junction is first analyzed theoretically, considering the effect of the parasitic absorption in the Ge layer, the design of the upper junctions, etc, showing that efficiencies approaching 34% can be obtained. Then, we show our first experimental results on GaInAs solar cells grown on ultrathin Ge/Si virtual substrates with a Ge layer as thin as 20 nm, aiming to test the stability of this thin Ge layer and its suitability as epitaxy template, resulting in a GaInAs/Si dual-junction solar cell, which shows no cracking and offers promise to obtain high efficiencies in next implementations using higher quality Ge/Si templates.

2 METHODS

The theoretical calculation of the external quantum efficiency, photocurrent and dark currents is performed using 1D models based on the Hovel approach and the generalized matrix method. The Ge/Si virtual substrates are fabricated by RF-PECVD using p-type Si substrates with a resistivity of 1-10 $\text{ohm} \cdot \text{cm}$. The results presented in this abstract are obtained for non-epiready Si substrates and with a miscut of 5° towards $\langle 110 \rangle$. Epiready substrates with a more appropriate miscut of 6° towards $\langle 111 \rangle$ are being used for the next developments. 20 nm Ge films are deposited in a standard 13.56 MHz capacitively coupled RF-PECVD, using the process parameters explained elsewhere [4]. The virtual substrates used are not optimized in terms of Ge layer quality, and they show a high TDD. III-V structures were grown by MOVPE (details can be found in [3]) and solar cell devices were fabricated using standard photolithography and wet etching techniques, with appropriate metal contacts for GaAs (front) and Si (back). No passivation of the Si back surface was applied. External quantum efficiency (EQE) and I-V curves were taken using conventional methods.

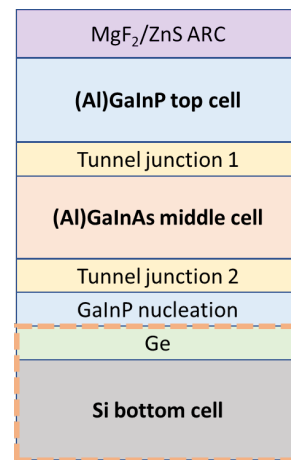


Figure 1: Baseline structure of the 3JSC on Ge/Si virtual substrate studied

3 ANALYSIS OF PERFORMANCE POTENTIAL

The suitable Ge layer thickness to achieve the highest quality template by low temperature RF-PECVD in terms of TDD and surface roughness has been found to lie between 20 and 140 nm. Therefore, the parasitic light absorption in this layer can be significant. Thus, the potential of these virtual substrates was analyzed towards the achievement of high efficiency two-terminal, monolithic (Al)GaInP/(Al)GaInAs/Ge/Si 3JSC. The baseline structure is shown in Fig. 1 (further details can be found elsewhere [7]).

Table I: Summary of the minority carrier parameters used in the analysis of potential.

| Layer | | τ (ns) | | μ (cm ² /V·s) | SRV (cm·s) |
|-------------|---------|---|---|---------------------------------|---------------|
| | | TDD: $1 \cdot 10^4$ (cm ⁻²) | TDD: $5 \cdot 10^6$ (cm ⁻²) | | |
| Top cell | Emitter | 1 | 0.1 | 40 | 1000 |
| | Base | 10 | 1 | 1100 | 100 |
| Middle cell | Emitter | 2 | 0.2 | 100 | 1000 |
| | Base | 20 | 0.5 | 3100 | 10 |
| Bottom cell | Emitter | $1 \cdot 10^5$ | | 500 | 1000 |
| | Base | $1 \cdot 10^6$ | | 1000 | 2 |

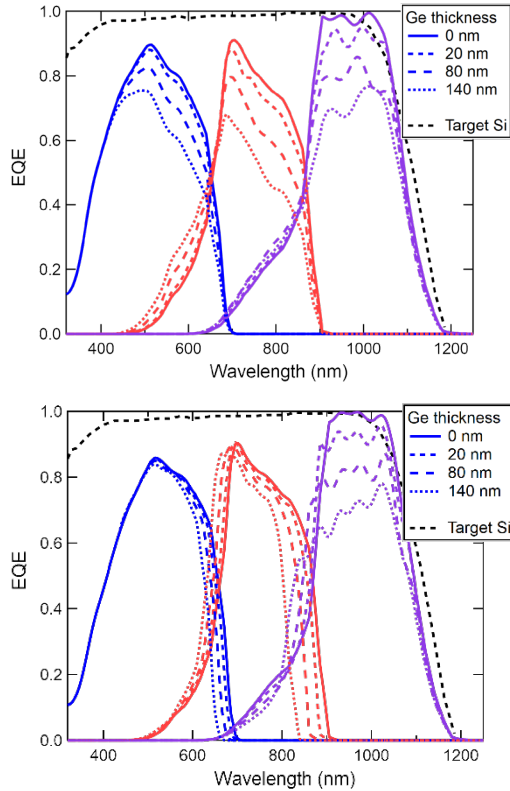


Figure 2: EQE of modeled current-matched 3JSC (AM1.5G solar spectrum) for different Ge layer thicknesses in the virtual substrate. Current matching for cells will Ge layer is achieved by: top: thinning the upper junctions; bottom: increasing the bandgap of the upper junctions using AlGaInP and AlGaAs. The dashed black line corresponds to the target EQE of the Si subcell.

Concerning the Si bottom cell, we assume the typical light trapping factor and back surface passivation achieved in III-V on Si designs [5]. We use typical experimental minority carrier parameters, as detailed in Table 1. We consider two scenarios: negligible TDD and the best value obtained in previous Ge/Si virtual substrates fabricated by RF-PECVD [4], which has a significant effect on the minority carrier properties [8]. Current developments on such virtual substrates are expected to improve the TDD, so with this analysis we are exploring the upper and lower performance limits that can be projected. We assume the same minority carrier parameters in the Al-containing compounds of the high bandgap design analyzed, since the Al compositions needed are below 10%.

Figure 2 shows the modeled EQE of current matched 3JSC for different thicknesses of the Ge layer in the virtual substrate. The graph on the top corresponds to a design (low-bandgap design) that achieves current matching as the Ge layer is made thicker by thinning the upper junctions. In the graph on the bottom (high-bandgap design) current matching is achieved by increasing the bandgap in these junctions, by using Al-containing compounds. It can be clearly observed how the EQE of the Si bottom junction is affected by the Ge layer, which forces the upper junctions to be thinned and lowering their EQE too. In the case of the high bandgap upper junctions, current is also lost as the Ge layer is made thicker, but the increased bandgap increases the junctions' voltage, assuming that their minority carrier parameters is preserved. It is important to point out that the total thickness of the III-V structure ranges from 1.5 to 2.2 μm , for the span of Ge layer thicknesses explored. These thicknesses are well below the critical thickness for crack propagation, a clear advantage of this 3JSC design to achieve crack-free III-V solar cells on Si substrates. Also, the EQE of the Si subcell is assumed to match the state-of-the-art, which implies using an efficient back passivation, light trapping and prevention of impurity diffusion during deposition of the III-V stack.

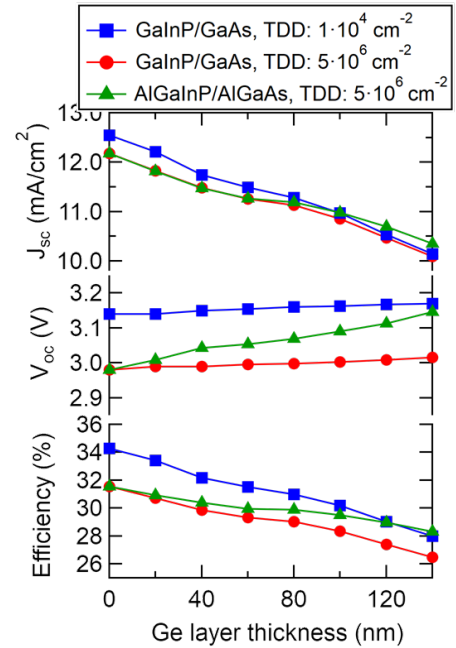


Figure 3: Modeled J_{sc} , V_{oc} and efficiency at 1-sun of the optimized 3JSC on Ge/Si vs the thickness of the Ge layer, for three design scenarios

Figure 3 shows a summary of the modeled electrical performance for the low and high bandgap cases with a TDD of $5 \cdot 10^6 \text{ cm}^{-2}$. The case of negligible TDD for the low bandgap design is also included. The J_{sc} , V_{oc} and efficiency of the cells at 1-sun is plotted versus the Ge layer thickness for the 3 cases described above. The effect of the TD in the performance is clearly observed. As the Ge layer thickness is increased and the upper junctions thinned, the minority carrier diffusion length becomes more resilient to the TD and so the J_{sc} of the high and low TDD cases converge. The thinning of the upper junction has also an effect on the V_{oc} , which slightly, but noticeably, increases as the Ge layer thickness is increased. The expected significant increase in the V_{oc} for the high bandgap case is also observed. Finally, the efficiency drop with Ge layer thickness is less steep for the high bandgap design, thanks to the effect of the V_{oc} increase. This efficiency chart shows that values between 30-34% can be achieved for Ge layer thicknesses below 60 nm. This must be considered when optimizing the Ge/Si templates. Besides, the significant effect of the TDD, despite the thin III-V junctions used, also encourages the pursue of lower TDD virtual substrates.

4 EXPERIMENTAL GAAS/GE/SI SOLAR CELLS

The preliminary experimental work presented here aimed to test the stability of the ultrathin Ge layer and its suitability as template for epitaxy. For this, we used virtual substrates with Ge layer thicknesses in the lower range, of just 20 nm. The test structure is depicted in Fig. 4. For this, we grew GaInAs cells using virtually the same process as in the case of standard Ge substrates. A GaInP nucleation layer was grown first, followed by a GaInAs overbuffer and a tunnel junction before the GaAs cell structure. In the fabrication of the devices, we did not attempt to modify the Si rear side to achieve any improved passivation or light trapping. Besides, we expect that some degradation of the Si substrate occurs during the MOVPE process, due to in-diffusion of impurities from the graphite susceptor, as described before [9]. All these issues will be addressed to achieve a proper EQE in the Si subcell in the future. Moreover, as commented in the Methods section, the Si substrates used were not fully epi-ready and they have not the optimum surface miscut. The reflectance of these virtual substrates was found to be virtually identical to standard Ge, but macroscopic defects developed during the III-V deposition affected the performance of the cells. The EQE and J-V curves obtained are shown in Fig. 5. Firstly, these measurements demonstrate functional devices with a reasonable performance for a first attempt using ultrathin Ge/Si virtual substrates. A well-defined response of the GaInAs and Si subcells is observed. An unusually high EQE for devices without ARC was measured, due to the antireflecting effect of the surface roughness. By measurement of the reflectance and comparison with that of similar devices on Ge substrates we could find a correction factor that was applied to the EQE curves. The modeling of the EQE data indicates a Si bottom cell with a back surface recombination around $1 \cdot 10^4 \text{ cm/s}$ and base lifetime over $1 \mu\text{s}$, as expected for the fabrication conditions used. The GaInAs subcell shows an EQE limited by the diffusion length in the base, below 600 nm, as evidenced also by the virtually identical curves for 2500 nm and 4000 nm thickness in the base layer of the devices (comparison not shown in Figure 5). The J-V

curves show a fine shape and low variability among the set of devices fabricated (J_{sc} varies due to different shadowing factor in the devices). The ideality factor of 3 in the 2JSC indicates that the GaInAs top cell is operating at $n=2$ regime, with a high J_{02} saturation current. The origin of the low minority diffusion length and low V_{oc} observed is mainly ascribed to the high TDD of the test virtual substrates used. Current experiments on new Ge/Si substrates show no macroscopic defects and a surface roughness comparable to standard Ge substrates that, together with optimized Ge layer deposition and thickness, are expected to enable a significant boost in the material quality and solar cell performance in the short term.

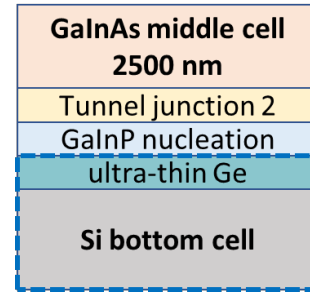


Figure 4: GaInAs/Si tandem solar cell structure used for the experimental test of the virtual substrates.

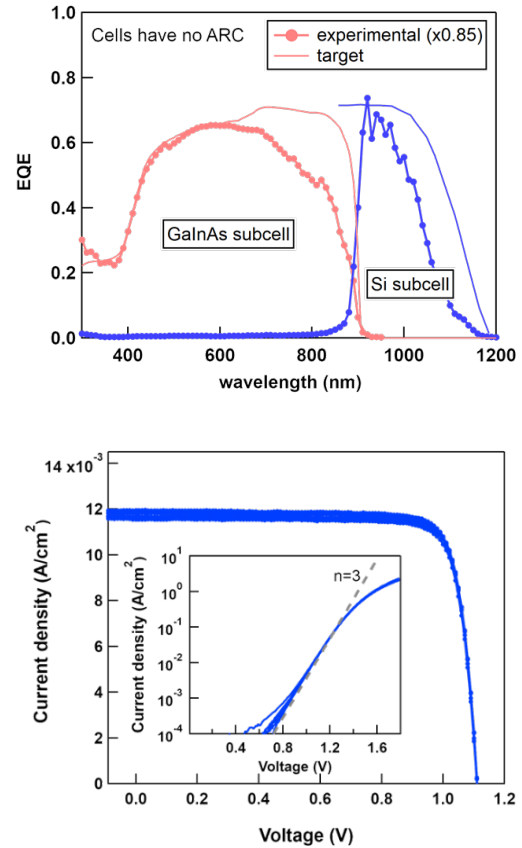


Figure 5: Top: Experimental EQE of the tandem solar cells implemented, compared to the target response. Bottom: uncalibrated light I-V curve of a set of devices. The inset shows the dark I-V curves.

5 SUMMARY AND CONCLUSIONS

Efficiencies approaching 34% are attainable with 3JSC on ultrathin Ge|Si substrates with an active Si bottom junction. For this, the Ge layer used must be kept below ~60 nm, and it is essential that a state-of-the-art Si solar cell performance is achieved in the bottom cell. The first III-V cells on ultrathin Ge|Si have been implemented and show functional devices with EQE and J-V results demonstrating the potential of these virtual substrates. An improved performance is expected as soon as the appropriate Si substrates are used to fabricate the Ge|Si templates with optimized Ge layers.

6 ACKNOWLEDGEMENT

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